

74ALVC373

Octal D-type transparent latch; 3-state

Rev. 3 — 30 April 2021

Product data sheet

1. General description

The 74ALVC373 is an octal D-type transparent latch with 3-state outputs. The device features latch enable (LE) and output enable (\overline{OE}) inputs. When LE is HIGH, data at the inputs enter the latches. In this condition the latches are transparent, a latch output will change each time its corresponding D-input changes. When LE is LOW the latches store the information that was present at the inputs a set-up time preceding the HIGH-to-LOW transition of LE. A HIGH on \overline{OE} causes the outputs to assume a high-impedance OFF-state. Operation of the \overline{OE} input does not affect the state of the latches. This device is fully specified for partial power down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

2. Features and benefits

- Wide supply voltage range from 1.65 V to 3.6 V
- 3.6 V tolerant inputs/outputs
- CMOS low power consumption
- Direct interface with TTL levels (2.7 V to 3.6 V)
- Power-down mode
- Latch-up performance exceeds 250 mA
- Complies with JEDEC standards:
 - JESD8-7 (1.65 V to 1.95 V)
 - JESD8-5 (2.3 V to 2.7 V)
 - JESD8B (2.7 V to 3.6 V)
- ESD protection:
 - HBM JESD22-A114E exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from -40 °C to +85 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74ALVC373D	-40 °C to +85 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74ALVC373PW	-40 °C to +85 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
74ALVC373BQ	-40 °C to +85 °C	DHVQFN20	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 × 4.5 × 0.85 mm	SOT764-1

4. Functional diagram

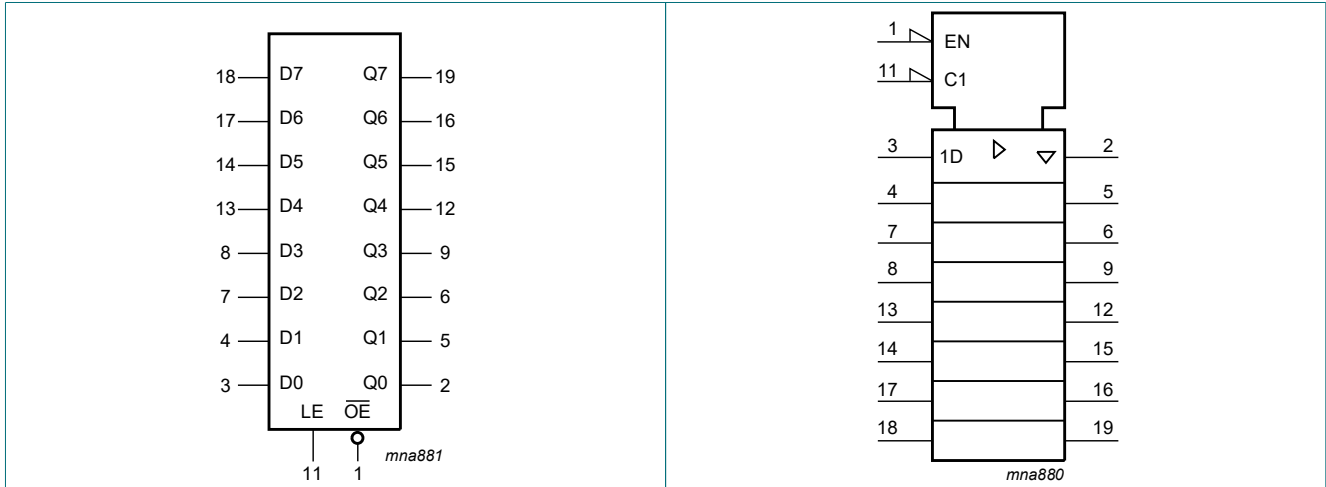


Fig. 1. Logic symbol

Fig. 2. IEC logic symbol

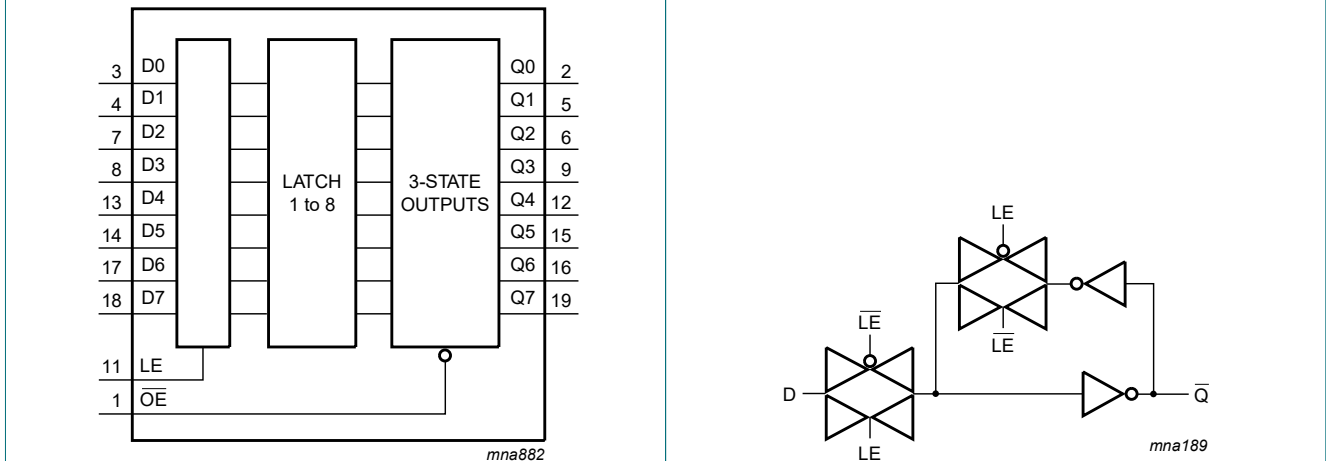


Fig. 3. Functional diagram

Fig. 4. Logic diagram (one latch)

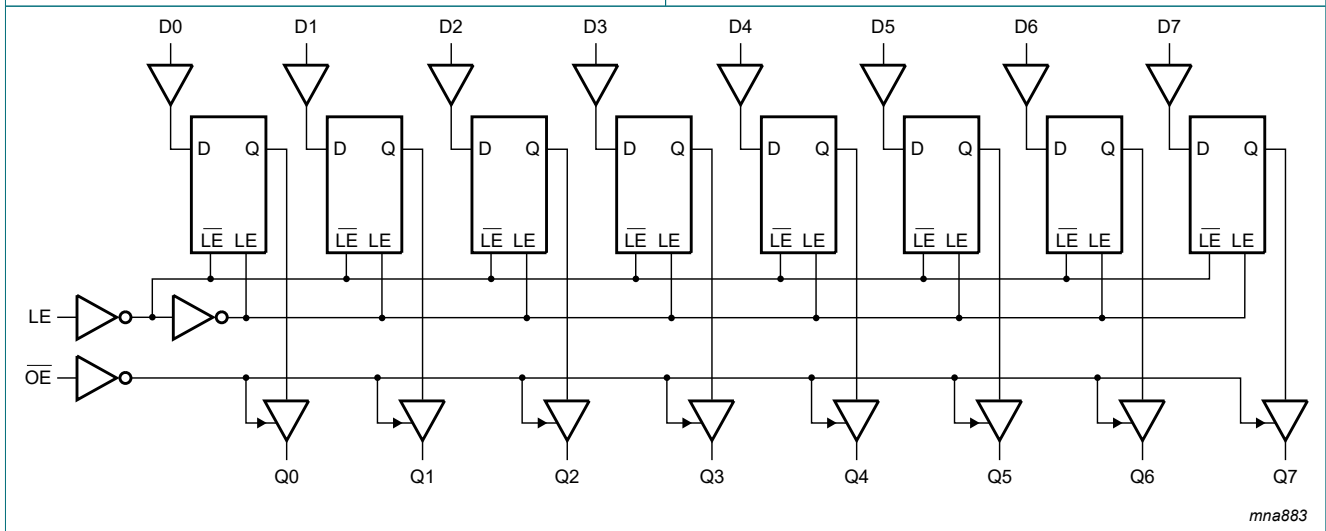
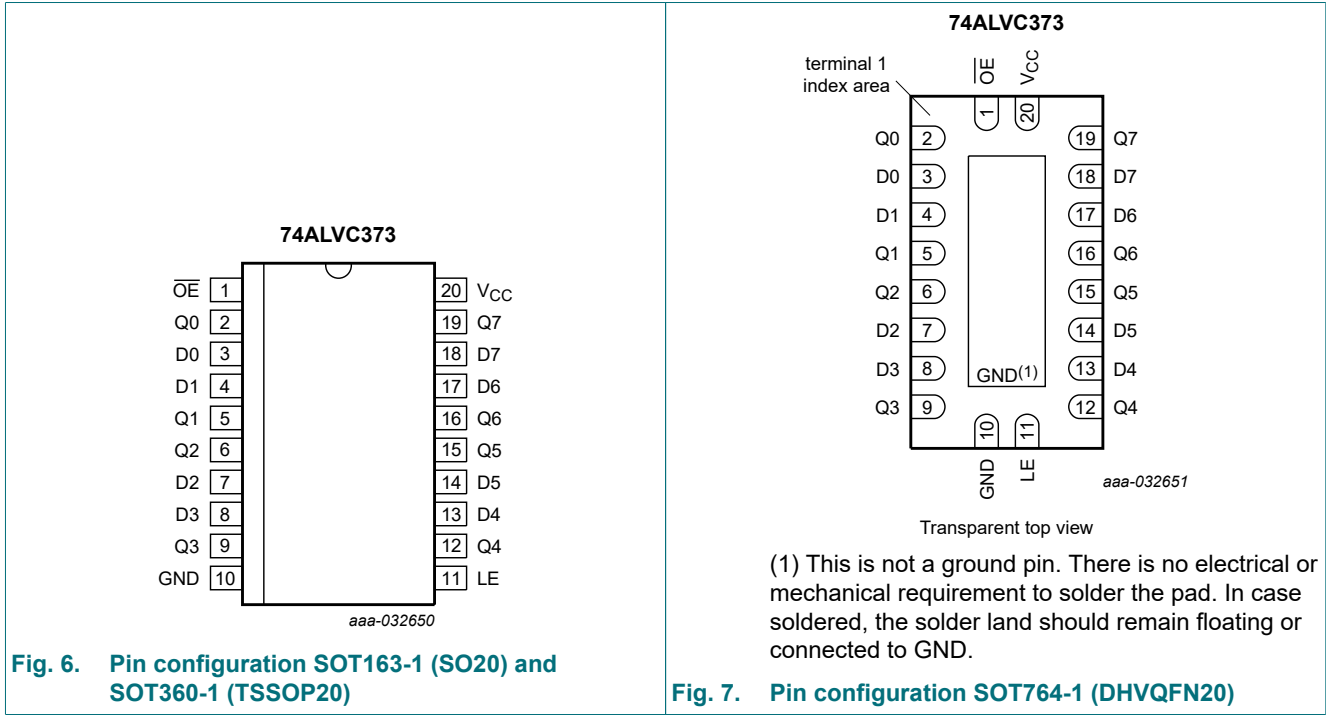


Fig. 5. Logic diagram

5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
D0, D1, D2, D3, D4, D5, D6, D7	3, 4, 7, 8, 13, 14, 17, 18	data input
LE	11	latch enable input (active HIGH)
OE	1	output enable input (active LOW)
Q0, Q1, Q2, Q3, Q4, Q5, Q6, Q7	2, 5, 6, 9, 12, 15, 16, 19	3-state latch output
V _{CC}	20	supply voltage
GND	10	ground (0 V)

6. Functional description

Table 3. Functional table

H = HIGH voltage level; h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition

L = LOW voltage level; l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition

X = don't care; Z = High-impedance OFF-state

Operating modes	Input			Internal latch	Output
	OE	LE	Dn		Qn
Enable and read register (transparent mode)	L	H	L	L	L
	L	H	H	H	H
Latch and read register	L	L	l	L	L
	L	L	h	H	H
Latch register and disable outputs	H	X	X	X	Z
	H	L	h	H	Z

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+4.6	V
I_{IK}	input clamping current	$V_I < 0$ V	-50	-	mA
V_I	input voltage	[1]	-0.5	+4.6	V
I_{OK}	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V	-	± 50	mA
V_O	output voltage	output HIGH or LOW state [1]	-0.5	$V_{CC} + 0.5$	V
		output 3-state	-0.5	+4.6	V
		power-down mode; $V_{CC} = 0$ V	-0.5	+4.6	V
I_O	output current	$V_O = 0$ V to V_{CC}	-	± 50	mA
I_{CC}	supply current		-	100	mA
I_{GND}	ground current		-100	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to +85 °C	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		1.65	3.6	V
V_I	input voltage		0	3.6	V
V_O	output voltage	output HIGH or LOW state	0	V_{CC}	V
		output 3-state	0	3.6	V
		power-down mode; $V_{CC} = 0$ V	0	3.6	V
T_{amb}	ambient temperature	in free air	-40	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.65$ V to 2.7 V	-	20	ns/V
		$V_{CC} = 2.7$ V to 3.6 V	-	10	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			Unit
			Min	Typ [1]	Max	
V_{IH}	HIGH-level input voltage	$V_{CC} = 1.65$ V to 1.95 V	$0.65 \times V_{CC}$	-	-	V
		$V_{CC} = 2.3$ V to 2.7 V	1.7	-	-	V
		$V_{CC} = 2.7$ V to 3.6 V	2.0	-	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 1.65$ V to 1.95 V	-	-	$0.35 \times V_{CC}$	V
		$V_{CC} = 2.3$ V to 2.7 V	-	-	0.7	V
		$V_{CC} = 2.7$ V to 3.6 V	-	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = -100$ μ A; $V_{CC} = 1.65$ V to 3.6 V	$V_{CC} - 0.2$	-	-	V
		$I_O = -6$ mA; $V_{CC} = 1.65$ V	1.25	1.51	-	V
		$I_O = -12$ mA; $V_{CC} = 2.3$ V	1.8	2.10	-	V
		$I_O = -18$ mA; $V_{CC} = 2.3$ V	1.7	2.01	-	V
		$I_O = -12$ mA; $V_{CC} = 2.7$ V	2.2	2.53	-	V
		$I_O = -18$ mA; $V_{CC} = 3.0$ V	2.4	2.76	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = 100$ μ A; $V_{CC} = 1.65$ V to 3.6 V	-	-	0.2	V
		$I_O = 6$ mA; $V_{CC} = 1.65$ V	-	0.11	0.3	V
		$I_O = 12$ mA; $V_{CC} = 2.3$ V	-	0.17	0.4	V
		$I_O = 18$ mA; $V_{CC} = 2.3$ V	-	0.25	0.6	V
		$I_O = 12$ mA; $V_{CC} = 2.7$ V	-	0.16	0.4	V
		$I_O = 18$ mA; $V_{CC} = 3.0$ V	-	0.23	0.4	V
I_I	input leakage current	$V_{CC} = 3.6$ V; $V_I = 3.6$ V or GND	-	± 0.1	± 5	μ A
		$V_I = V_{IH}$ or V_{IL} ; $V_{CC} = 1.65$ V to 3.6 V; $V_O = 3.6$ V or GND;	-	± 0.1	± 10	μ A
I_{OFF}	power-off leakage supply	$V_{CC} = 0$ V; V_I or $V_O = 0$ V to 3.6 V	-	± 0.1	± 10	μ A

Symbol	Parameter	Conditions	-40 °C to +85 °C			Unit
			Min	Typ [1]	Max	
I_{CC}	supply current	$V_{CC} = 3.6\text{ V}$; $V_I = V_{CC}$ or GND; $I_O = 0\text{ A}$	-	0.2	10	μA
ΔI_{CC}	additional supply current	per input pin; $V_{CC} = 3.0\text{ V}$ to 3.6 V ; $V_I = V_{CC} - 0.6\text{ V}$; $I_O = 0\text{ A}$	-	5	750	μA
C_I	input capacitance		-	3.5	-	pF

[1] All typical values are measured at $V_{CC} = 3.3\text{ V}$ (unless stated otherwise) and $T_{amb} = 25\text{ °C}$.

10. Dynamic characteristics

Table 7. Dynamic characteristics

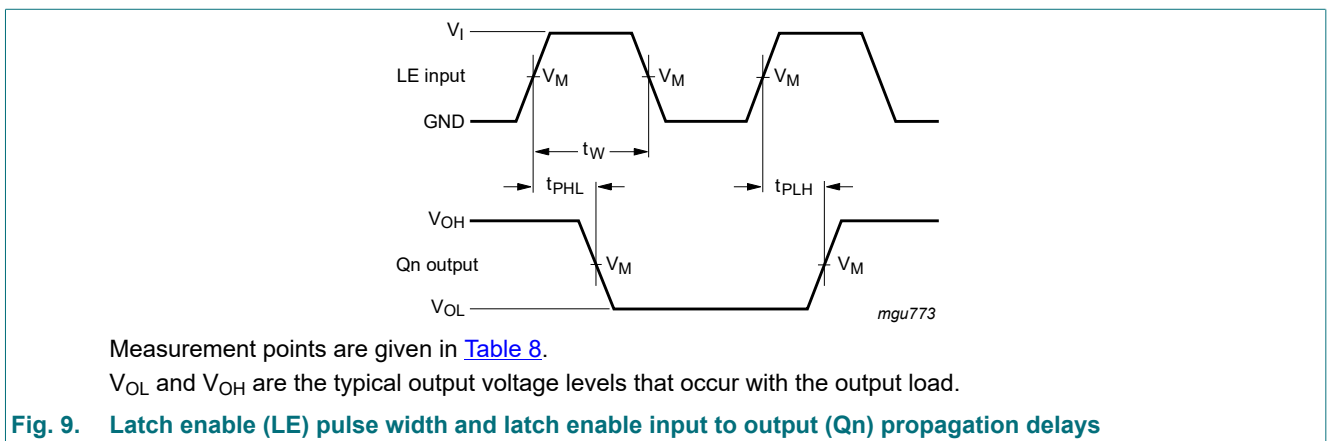
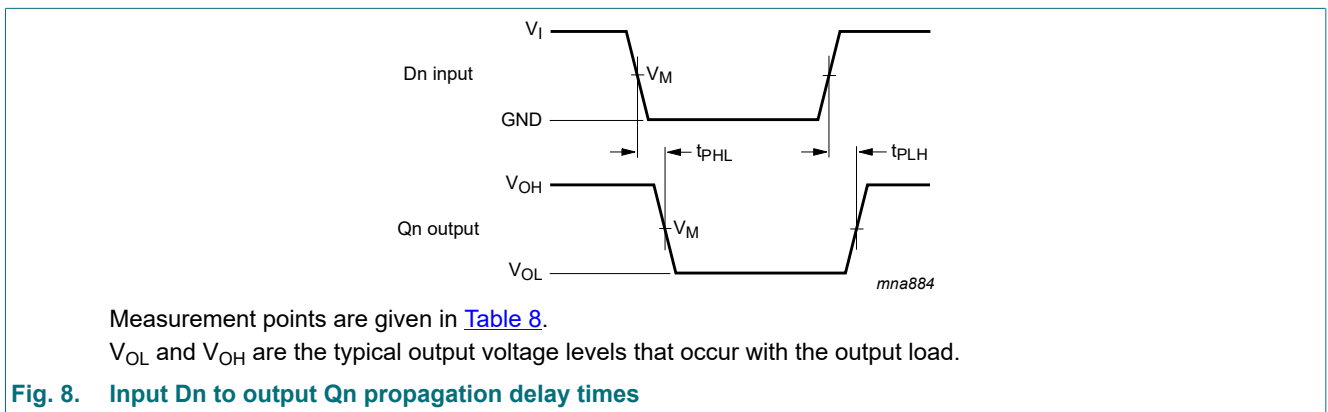
Voltages are referenced to GND (ground = 0 V). For test circuit see Fig. 12.

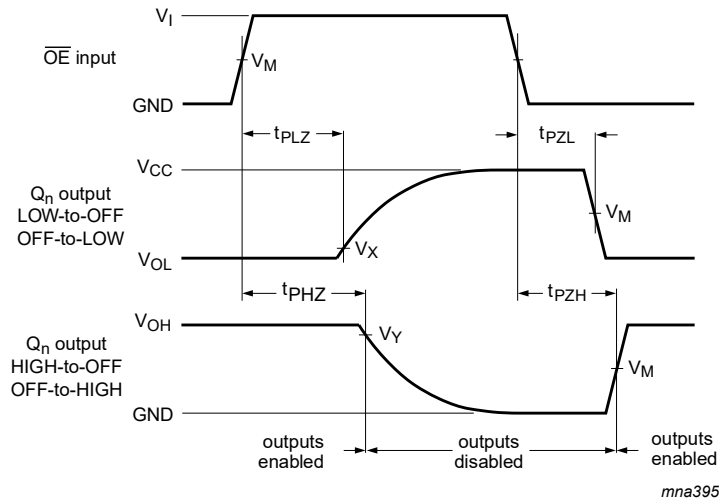
Symbol	Parameter	Conditions	-40 °C to +85 °C			Unit
			Min	Typ [1]	Max	
t_{pd}	propagation delay	Dn to Qn; see Fig. 8 [2]				
		$V_{CC} = 1.65\text{ V}$ to 1.95 V	1.0	2.5	5.4	ns
		$V_{CC} = 2.3\text{ V}$ to 2.7 V	1.0	2.0	3.5	ns
		$V_{CC} = 2.7\text{ V}$	1.0	2.3	3.6	ns
		$V_{CC} = 3.0\text{ V}$ to 3.6 V	1.0	2.2	3.3	ns
		LE to Qn; see Fig. 9				
		$V_{CC} = 1.65\text{ V}$ to 1.95 V	1.0	2.8	6.0	ns
		$V_{CC} = 2.3\text{ V}$ to 2.7 V	1.0	2.1	3.8	ns
		$V_{CC} = 2.7\text{ V}$	1.0	2.4	3.7	ns
		$V_{CC} = 3.0\text{ V}$ to 3.6 V	1.0	2.3	3.3	ns
t_{en}	enable time	\overline{OE} to Qn; see Fig. 10 [2]				
		$V_{CC} = 1.65\text{ V}$ to 1.95 V	1.5	3.0	6.4	ns
		$V_{CC} = 2.3\text{ V}$ to 2.7 V	1.0	2.4	4.5	ns
		$V_{CC} = 2.7\text{ V}$	1.5	3.0	4.6	ns
		$V_{CC} = 3.0\text{ V}$ to 3.6 V	1.0	2.3	4.0	ns
t_{dis}	disable time	\overline{OE} to Qn; see Fig. 10 [2]				
		$V_{CC} = 1.65\text{ V}$ to 1.95 V	1.5	3.4	7.0	ns
		$V_{CC} = 2.3\text{ V}$ to 2.7 V	1.0	2.2	4.4	ns
		$V_{CC} = 2.7\text{ V}$	1.5	2.8	4.4	ns
		$V_{CC} = 3.0\text{ V}$ to 3.6 V	1.0	2.7	4.4	ns
t_W	pulse width	LE pulse width HIGH; see Fig. 9				
		$V_{CC} = 1.65\text{ V}$ to 1.95 V	3.8	1.0	-	ns
		$V_{CC} = 2.3\text{ V}$ to 2.7 V	3.3	0.8	-	ns
		$V_{CC} = 2.7\text{ V}$	3.3	2.0	-	ns
		$V_{CC} = 3.0\text{ V}$ to 3.6 V	3.3	2.2	-	ns
t_{su}	set-up time	Dn to LE; see Fig. 11				
		$V_{CC} = 1.65\text{ V}$ to 1.95 V	0.8	0.1	-	ns
		$V_{CC} = 2.3\text{ V}$ to 2.7 V	0.8	0.1	-	ns
		$V_{CC} = 2.7\text{ V}$	0.8	0.1	-	ns
		$V_{CC} = 3.0\text{ V}$ to 3.6 V	0.8	0.1	-	ns

Symbol	Parameter	Conditions	-40 °C to +85 °C			Unit
			Min	Typ [1]	Max	
t _h	hold time	Dn to LE; see Fig. 11				
		V _{CC} = 1.65 V to 1.95 V	0.8	-0.1	-	ns
		V _{CC} = 2.3 V to 2.7 V	0.8	-0.2	-	ns
		V _{CC} = 2.7 V	0.8	-0.3	-	ns
C _{PD}	power dissipation capacitance	per latch; V _I = GND to V _{CC} ; V _{CC} = 3.3 V [3]				
		outputs HIGH or LOW state	-	35	-	pF
		outputs 3-state	-	14	-	pF

- [1] Typical values are measured at T_{amb} = 25 °C
- [2] t_{pd} is the same as t_{PHL} and t_{PLH}.
t_{en} is the same as t_{PZH} and t_{PZL}.
t_{dis} is the same as t_{PHZ} and t_{PLZ}.
- [3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz; f_o = output frequency in MHz
 C_L = output load capacitance in pF
 V_{CC} = supply voltage in Volts
 N = number of inputs switching
 Σ(C_L × V_{CC}² × f_o) = sum of the outputs

10.1. Waveforms and test circuit

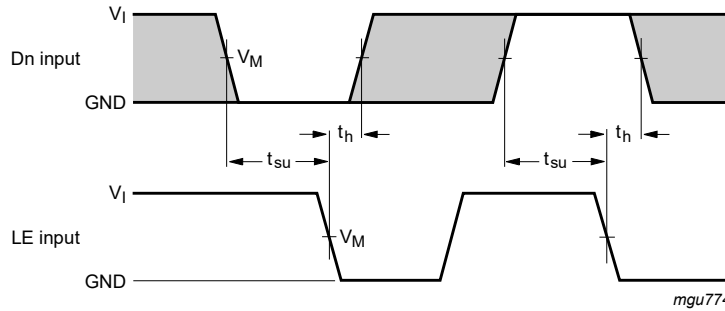




Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are the typical output voltage levels that occur with the output load.

Fig. 10. Enable and disable times



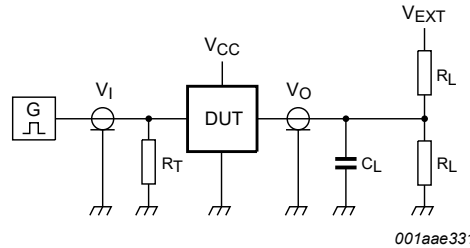
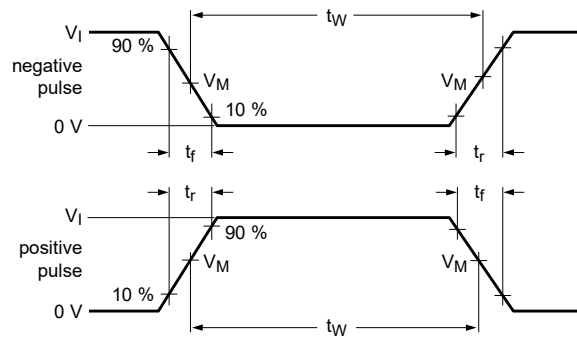
Measurement points are given in [Table 8](#).

The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig. 11. The data set-up and hold times for Dn input to LE input

Table 8. Measurement points

Supply voltage V_{CC}	V_M	Output	
		V_x	V_y
1.65 V to 1.95 V	$0.5V_{CC}$	$V_{OL} + 0.15 V$	$V_{OH} - 0.15 V$
2.3 V to 2.7 V	$0.5V_{CC}$	$V_{OL} + 0.15 V$	$V_{OH} - 0.15 V$
2.7 V	1.5 V	$V_{OL} + 0.3 V$	$V_{OH} - 0.3 V$
3.0 V to 3.6 V	1.5 V	$V_{OL} + 0.3 V$	$V_{OH} - 0.3 V$



001aae331

Test data is given in [Table 9](#).

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

Fig. 12. Test circuit for measuring switching times

Table 9. Test data

Supply voltage	Input		Load		V_{EXT}		
	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PLZ}, t_{PZL}	t_{PHZ}, t_{PZH}
1.65 V to 1.95 V	V_{CC}	≤ 2.0 ns	30 pF	1 k Ω	open	$2 \times V_{CC}$	GND
2.3 V to 2.7 V	V_{CC}	≤ 2.0 ns	30 pF	500 Ω	open	$2 \times V_{CC}$	GND
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	6 V	GND
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	6 V	GND

11. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1

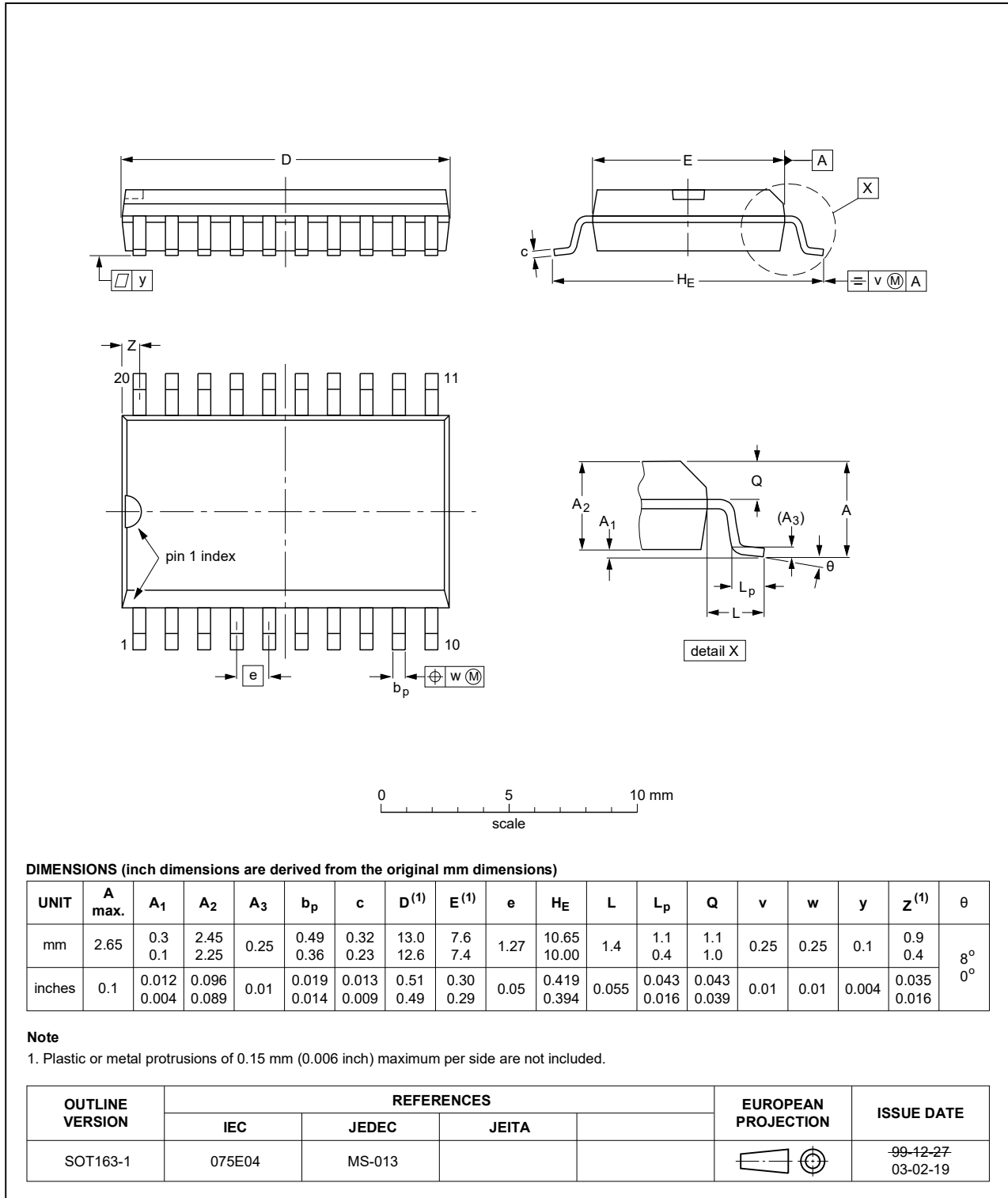


Fig. 13. Package outline SOT163-1 (SO20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1

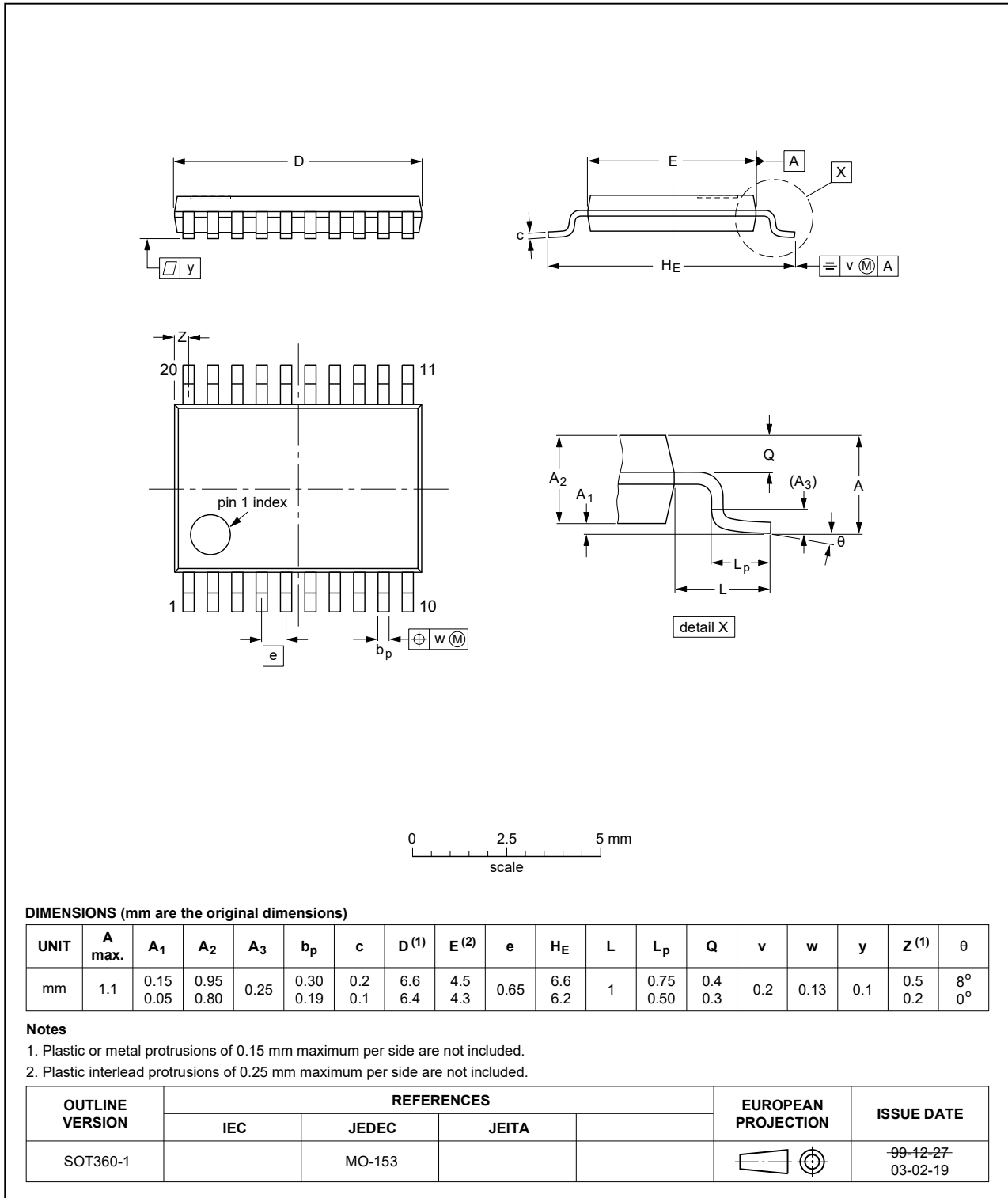


Fig. 14. Package outline SOT360-1 (TSSOP20)

DHVQFN20: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 x 4.5 x 0.85 mm

SOT764-1



Fig. 15. Package outline SOT764-1 (DHVQFN20)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74ALVC373 v.3	20210430	Product data sheet	-	74ALVC373 v.2
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Section 1 updated. Section 2: Reference to JESD36 removed. Section 7: Derating values for P_{tot} total power dissipation removed (errata). Fig. 9 and Fig. 11 corrected. Package outline drawing SOT764-1 (DHVQFN20) updated. 			
74ALVC373 v.2	20071018	Product data sheet	-	74ALVC373 v.1
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. Legal texts have been adapted to the new company name where appropriate. Section 3: DHVQFN20 package added. Section 7: derating values added for DHVQFN20 package. Section 11: outline drawing added for DHVQFN20 package. 			
74ALVC373 v.1	20020226	Product specification	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions".
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