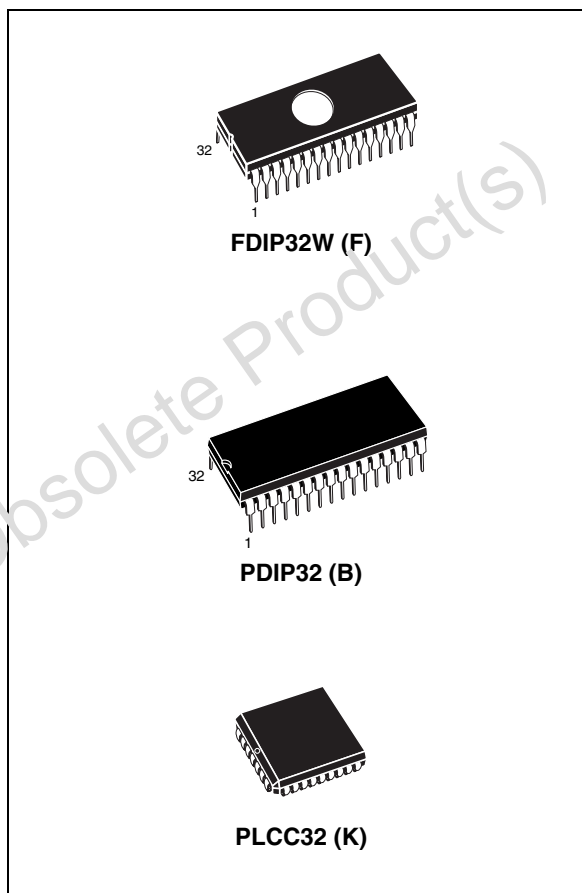


8 Mbit (1Mb x 8) UV EPROM and OTP EPROM**Features**

- 5 V \pm 10% supply voltage in Read operation
- Access time: 55 ns
- low Power Consumption:
 - Active current: 35 mA at 5 MHz
 - Standby current: 100 μ A
- Programming voltage: 12.75 V \pm 0.25 V
- Programming time: 50 μ s/word
- Electronic signature
 - Manufacturer code: 20h
 - Device code: 42h
- ECOPACK® packages available



Contents

| | | |
|----------|--|-----------|
| 1 | Description | 5 |
| 2 | Device description | 8 |
| 2.1 | Read mode | 8 |
| 2.2 | Standby mode | 8 |
| 2.3 | Two-line output control | 8 |
| 2.4 | System considerations | 9 |
| 2.5 | Programming | 9 |
| 2.6 | Presto IIB programming algorithm | 9 |
| 2.7 | Program Inhibit | 10 |
| 2.8 | Program Verify | 10 |
| 2.9 | Electronic Signature | 10 |
| 2.10 | Erasure operation (applies to UV EFRoM) | 11 |
| 3 | Maximum ratings | 12 |
| 4 | DC and AC characteristics | 13 |
| 5 | Package mechanical data | 19 |
| 5.1 | 32-pin ceramic frit-seal DIP, with round window (FDIP32WA) | 19 |
| 5.2 | 32-pin plastic DIP, 600 mils width (PDIP32) | 20 |
| 5.3 | 32-lead rectangular plastic leaded chip carrier (PLCC32) | 21 |
| 6 | Part numbering | 22 |
| 7 | Revision history | 23 |

List of tables

| | | |
|-----------|---|----|
| Table 1. | Signal descriptions | 6 |
| Table 2. | Operating modes | 8 |
| Table 3. | Electronic signature | 11 |
| Table 4. | Absolute maximum ratings | 12 |
| Table 5. | AC measurement conditions | 13 |
| Table 6. | Capacitance | 14 |
| Table 7. | Read mode DC characteristics | 14 |
| Table 8. | Programming mode DC characteristics | 15 |
| Table 9. | Read mode AC characteristics | 16 |
| Table 10. | Margin mode AC characteristics | 17 |
| Table 11. | Programming mode AC characteristics | 18 |
| Table 12. | FDIP32WA package mechanical data | 19 |
| Table 13. | PDIP32 package mechanical data | 20 |
| Table 14. | PLCC32 package mechanical data | 21 |
| Table 15. | Ordering information scheme | 22 |
| Table 16. | Document revision history | 23 |

List of figures

| | | |
|------------|---|----|
| Figure 1. | Logic diagram | 5 |
| Figure 2. | DIP connections | 6 |
| Figure 3. | PLCC connections | 7 |
| Figure 4. | Programming flowchart | 10 |
| Figure 5. | AC testing input output waveform | 13 |
| Figure 6. | AC testing load circuit | 14 |
| Figure 7. | Read mode AC waveforms | 16 |
| Figure 8. | Margin mode AC waveforms | 17 |
| Figure 9. | Programming and verify modes AC waveforms | 18 |
| Figure 10. | FDIP32WA package outline | 19 |
| Figure 11. | PDIP32 package outline | 20 |
| Figure 12. | PLCC32 package outline | 21 |

Obsolete Product(s) - Obsolete Product(s)

1 Description

The M27C801 is an 8 Mbit EPROM offered in the two ranges UV (ultra violet erase) and OTP (one time programmable). It is ideally suited for applications where fast turn-around and pattern experimentation are important requirements and is organized as 1,048,576 by 8 bits.

The FDIP32W (window ceramic frit-seal package) has transparent lid which allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

For applications where the content is programmed only one time and erasure is not required, the M27C801 is offered in PDIP32 and PLCC32 packages.

In order to meet environmental requirements, ST offers the M27C801 in ECOPACK® packages. ECOPACK packages are Lead-free. The category of second-level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

ECOPACK is an ST trademark. ECOPACK® specifications are available at: www.st.com.

See [Figure 1: Logic diagram](#) and [Table 1: Signal descriptions](#) for a brief overview of the signals connected to this device.

Figure 1. Logic diagram

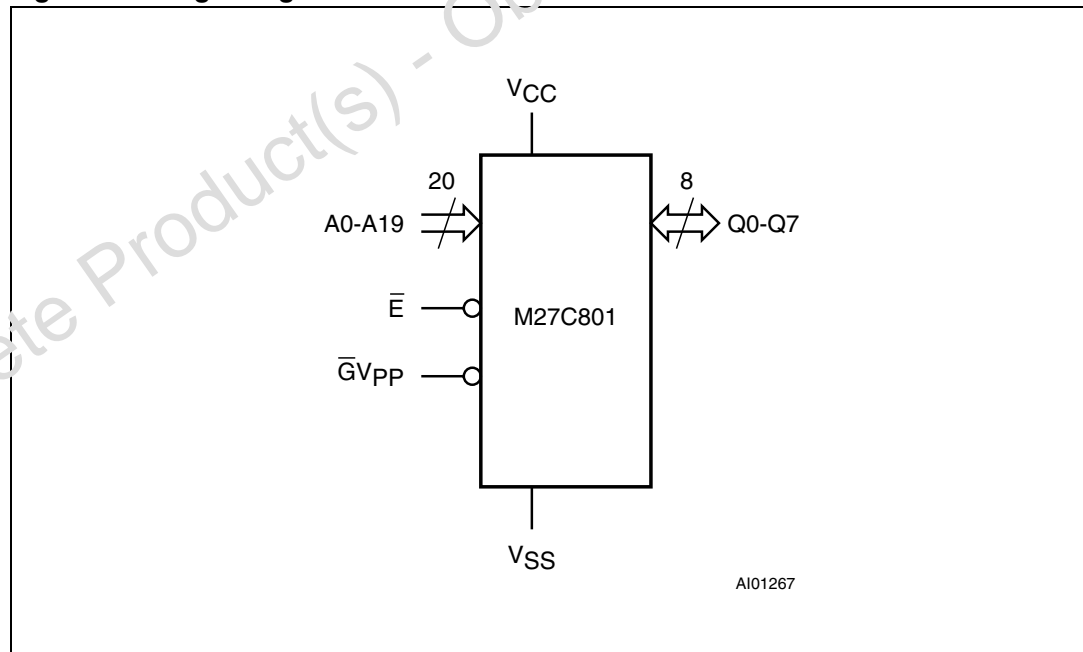


Table 1. Signal descriptions

| Signal | Description |
|-----------------|--------------------------------|
| A0-A19 | Address inputs |
| Q0-Q7 | Data outputs |
| \bar{E} | Chip Enable |
| $\bar{G}V_{PP}$ | Output enable / program supply |
| V_{CC} | Supply voltage |
| V_{SS} | Ground |

Figure 2. DIP connections

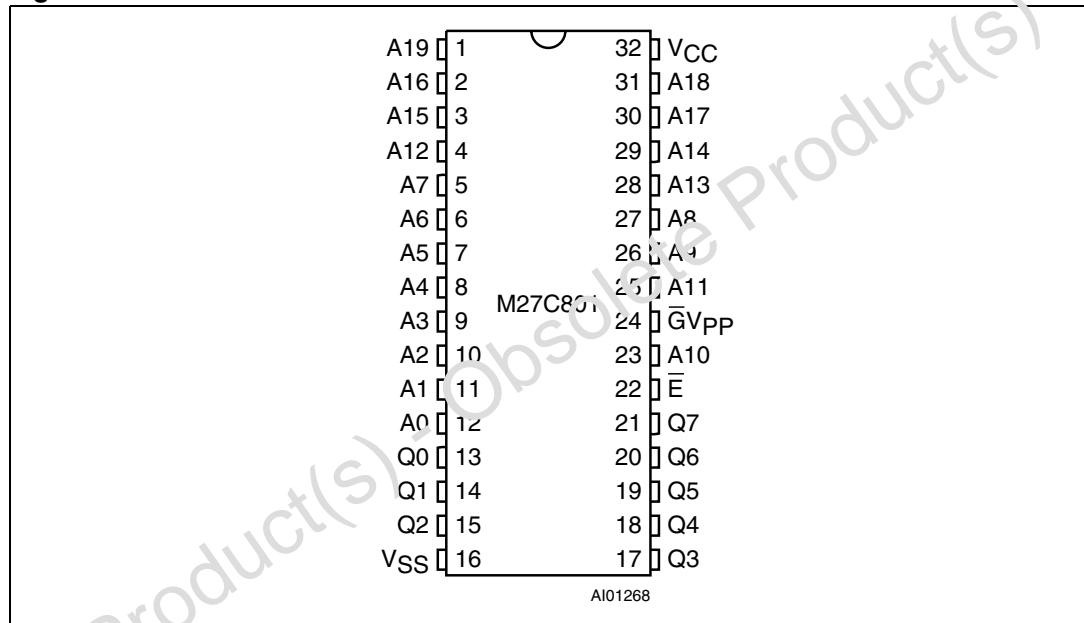
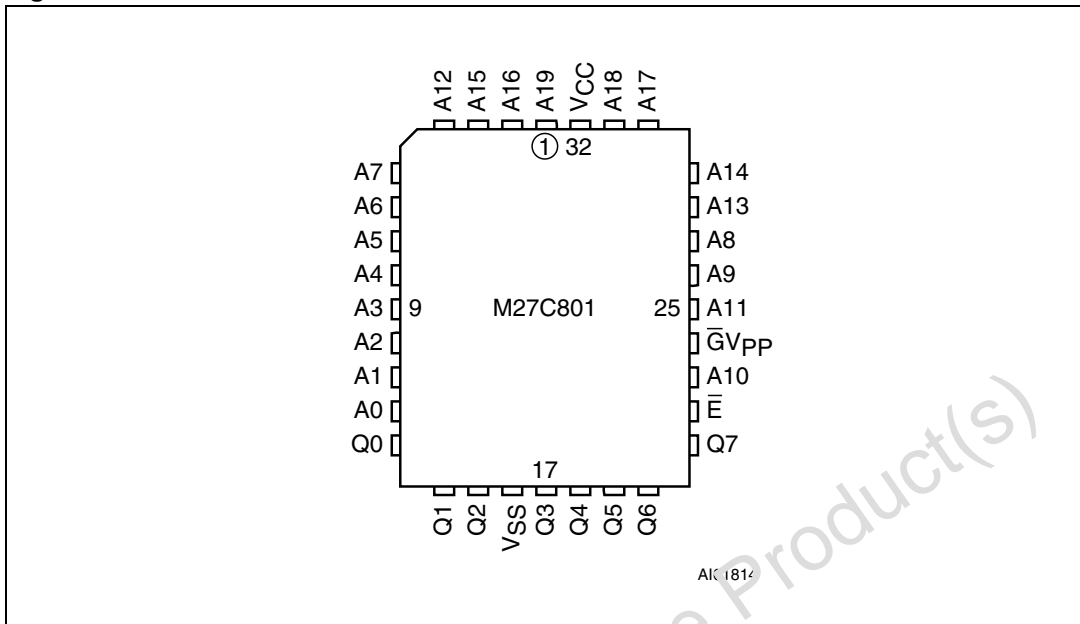


Figure 3. PLCC connections



Obsolete Product(s) - Obsolete Product(s)

2 Device description

The operating modes of the M27C801 are listed in the Operating Modes table. A single power supply is required in Read mode. All inputs are TTL levels except for $\overline{G}V_{PP}$ and 12V on A9 for Electronic Signature and Margin Mode Set or Reset.

Table 2. Operating modes ⁽¹⁾

| Mode | \overline{E} | $\overline{G}V_{PP}$ | A9 | Q7-Q0 |
|----------------------|----------------|----------------------|----------|----------|
| Read | V_{IL} | V_{IL} | X | Data Out |
| Output Disable | V_{IL} | V_{IH} | X | Hi-Z |
| Program | V_{IL} Pulse | V_{PP} | X | Data In |
| Program Inhibit | V_{IH} | V_{PP} | X | Hi-Z |
| Standby | V_{IH} | X | X | Hi-Z |
| Electronic signature | V_{IL} | V_{IL} | V_{IC} | Codes |

1. X = V_{IH} or V_{IL} , $V_{ID} = 12 V \pm 0.5 V$.

2.1 Read mode

The M27C801 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable (\overline{E}) is the power control and should be used for device selection. Output Enable (\overline{G}) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, the address access time (t_{AVQV}) is equal to the delay from \overline{E} to output (t_{ELQV}). Data is available at the output after a delay of t_{GLQV} from the falling edge of \overline{G} , assuming that \overline{E} has been low and the addresses have been stable for at least $t_{AVQV} - t_{GLQV}$.

2.2 Standby mode

The M27C801 has a standby mode which reduces the supply current from 35mA to 100 μ A.

The M27C801 is placed in the standby mode by applying a CMOS high signal to the \overline{E} input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{G}V_{PP}$ input.

2.3 Two-line output control

Because EPROMs are usually used in larger memory arrays, the product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows:

- the lowest possible memory power dissipation,
- complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, \overline{E} should be decoded and used as the primary device selecting function, while \overline{G} should be made a common connection to all devices in the array and connected to the READ line from the system control bus. This

ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is required from a particular memory device.

2.4 System considerations

The power switching characteristics of Advanced CMOS EPROMs require careful decoupling of the devices. The supply current, I_{CC} , has three segments that are of interest to the system designer: the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of \bar{E} . The magnitude of the transient current peaks is dependent on the capacitive and inductive loading of the device at the output. The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 0.1 μF ceramic capacitor be used on every device between V_{CC} and V_{SS} . This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for every eight devices. The bulk capacitor should be located near the power supply connection point. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

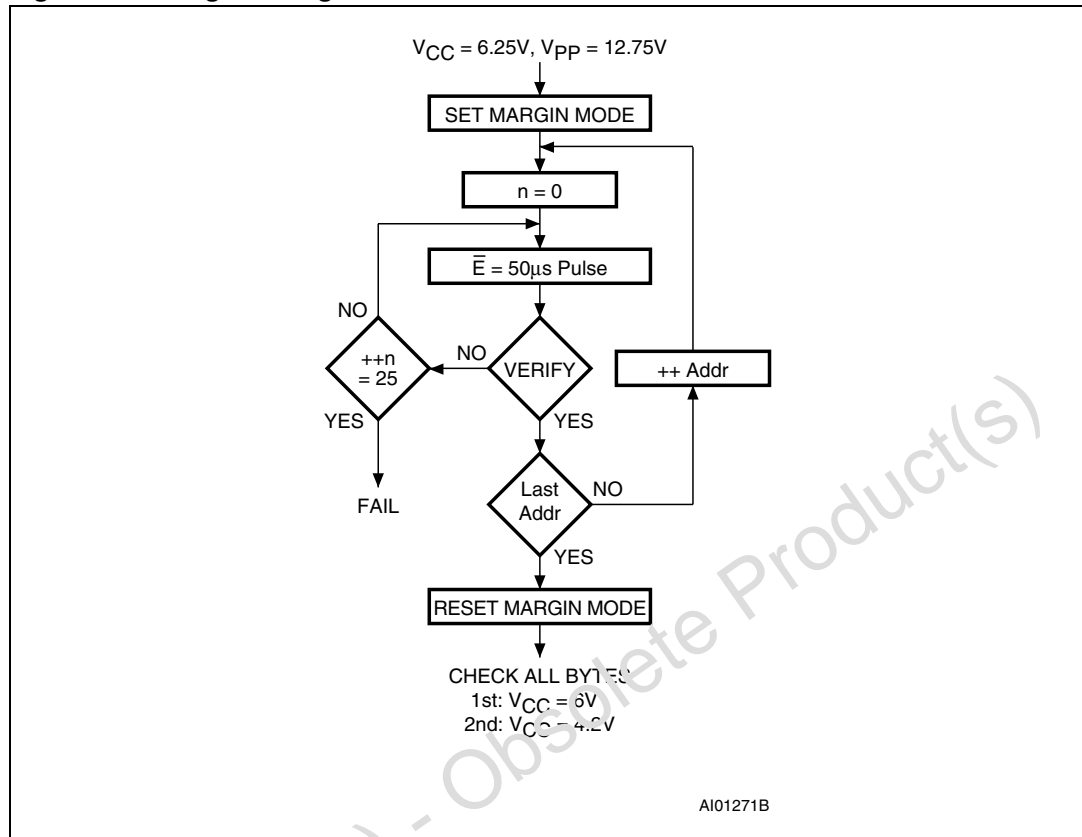
2.5 Programming

When delivered (and after each erasure for UV EPROM), all bits of the M27C801 are in the '1' state. Data is introduced by selectively programming '0's into the desired bit locations. Although only '0' will be programmed, both '1's and '0's can be present in the data word. The only way to change a '0' to a '1' is by die exposure to ultraviolet light (UV EPROM). The M27C801 is in the programming mode when V_{PP} input is at 12.75V and \bar{E} is pulsed to V_{IL} . The data to be programmed is applied to 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL. V_{CC} is specified to be $6.25\text{V} \pm 0.25\text{V}$.

2.6 Presto II B programming algorithm

Presto II B Programming Algorithm allows the whole array to be programmed with a guaranteed margin, in a typical time of 52.5 seconds. This can be achieved with STMicroelectronics M27C801 due to several design innovations to improve programming efficiency and to provide adequate margin for reliability. Before starting the programming the internal Margin Mode circuit is set in order to guarantee that each cell is programmed with enough margin. Then a sequence of 50 μs program pulses are applied to each byte until a correct Verify occurs (see [Figure 4](#)). No overprogram pulses are applied since the Verify in Margin Mode provides the necessary margin.

Figure 4. Programming flowchart



2.7 Program Inhibit

Programming of multiple M27C801s in parallel with different data is also easily accomplished. Except for \bar{E} , all like inputs including V_{PP} of the parallel M27C801 may be common. A TTL low level pulse applied to a M27C801's \bar{E} input, with V_{PP} at 12.75V, will program that M27C801. A high level \bar{E} input inhibits the other M27C801s from being programmed.

2.8 Program Verify

A Verify (Read) should be performed on the programmed bits to determine that they were correctly programmed. The Verify is accomplished with \bar{G} at V_{IL} . Data should be verified with t_{ELQV} after the falling edge of \bar{E} .

2.9 Electronic Signature

The Electronic Signature (ES) mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. The ES mode is functional in the $25^{\circ}\text{C} \pm 5^{\circ}\text{C}$ ambient temperature range that is required when programming the M27C801. To activate

the ES mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the M27C801. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH} . All other address lines must be held at V_{IL} during Electronic Signature mode. Byte 0 ($A0 = V_{IL}$) represents the manufacturer code and byte 1 ($A0 = V_{IH}$) the device identifier code. For the STMicroelectronics M27C801, these two identifier bytes are given in [Table 3](#) and can be read-out on outputs Q7 to Q0.

Table 3. Electronic signature

| Identifier | A0 | Q7 | Q6 | Q5 | Q4 | Q3 | Q2 | Q1 | Q0 | Hex Data |
|-------------------|----------|----|----|----|----|----|----|----|----|----------|
| Manufacturer code | V_{IL} | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 20h |
| Device code | V_{IH} | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 42h |

2.10 Erasure operation (applies to UV EPROM)

The erasure characteristics of the M27C801 is such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Å. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000 Å range. Research shows that constant exposure to room level fluorescent lighting could erase a typical M27C801 in about 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the M27C801 is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M27C801 window to prevent unintentional erasure. The recommended erasure procedure for the M27C801 is exposure to short wave ultraviolet light which has wavelength 2537 Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 30 W-sec/cm². The erasure time with this dosage is approximately 30 to 40 minutes using an ultraviolet lamp with 12000 µW/cm² power rating. The M27C801 should be placed within 2.5 cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

3 Maximum ratings

Stressing the device outside the ratings listed in [Table 4](#) may cause permanent damage to the device. These are stress ratings only, and operation of the device at these, or any other conditions outside those indicated in the Operating sections of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 4. Absolute maximum ratings

| Symbol | Parameter | Value | Unit |
|-------------------------|--|------------|------|
| T_A | Ambient operating temperature ⁽¹⁾ | -40 to 125 | °C |
| T_{BIAS} | Temperature under bias | -50 to 125 | °C |
| T_{STG} | Storage temperature | -60 to 150 | °C |
| V_{IO} ⁽²⁾ | Input or output voltage (except A9) | -2 to 7 | V |
| V_{CC} | Supply voltage | -2 to 7 | V |
| V_{A9} ⁽²⁾ | A9 voltage | -2 to 13.5 | V |
| V_{PP} | Program supply voltage | -2 to 14 | V |

1. Depends on range.
2. Minimum DC voltage on Input or Output is -0.5 V with possible undershoot to -2.0 V for a period less than 20 ns. Maximum DC voltage on Output is $V_{CC} + 0.5$ V with possible overshoot to $V_{CC} + 2$ V for a period less than 20 ns.

4 DC and AC characteristics

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristic tables that follow are derived from tests performed under the measurement conditions summarized in the relevant tables. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

Table 5. AC measurement conditions

| Parameter | High Speed | Standard |
|---------------------------------------|--------------------|---------------------------------|
| Input rise and fall times | $\leq 10\text{ns}$ | $\leq 20\text{ns}$ (10% to 90%) |
| Input pulse voltages | 0 to 3V | 0.4 to 2.4V |
| Input and output timing ref. voltages | 1.5V | 0.8 and 2V |

Figure 5. AC testing input output waveform

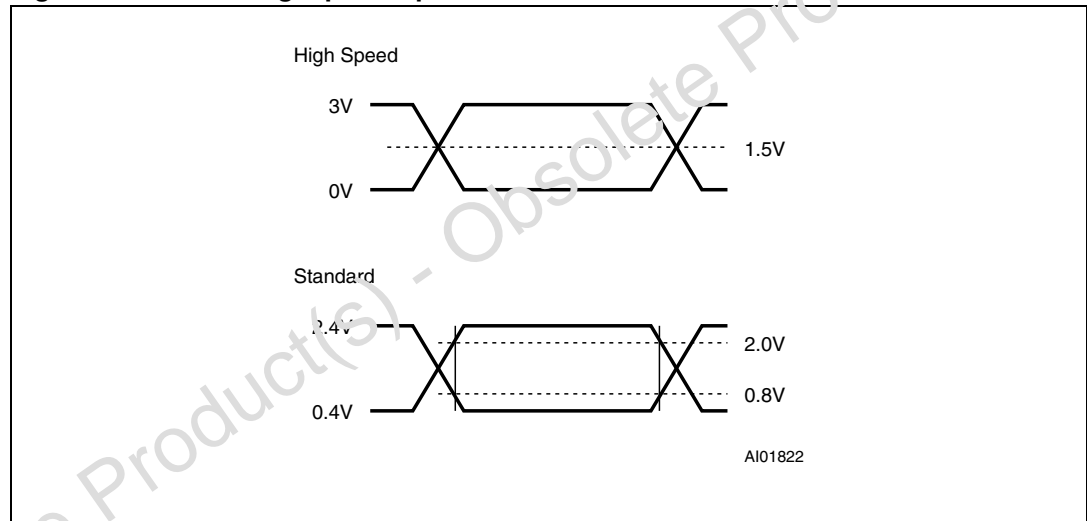


Figure 6. AC testing load circuit

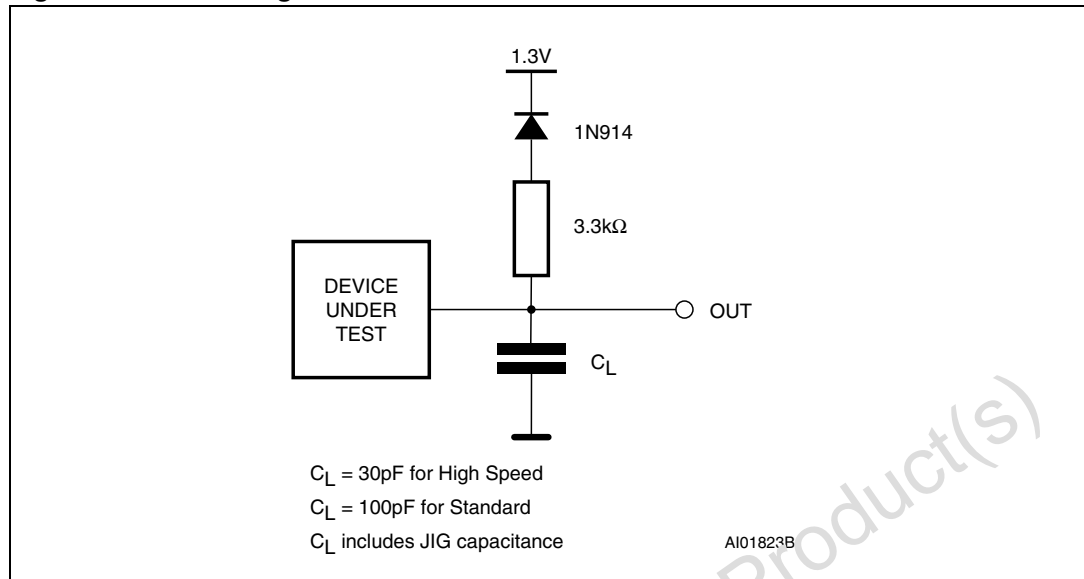


Table 6. Capacitance^{(1) (2)}

| Symbol | Parameter | Test condition | Min. | Max. | Unit |
|-----------|--------------------|------------------------|------|------|------|
| C_{IN} | Input capacitance | $V_{IH} = 0\text{ V}$ | | 6 | pF |
| C_{OUT} | Output capacitance | $V_{OUT} = 0\text{ V}$ | | 12 | pF |

- $T_A = 25\text{ °C}$, $f = 1\text{ MHz}$.
- Sampled only, not 100% tested.

Table 7. Read mode DC characteristics^{(1) (2)}

| Symbol | Parameter | Test condition | Min. | Max. | Unit |
|----------------|-------------------------------|--|----------------|--------------|---------------|
| I_{LI} | Input leakage current | $0\text{ V} \leq V_{IN} \leq V_{CC}$ | | ± 10 | μA |
| I_{LO} | Output leakage current | $0\text{ V} \leq V_{OUT} \leq V_{CC}$ | | ± 10 | μA |
| I_{CC} | Supply current | $\bar{E} = V_{IL}$, $\overline{G}V_{PP} = V_{IL}$, $I_{OUT} = 0\text{ mA}$, $f = 5\text{ MHz}$ | | 35 | mA |
| I_{CC1} | Supply current (Standby) TTL | $\bar{E} = V_{IH}$ | | 1 | mA |
| I_{CC2} | Supply current (Standby) CMOS | $\bar{E} > V_{CC} - 0.2\text{ V}$ | | 100 | μA |
| I_{PP} | Program current | $V_{PP} = V_{CC}$ | | 10 | μA |
| V_{IL} | Input low voltage | | -0.3 | 0.8 | V |
| $V_{IH}^{(3)}$ | Input high voltage | | 2 | $V_{CC} + 1$ | V |
| V_{OL} | Output low voltage | $I_{OL} = 2.1\text{ mA}$ | | 0.4 | V |
| V_{OH} | Output high voltage TTL | $I_{OH} = -1\text{ mA}$ | 3.6 | | V |
| | Output high voltage CMOS | $I_{OH} = -100\text{ }\mu\text{A}$ | $V_{CC} - 0.7$ | | V |

- $T_A = 0$ to 70 °C or -40 to 85 °C ; $V_{CC} = 5\text{ V} \pm 10\%$.
- V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP} .
- Maximum DC voltage on Output is $V_{CC} + 0.5\text{ V}$.

Table 8. Programming mode DC characteristics^{(1) (2)}

| Symbol | Parameter | Test condition | Min. | Max. | Unit |
|----------|-------------------------|----------------------------------|------|----------------|------|
| I_{LI} | Input leakage current | $V_{IL} \leq V_{IN} \leq V_{IH}$ | | ±10 | µA |
| I_{CC} | Supply current | | | 50 | mA |
| I_{PP} | Program current | $\bar{E} = V_{IL}$ | | 50 | mA |
| V_{IL} | Input low voltage | | -0.3 | 0.8 | V |
| V_{IH} | Input high voltage | | 2 | $V_{CC} + 0.5$ | V |
| V_{OL} | Output low voltage | $I_{OL} = 2.1\text{mA}$ | | 0.4 | V |
| V_{OH} | Output high voltage TTL | $I_{OH} = -1\text{mA}$ | 3.6 | | V |
| V_{ID} | A9 voltage | | 11.5 | 12.5 | V |

1. $T_A = 25\text{ °C}$; $V_{CC} = 6.25\text{V} \pm 0.25\text{V}$; $V_{PP} = 12.75\text{V} \pm 0.25\text{V}$

2. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP} .

Table 9. Read mode AC characteristics^{(1) (2)}

| Symbol | Alt | Parameter | Test condition | -55 ⁽³⁾ | | -80/-90 | | -100 | | Unit |
|---------------------------------|------------------|---|--|--------------------|------|---------|------|------|------|------|
| | | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| t _{AVQV} | t _{ACC} | Address valid to output valid | $\bar{E} = V_{IL}, \bar{G}V_{PP} = V_{IL}$ | | 55 | | 80 | | 100 | ns |
| t _{ELQV} | t _{CE} | Chip Enable low to output valid | $\bar{G}V_{PP} = V_{IL}$ | | 55 | | 80 | | 100 | ns |
| t _{GLQV} | t _{OE} | Output Enable low to output valid | $\bar{E} = V_{IL}$ | | 30 | | 40 | | 50 | ns |
| t _{EHQZ⁽⁴⁾} | t _{DF} | Chip Enable high to output Hi-Z | $\bar{G}V_{PP} = V_{IL}$ | 0 | 25 | 0 | 35 | 0 | 40 | ns |
| t _{GHQZ⁽⁴⁾} | t _{DF} | Output Enable high to output Hi-Z | $\bar{E} = V_{IL}$ | 0 | 25 | 0 | 35 | 0 | 40 | ns |
| t _{AXQX} | t _{OH} | Address transition to output transition | $\bar{E} = V_{IL}, \bar{G}V_{PP} = V_{IL}$ | 0 | | 0 | | 0 | | ns |

1. T_A = 0 to 70 °C or -40 to 85 °C; V_{CC} = 5 V ± 10%.
2. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
3. Speed obtained with High Speed AC measurement conditions.
4. Sampled only, not 100% tested.

Figure 7. Read mode AC waveforms

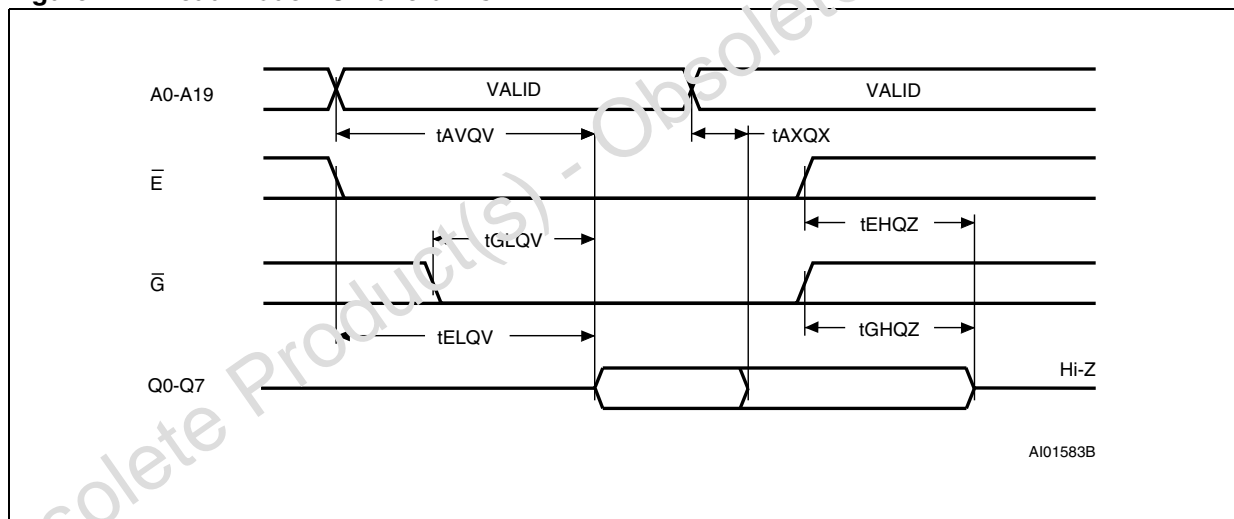


Table 10. Margin mode AC characteristics^{(1) (2)}

| Symbol | Alt | Parameter | Test condition | Min | Max | Unit |
|--------------|------------|--|----------------|-----|-----|---------|
| t_{A9HVPH} | t_{AS9} | V_{A9} high to V_{PP} high | | 2 | | μs |
| t_{VPHEL} | t_{VPS} | V_{PP} high to Chip Enable low | | 2 | | μs |
| t_{A10HEH} | t_{AS10} | V_{A10} high to Chip Enable high (Set) | | 1 | | μs |
| t_{A10LEH} | t_{AS10} | V_{A10} low to Chip Enable high (Reset) | | 1 | | μs |
| t_{EXA10X} | t_{AH10} | Chip Enable transition to V_{A10} transition | | 1 | | μs |
| t_{EXVPX} | t_{VPH} | Chip Enable transition to V_{PP} transition | | 2 | | μs |
| t_{VPXA9X} | t_{AH9} | V_{PP} transition to V_{A9} transition | | 2 | | μs |

1. $T_A = 25\text{ }^\circ\text{C}$; $V_{CC} = 6.25\text{ V} \pm 0.25\text{ V}$; $V_{PP} = 12.75\text{ V} \pm 0.25\text{ V}$

2. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP} .

Figure 8. Margin mode AC waveforms

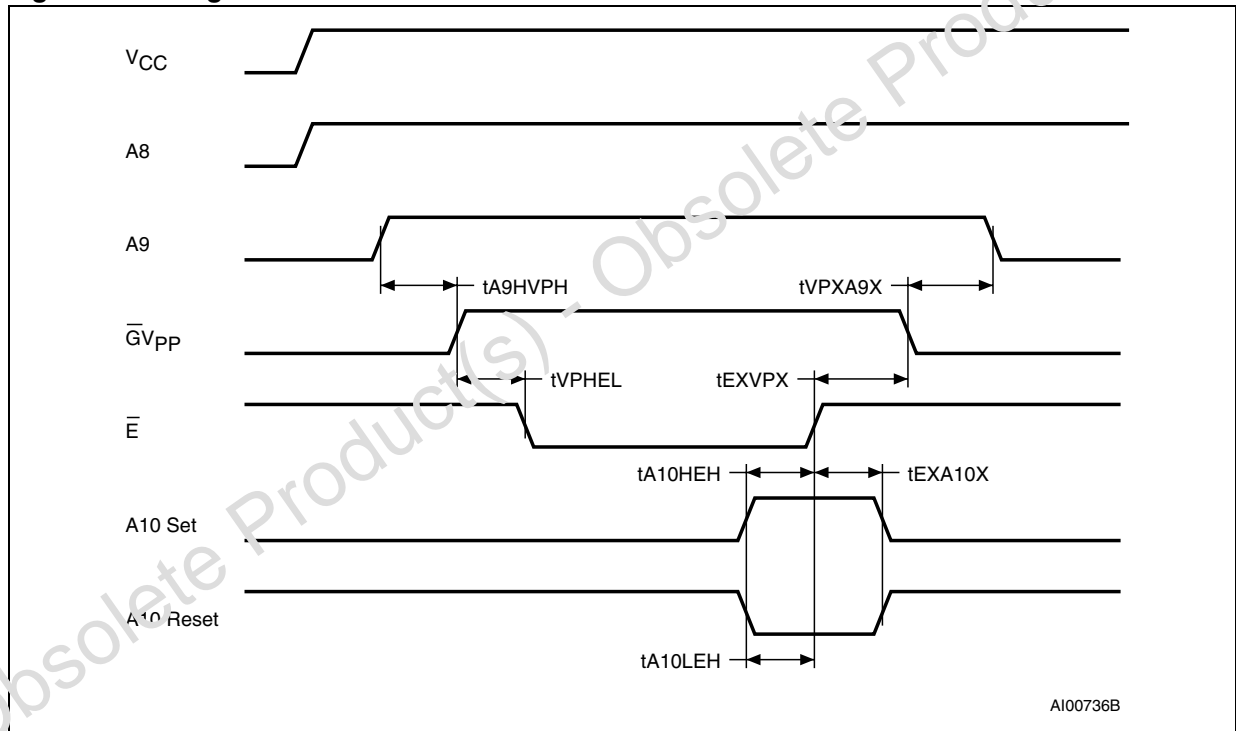
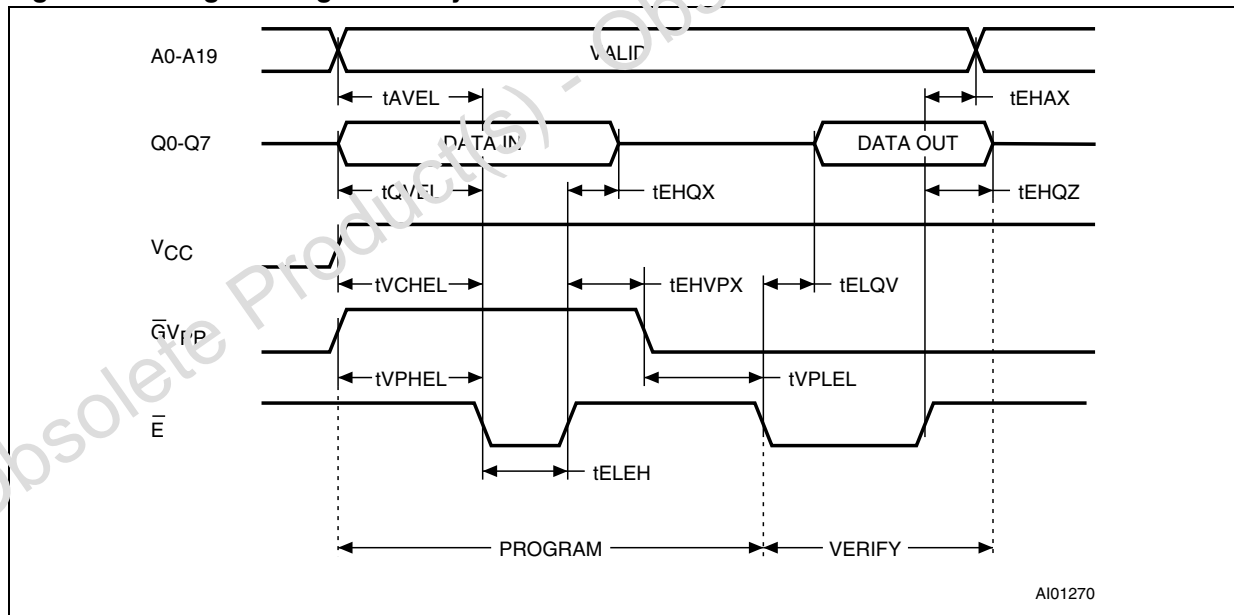


Table 11. Programming mode AC characteristics ⁽¹⁾

| Symbol | Alt | Parameter | Test condition | Min. | Max. | Unit |
|------------------|-----------|---|----------------|------|------|---------|
| t_{AVEL} | t_{AS} | Address valid to Chip Enable low | | 2 | | μs |
| t_{QVEL} | t_{DS} | Input valid to Chip Enable low | | 2 | | μs |
| t_{VCHEL} | t_{VCS} | V_{CC} high to Chip Enable low | | 2 | | μs |
| t_{VPHEL} | t_{OES} | V_{PP} high to Chip Enable low | | 2 | | μs |
| t_{VPLVPH} | t_{PRT} | V_{PP} rise time | | 50 | | ns |
| t_{ELEH} | t_{PW} | Chip Enable program pulse width (initial) | | 45 | 55 | μs |
| t_{EHQX} | t_{DH} | Chip Enable high to Input transition | | 2 | | μs |
| t_{EHVPX} | t_{OEH} | Chip Enable high to V_{PP} transition | | 2 | | μs |
| t_{VPLEL} | t_{VR} | V_{PP} low to Chip Enable low | | 2 | | μs |
| t_{ELQV} | t_{DV} | Chip Enable low to output valid | | | 1 | μs |
| $t_{EHQZ}^{(2)}$ | t_{DFP} | Chip Enable high to output Hi-Z | | 0 | 130 | ns |
| t_{EHAX} | t_{AH} | Chip Enable high to address transition | | 0 | | ns |

- V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously with or after V_{PP} .
- Sampled only, not 100% tested.

Figure 9. Programming and verify modes AC waveforms



5 Package mechanical data

5.1 32-pin ceramic frit-seal DIP, with round window (FDIP32WA)

Figure 10. FDIP32WA package outline

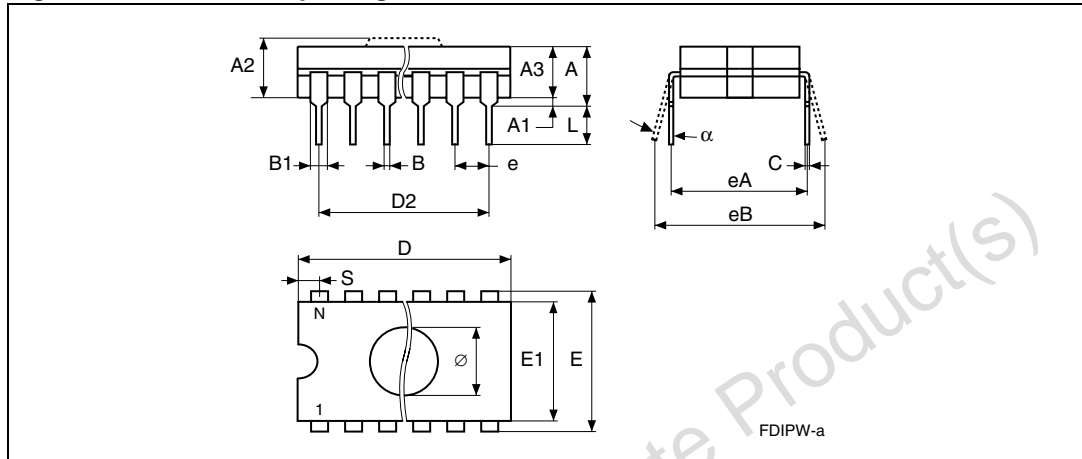


Table 12. FDIP32WA package mechanical data

| Symbol | millimeters | | | inches | | |
|--------|-------------|-------|-------|--------|-------|-------|
| | Min | Typ | Max | Min | Typ | Max |
| A | | | 5.72 | | | 0.225 |
| A1 | 0.51 | | 1.40 | 0.020 | | 0.055 |
| A2 | 3.91 | | 4.57 | 0.154 | | 0.180 |
| A3 | 3.03 | | 4.50 | 0.153 | | 0.177 |
| B | 0.41 | | 0.56 | 0.016 | | 0.022 |
| B1 | | 1.45 | | | 0.057 | |
| C | 0.23 | | 0.30 | 0.009 | | 0.012 |
| D | 41.73 | | 42.04 | 1.643 | | 1.655 |
| D2 | | 38.10 | | | 1.500 | |
| e | | 2.54 | | | 0.100 | |
| E | | 15.24 | | | 0.600 | |
| E1 | 13.06 | | 13.36 | 0.514 | | 0.526 |
| eA | | 14.99 | | | 0.590 | |
| eB | 16.18 | | 18.03 | 0.637 | | 0.710 |
| L | 3.18 | | 4.10 | 0.125 | | 0.161 |
| N | | 32 | | | 32 | |
| S | 1.52 | | 2.49 | 0.060 | | 0.098 |
| Ø | | 7.11 | | | 0.280 | |
| α | 4° | | 11° | 4° | | 11° |

5.2 32-pin plastic DIP, 600 mils width (PDIP32)

Figure 11. PDIP32 package outline

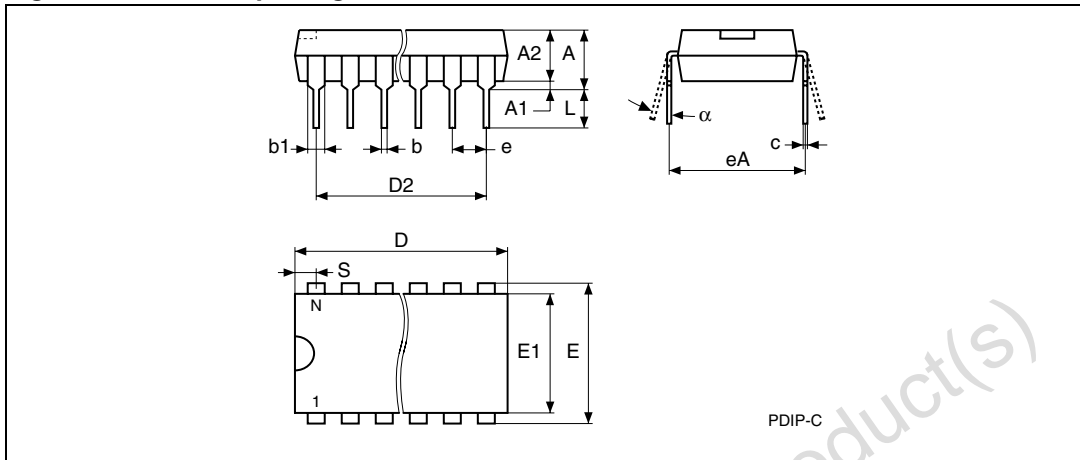


Table 13. PDIP32 package mechanical data

| Symbol | millimeters | | | inches | | |
|----------|-------------|-------|-------|--------|-------|-------|
| | Min | Typ | Max | Min | Typ | Max |
| A | | | 4.93 | | | 0.190 |
| A1 | 0.38 | | | 0.015 | | |
| A2 | | 3.81 | | | 0.150 | |
| b | 0.41 | | 0.53 | 0.016 | | 0.021 |
| b1 | 1.14 | | 1.65 | 0.045 | | 0.065 |
| c | 0.23 | | 0.38 | 0.009 | | 0.015 |
| D | 41.78 | | 42.29 | 1.645 | | 1.665 |
| D2 | | 38.10 | | | 1.500 | |
| eA | | 15.24 | | | 0.600 | |
| e | | 2.54 | | | 0.100 | |
| E | 15.24 | | 15.88 | 0.600 | | 0.625 |
| E1 | 13.46 | | 13.97 | 0.530 | | 0.550 |
| S | 1.65 | | 2.21 | 0.065 | | 0.087 |
| L | 3.05 | | 3.56 | 0.120 | | 0.140 |
| α | 0° | | 15° | 0° | | 15° |
| N | 32 | | | 32 | | |

5.3 32-lead rectangular plastic leaded chip carrier (PLCC32)

Figure 12. PLCC32 package outline

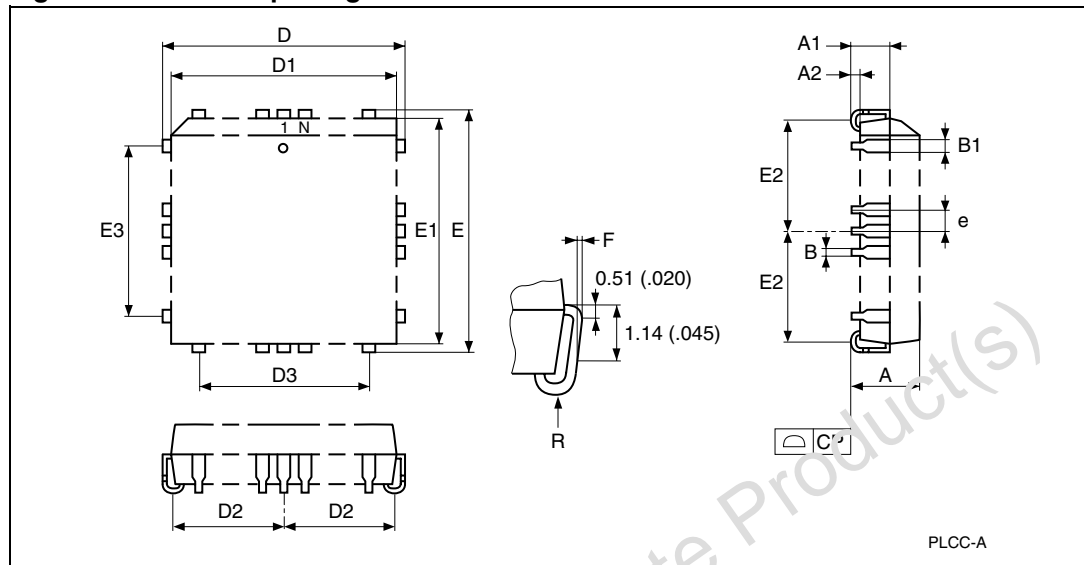


Table 14. PLCC32 package mechanical data

| Symbol | millimeters | | | inches | | |
|----------------|-------------|-------|-------|--------|-------|-------|
| | Min | Typ | Max | Min | Typ | Max |
| A | 3.18 | | 3.56 | 0.125 | | 0.140 |
| A1 | 1.53 | | 2.41 | 0.060 | | 0.095 |
| A2 | 0.38 | | – | 0.015 | | – |
| B | 0.33 | | 0.53 | 0.013 | | 0.021 |
| B1 | 0.66 | | 0.81 | 0.026 | | 0.032 |
| C _T | | | 0.10 | | | 0.004 |
| D | 12.32 | | 12.57 | 0.485 | | 0.495 |
| D1 | 11.35 | | 11.51 | 0.447 | | 0.453 |
| D2 | 4.78 | | 5.66 | 0.188 | | 0.223 |
| D3 | | 7.62 | | | 0.300 | |
| E | 14.86 | | 15.11 | 0.585 | | 0.595 |
| E1 | 13.89 | | 14.05 | 0.547 | | 0.553 |
| E2 | 6.05 | | 6.93 | 0.238 | | 0.273 |
| E3 | | 10.16 | | | 0.400 | |
| e | | 1.27 | | | 0.050 | |
| F | 0.00 | | 0.13 | 0.000 | | 0.005 |
| R | | 0.89 | | | 0.035 | |
| N | | 32 | | | 32 | |

6 Part numbering

Table 15. Ordering information scheme

| | | | | |
|---|---------|-----|---|---|
| Example: | M27C801 | -55 | K | 1 |
| Device type M27 | | | | |
| Supply voltage C = 5 V ±10% | | | | |
| Device function 801 = 8 Mbit (1Mb x 8) | | | | |
| Speed -55 ⁽¹⁾ = 55 ns -80 = 80 ns -90 = 90 ns -100 = 100 ns | | | | |
| Package F = FDIP32W B = PDIP32 K = PLCC32 | | | | |
| Temperature range 1 = 0 to 70 °C 6 = -40 to 85 °C | | | | |

¹. High Speed, see [DC and AC characteristics](#) section for further information.

For a list of available options (speed, package, etc...) or for further information on any aspect of this device, please contact the nearest STMicroelectronics sales office.

7 Revision history

Table 16. Document revision history

| Date | Revision | Changes |
|--------------|----------|--|
| 10-Sept-1998 | 1 | First Issue |
| 21-Mar-2000 | 2 | FDIP32W Package changed |
| 25-Sep-2000 | 3 | AN620 Reference removed |
| 12-Jul-2002 | 4 | 55ns speed class added PLCC32 Package mechanical drawing and data clarified |
| 12-Apr-2006 | 5 | Converted to new template. Added ECOPACK® information. Removed Tape & Reel Packing option. |
| 24-Sep-2007 | 6 | TSOP32 (N) package removed. 45 ns, 60 ns, 70 ns, 120 ns and 150 ns speed classes removed, 90 ns speed class added. |

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST's terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST'S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

UNLESS EXPRESSLY APPROVED IN WRITING BY AN AUTHORIZED ST REPRESENTATIVE, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS "AUTOMOTIVE GRADE" MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER'S OWN RISK.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2007 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com