

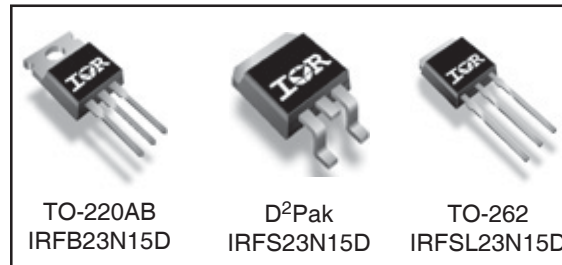
Applications

- High frequency DC-DC converters
- Lead-Free

V_{DSS}	R_{DS(on) max}	I_D
150V	0.090Ω	23A

Benefits

- Low Gate-to-Drain Charge to Reduce Switching Losses
- Fully Characterized Capacitance Including Effective C_{OSS} to Simplify Design, (See App. Note AN1001)
- Fully Characterized Avalanche Voltage and Current



Absolute Maximum Ratings

	Parameter	Max.	Units
I _D @ T _C = 25°C	Continuous Drain Current, V _{GS} @ 10V	23	A
I _D @ T _C = 100°C	Continuous Drain Current, V _{GS} @ 10V	17	
I _{DM}	Pulsed Drain Current ①	92	
P _D @ T _A = 25°C	Power Dissipation ②	3.8	W
P _D @ T _C = 25°C	Power Dissipation	136	
	Linear Derating Factor	0.9	W/°C
V _{GS}	Gate-to-Source Voltage	± 30	V
dv/dt	Peak Diode Recovery dv/dt ③	4.1	V/ns
T _J	Operating Junction and	-55 to + 175	°C
T _{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds		
	Mounting torque, 6-32 or M3 screw④	10 lbf•in (1.1N•m)	

Typical SMPS Topologies

- Telecom 48V input DC-DC Active Clamp Reset Forward Converter

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Static @ T_J = 25°C (unless otherwise specified)

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	Parameter	Min.	Typ.	Max.	Units	Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	150	—	—	V	V _{GS} = 0V, I _D = 250μA
ΔV _{(BR)DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	—	0.18	—	V/°C	Reference to 25°C, I _D = 1mA
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	—	0.090	Ω	V _{GS} = 10V, I _D = 14A ④
V _{GS(th)}	Gate Threshold Voltage	3.0	—	5.5	V	V _{DS} = V _{GS} , I _D = 250μA
I _{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	V _{DS} = 150V, V _{GS} = 0V
		—	—	250		V _{DS} = 120V, V _{GS} = 0V, T _J = 150°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V _{GS} = 30V
	Gate-to-Source Reverse Leakage	—	—	-100		V _{GS} = -30V

Dynamic @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
g _{fs}	Forward Transconductance	11	—	—	S	V _{DS} = 25V, I _D = 14A
Q _g	Total Gate Charge	—	37	56	nC	I _D = 14A V _{DS} = 120V V _{GS} = 10V, ④
Q _{gs}	Gate-to-Source Charge	—	9.6	14		
Q _{gd}	Gate-to-Drain ("Miller") Charge	—	19	29		
t _{d(on)}	Turn-On Delay Time	—	10	—	ns	V _{DD} = 75V I _D = 14A R _G = 5.1Ω V _{GS} = 10V ④
t _r	Rise Time	—	32	—		
t _{d(off)}	Turn-Off Delay Time	—	18	—		
t _f	Fall Time	—	8.4	—		
C _{iss}	Input Capacitance	—	1200	—	pF	V _{GS} = 0V V _{DS} = 25V f = 1.0MHz⑥
C _{oss}	Output Capacitance	—	260	—		
C _{rss}	Reverse Transfer Capacitance	—	65	—		
C _{oss}	Output Capacitance	—	1520	—		
C _{oss}	Output Capacitance	—	120	—		
C _{oss eff.}	Effective Output Capacitance	—	210	—		

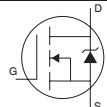
Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E _{AS}	Single Pulse Avalanche Energy②	—	260	mJ
I _{AR}	Avalanche Current①	—	14	A
E _{AR}	Repetitive Avalanche Energy①	—	13.6	mJ

Thermal Resistance

	Parameter	Typ.	Max.	Units
R _{θJC}	Junction-to-Case	—	1.1	°C/W
R _{θCS}	Case-to-Sink, Flat, Greased Surface ⑥	0.50	—	
R _{θJA}	Junction-to-Ambient⑥	—	62	
R _{θJA}	Junction-to-Ambient⑦	—	40	

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	—	23	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I _{SM}	Pulsed Source Current (Body Diode) ①	—	—	92		
V _{SD}	Diode Forward Voltage	—	—	1.3	V	T _J = 25°C, I _S = 14A, V _{GS} = 0V ④
t _{rr}	Reverse Recovery Time	—	150	220	ns	T _J = 25°C, I _F = 14A
Q _{rr}	Reverse Recovery Charge	—	0.8	1.2	μC	di/dt = 100A/μs ④
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)				

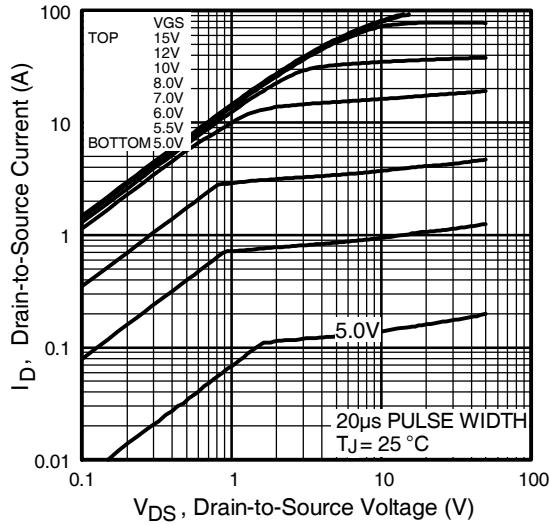


Fig 1. Typical Output Characteristics

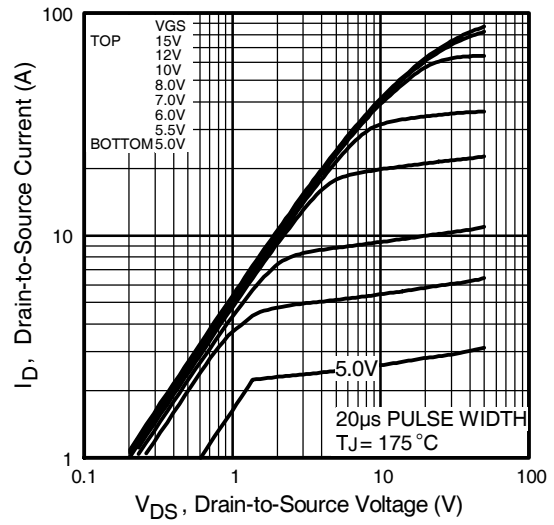


Fig 2. Typical Output Characteristics

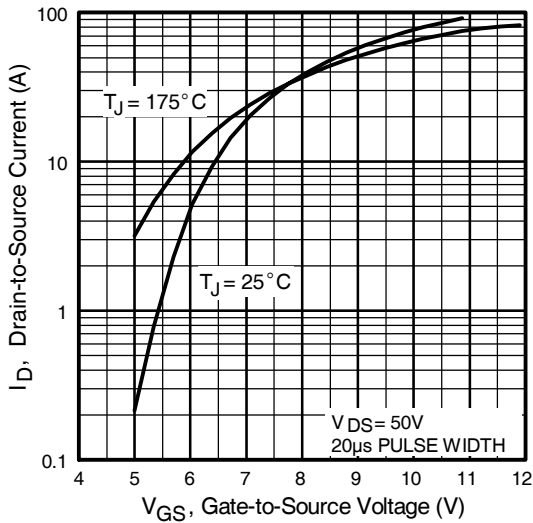


Fig 3. Typical Transfer Characteristics

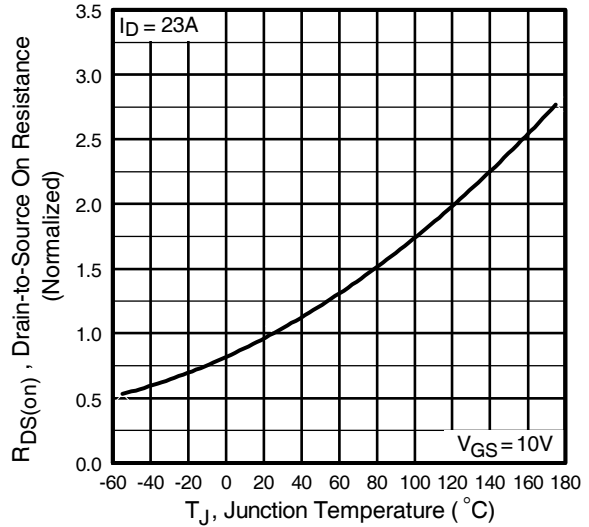


Fig 4. Normalized On-Resistance Vs. Temperature

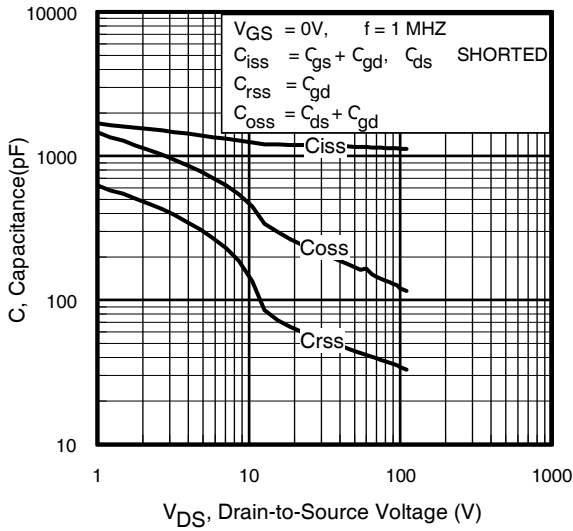


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

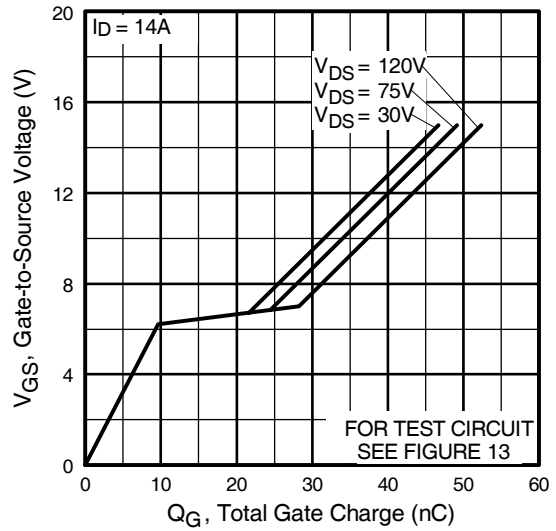


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

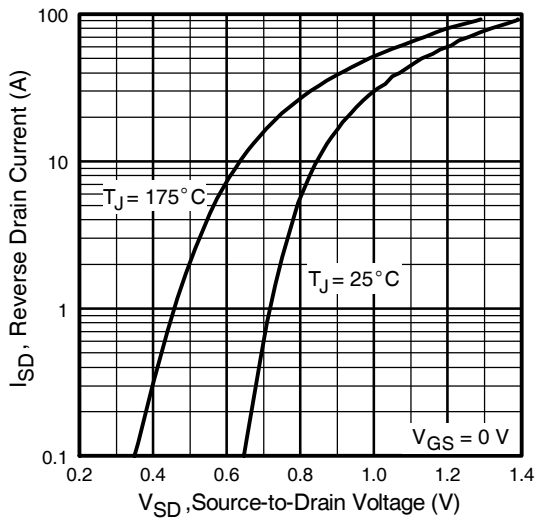


Fig 7. Typical Source-Drain Diode Forward Voltage

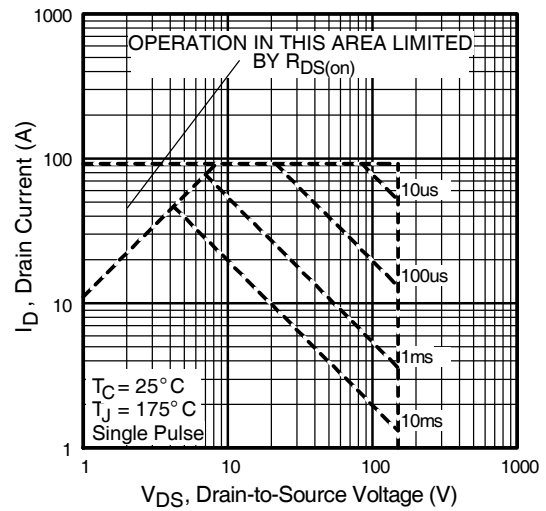


Fig 8. Maximum Safe Operating Area

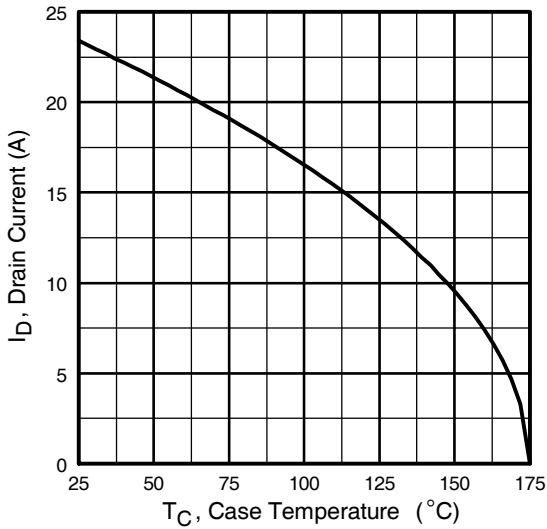


Fig 9. Maximum Drain Current Vs. Case Temperature



Fig 10a. Switching Time Test Circuit



Fig 10b. Switching Time Waveforms

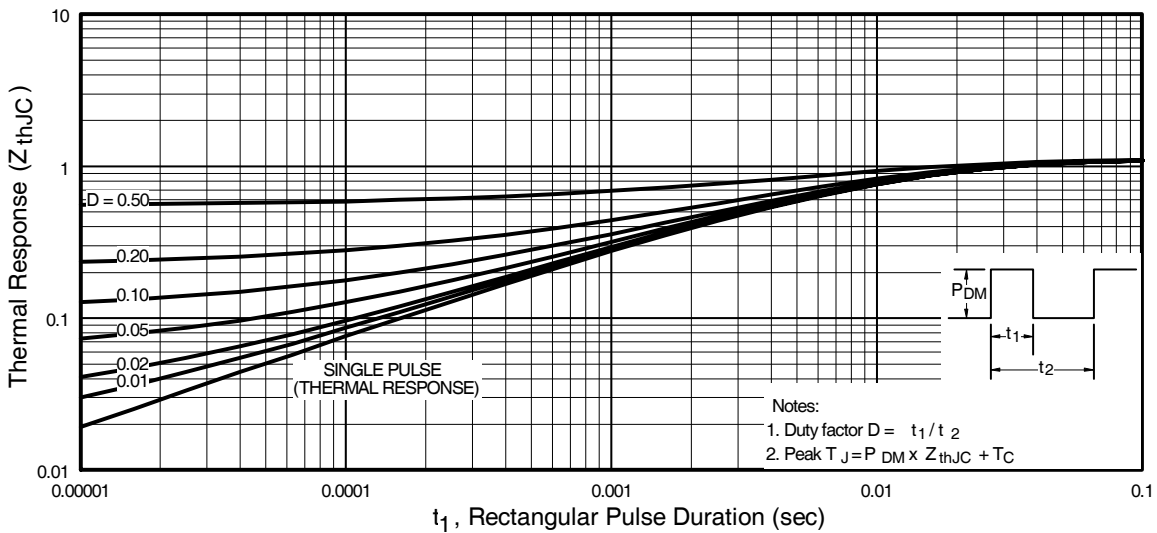


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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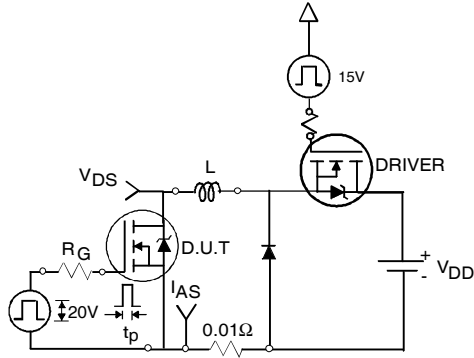


Fig 12a. Unclamped Inductive Test Circuit

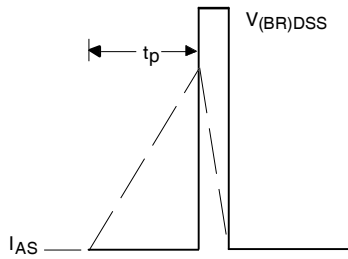


Fig 12b. Unclamped Inductive Waveforms

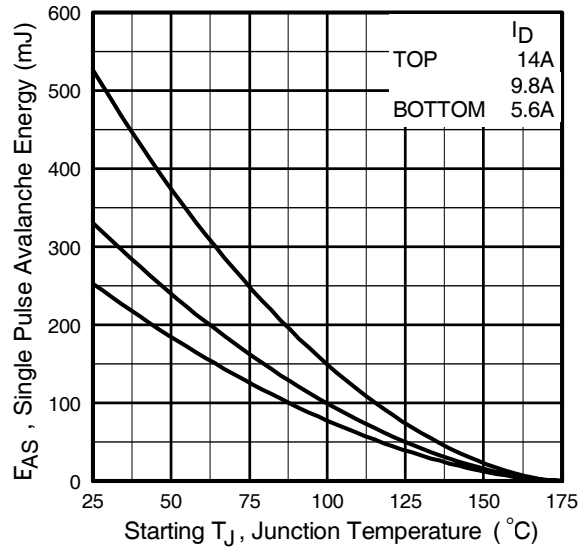


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

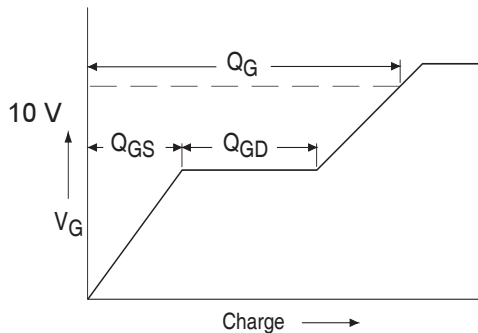


Fig 13a. Basic Gate Charge Waveform

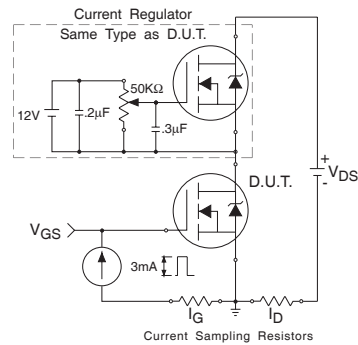
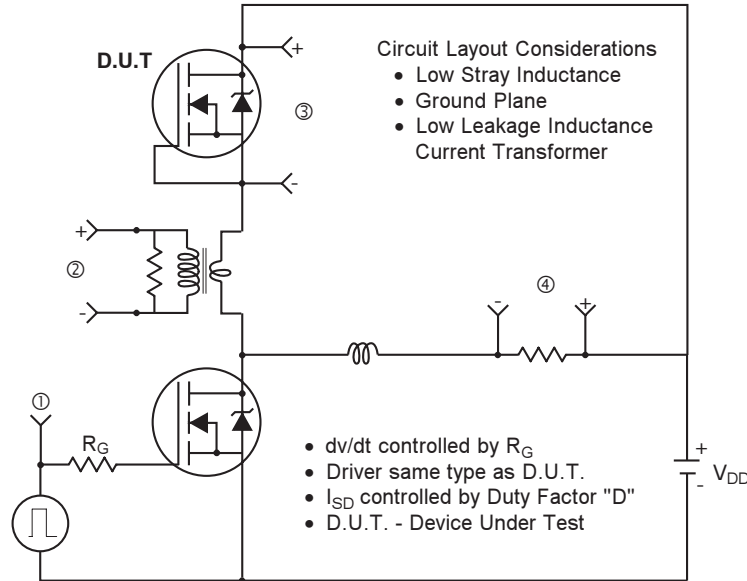


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* $V_{GS} = 5V$ for Logic Level Devices

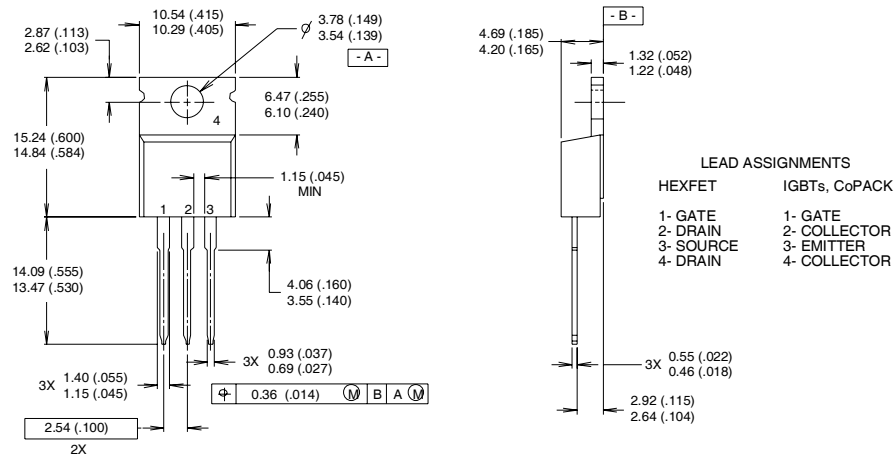
Fig 14. For N-Channel HEXFET® Power MOSFETs

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TO-220AB Package Outline

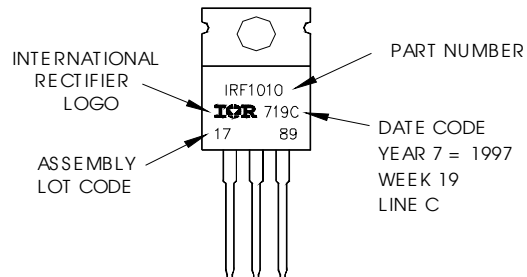
Dimensions are shown in millimeters (inches)



- NOTES:
- 1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
 - 2 CONTROLLING DIMENSION : INCH
 - 3 OUTLINE CONFORMS TO JEDEC OUTLINE TO-220AB.
 - 4 HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

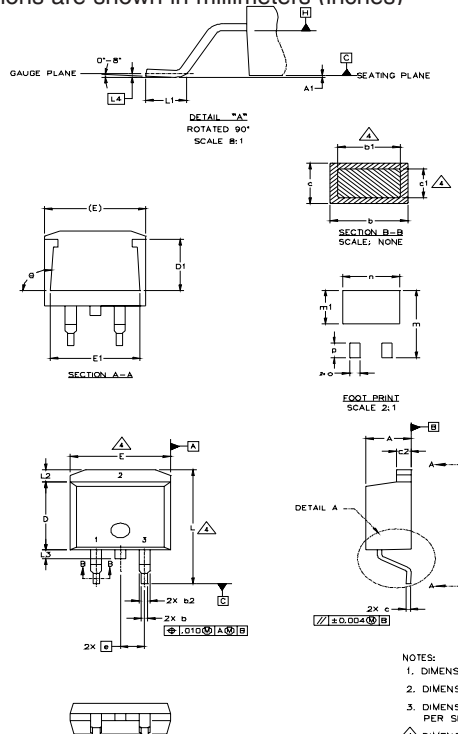
TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010
 LOT CODE 1789
 ASSEMBLED ON WW 19, 1997
 IN THE ASSEMBLY LINE "C"
Note: "P" in assembly line position indicates "Lead-Free"



D²Pak Package Outline

Dimensions are shown in millimeters (inches)



SYMBOL	DIMENSIONS				UNIT	
	MILLIMETERS		INCHES			
	MIN.	MAX.	MIN.	MAX.		
A	4.06	4.83	.160	.190	4	
A1		0.127	.005	4		
b	0.51	0.99	.020			.039
b1	0.51	0.89	.020			.035
b2	1.14	1.40	.045		.055	3
c	0.43	0.63	.017	.025		
c1	0.38	0.74	.015	.029		
c2	1.14	1.40	.045	.055		
D	8.51	9.65	.335	.380	3	
D1	5.33		.210			
E	9.65	10.67	.380	.420		
E1	6.22		.245		3	
e	2.54 BSC		.100 BSC			
L	14.61	15.88	.575	.625		
L1	1.78	2.79	.070	.110		
L2		1.65		.065	3	
L3	1.27	1.78	.050	.070		
L4	0.25 BSC		.010 BSC			
m	17.78		.700		3	
m1	8.89		.350			
n	11.43		.450			
o	2.08		.082			
p	3.81		.150		3	
θ	90°	93°	90°	93°		

LEAD ASSIGNMENTS

HEXFET	IGBTs_CoPACK	DIODES
1.- GATE	1.- GATE	1.- ANODE *
2.- DRAIN	2.- COLLECTOR	2.- CATHODE
3.- SOURCE	3.- EMITTER	3.- ANODE

* PART DEPENDENT.

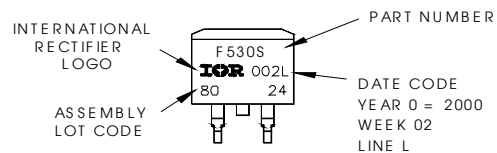
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES]
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
4. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
5. CONTROLLING DIMENSION: INCH.

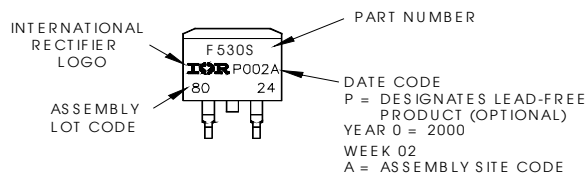
D²Pak Part Marking Information (Lead-Free)

EXAMPLE: THIS IS AN IRF530S WITH
LOT CODE 8024
ASSEMBLED ON WW 02, 2000
IN THE ASSEMBLY LINE "L"

Note: "P" in assembly line
position indicates "Lead-Free"



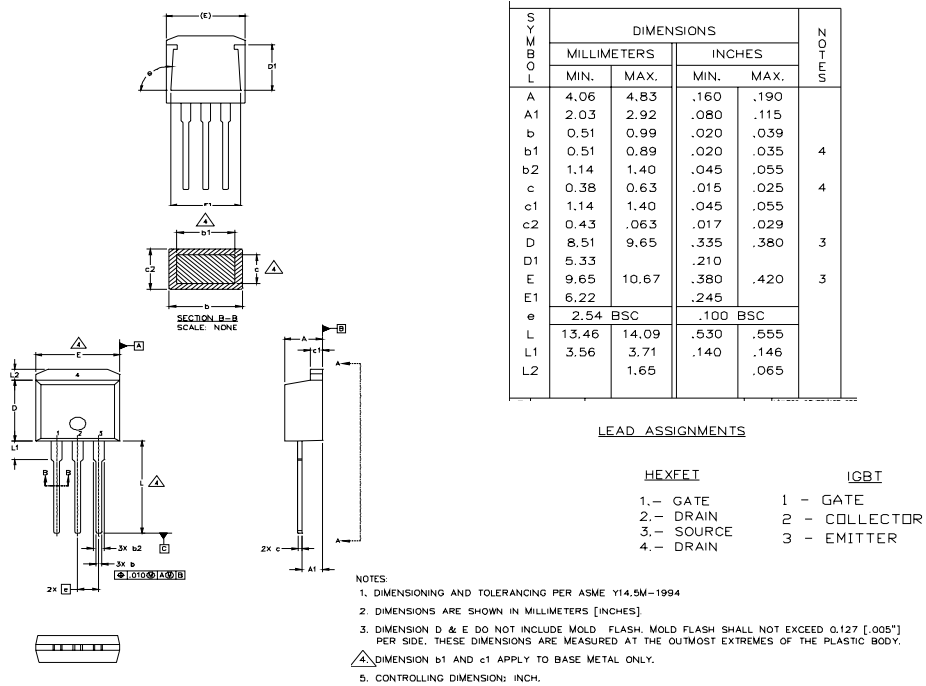
OR



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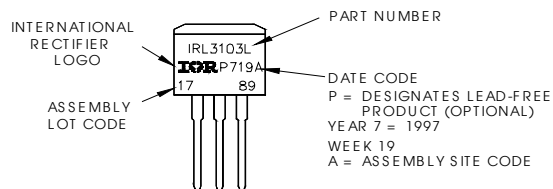
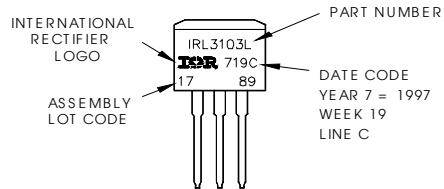
TO-262 Package Outline



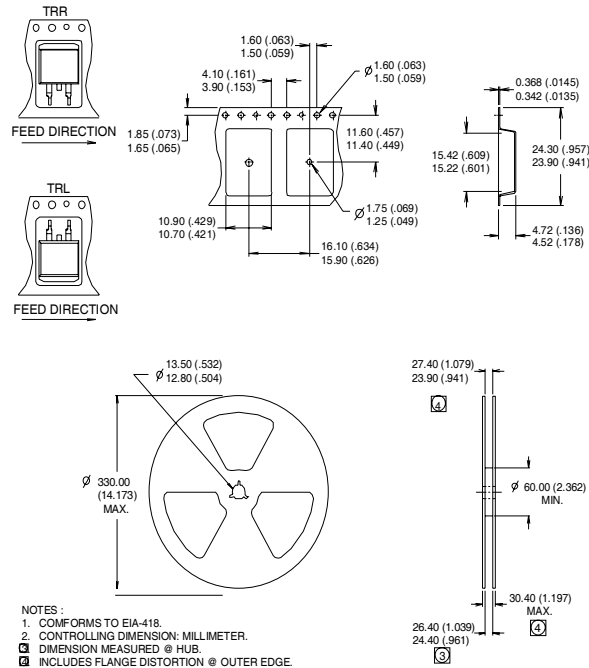
TO-262 Part Marking Information

EXAMPLE: THIS IS AN IRL3103L
 LOT CODE 1789
 ASSEMBLED ON WW 19, 1997
 IN THE ASSEMBLY LINE "C"
 Note: "P" in assembly line position indicates "Lead-Free"

OR



D²Pak Tape & Reel Information



Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting $T_J = 25^\circ\text{C}$, $L = 2.7\text{mH}$
 $R_G = 25\Omega$, $I_{AS} = 14\text{A}$.
- ③ $I_{SD} \leq 14\text{A}$, $di/dt \leq 240\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$,
 $T_J \leq 175^\circ\text{C}$
- ④ Pulse width $\leq 300\mu\text{s}$; duty cycle $\leq 2\%$.
- ⑤ C_{OSS} eff. is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 80% V_{DSS}
- ⑥ This is only applied to TO-220AB package
- ⑦ This is applied to D²Pak, when mounted on 1" square PCB (FR-4 or G-10 Material).
 For recommended footprint and soldering techniques refer to application note #AN-994.

Data and specifications subject to change without notice.

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 TAC Fax: (310) 252-7903

Visit us at www.irf.com for sales contact information.07/04

Note: For the most current drawings please refer to the IR website at:
<http://www.irf.com/package/>