54/74197
54LS/74LS197
PRESETTABLE BINARY COUNTERS

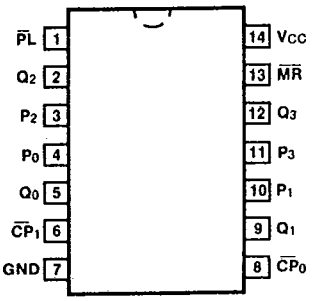
DESCRIPTION — The '197 ripple counter contains divide-by-two and divide-by-eight sections which can be combined to form a modulo-16 binary counter. State changes are initiated by the falling edge of the clock. The '197 has a Master Reset ($\overline{MR}$) input which overrides all other inputs and asynchronously forces all outputs LOW. A Parallel Load input ($\overline{PL}$) overrides clocked operations and asynchronously loads the data on the Parallel Data inputs (P_n) into the flip-flops.This preset feature makes the circuit usable as a programmable counter. The circuit can also be used as a 4-bit latch, loading data from the Parallel Data inputs when $\overline{PL}$ is LOW and storing the data when $\overline{PL}$ is HIGH. For detail specifications and functional description, please refer to the '196 data sheet.

- **HIGH COUNTING RATES — TYPICALLY 70 MHz**
- **ASYNCHRONOUS PRESET**
- **ASYNCHRONOUS MASTER RESET**

ORDERING CODE: See Section 9

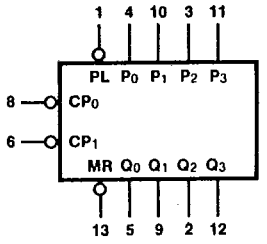
PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74197PC, 74LS197PC		9A
Ceramic DIP (D)	A	74197DC, 74LS197DC	54197DM, 54LS197DM	6A
Flatpak (F)	A	74197FC, 74LS197FC	54197FM, 54LS197FM	3I

CONNECTION DIAGRAM
PINOUT A



4

LOGIC SYMBOL



V_{CC} = Pin 14
GND = Pin 7

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
$\overline{CP_0}$	÷2 Section Clock Input (Active Falling Edge)	2.0/3.0	1.0/1.5
$\overline{CP_1}$	÷8 Section Clock Input (Active Falling Edge)	2.0/2.0	1.0/0.81
$\overline{MR}$	Asynchronous Master Reset Input (Active LOW)	2.0/2.0	1.0/0.5
$P_0 - P_3$	Parallel Data Inputs	1.0/1.0	0.5/0.25
$\overline{PL}$	Asynchronous Parallel Load Input (Active LOW)	1.0/1.0	0.5/0.25
Q_0	÷2 Section Output*	20/10	10/5.0 (2.5)
$Q_1 - Q_3$	÷8 Section Outputs	20/10	10/5.0 (2.5)

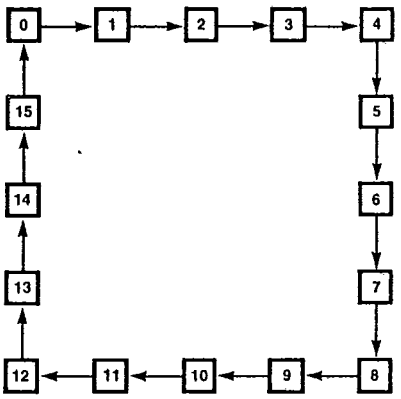
*Q_0 output is guaranteed to drive the full rated fan-out plus the $\overline{CP_1}$ input.

MODE SELECTION TABLE

INPUTS			RESPONSE
$\overline{MR}$	$\overline{PL}$	$\overline{CP}$	
L	X	X	Q_n forced LOW
H	L	X	$P_n \rightarrow Q_n$
H	H	⌐	Count Up

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

÷ 16 STATE DIAGRAM



LOGIC DIAGRAM