Integrated Device Technology, Inc.

FAST CMOS SYNCHRONOUS PRESETTABLE BINARY COUNTERS

IDT54/74FCT161/A/C
IDT54/74FCT163/A/C

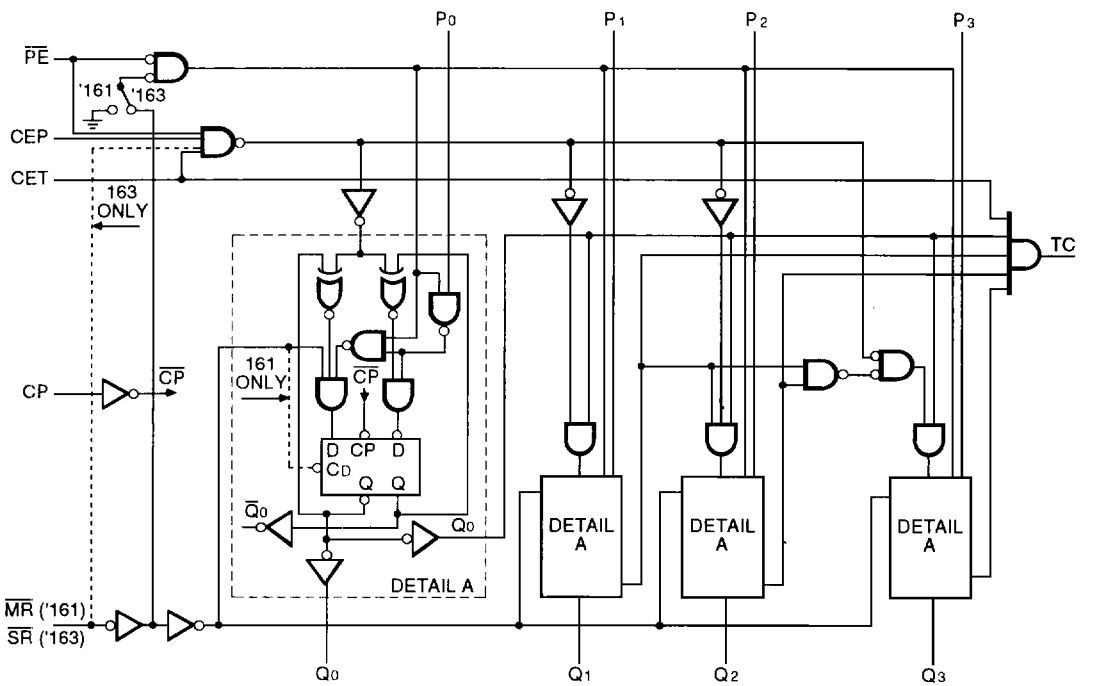
FEATURES:

- IDT54/74FCT161/163 equivalent to FAST™ speed
- **IDT54/74FCT161A/163A 35% faster than FAST**
- **IDT54/74FCT161A/163C 45% faster than FAST**
- Equivalent to FAST output drive over full temperature and voltage supply extremes
- IOL = 48mA (commercial), 32mA (military)
- CMOS power levels (1mW typ. static)
- CMOS output level compatible
- Substantially lower input current levels than FAST (5μA max.)
- JEDEC standard pinout for DIP and LCC
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT54/74FCT161/163, IDT54/74FCT161A/163A and IDT54/74FCT161C/163C are high-speed synchronous modulo-16 binary counters built using an advanced dual metal CMOS technology. They are synchronously presettable for application in programmable dividers and have two types of count enable inputs plus a terminal count output for versatility in forming synchronous multistage counters. The IDT54/74FCT161/A/C have asynchronous Master Reset inputs that override all other inputs and force the outputs LOW. The IDT54/74FCT163/A/C have Synchronous Reset inputs that override counting and parallel loading and allow the outputs to be simultaneously reset on the rising edge of the clock.

FUNCTIONAL BLOCK DIAGRAMS



2612 drw 01

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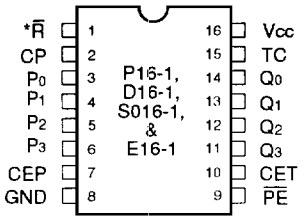
FAST is a trademark of National Semiconductor Co.

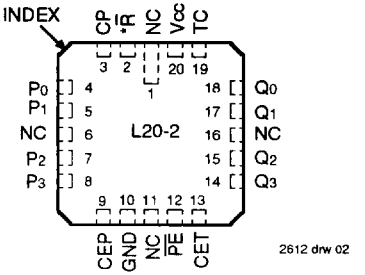
PIN CONFIGURATIONS

IDT54/74FCT861 10-BIT TRANSCEIVERS



DIP/SOIC/CERPACK
TOP VIEW

*SR for '163
*MR for '161



2612 drw 02

LCC
TOP VIEW
*SR FOR '163

PIN DESCRIPTION

Pin Names	Description
CEP	Count Enable Parallel Input
CET	Count Enable Trickle Input
CP	Clock Pulse Input (Active Rising Edge)
$\overline{MR}$ ('161)	Asynchronous Master Reset Input (Active LOW)
$\overline{SR}$ ('163)	Synchronous Reset Input (Active LOW)
P0-3	Parallel Data Inputs
$\overline{PE}$	Parallel Enable Input (Active LOW)
Q0-3	Flip-Flop Outputs
TC	Terminal Count Output

2612 tbl 05

FUNCTION TABLE[2]

$\overline{SR}$[1]	$\overline{PE}$	CET	CEP	Action on the Rising Clock Edge(s)
L	X	X	X	Reset (Clear)
H	L	X	X	Load (Pn→Qn)
H	H	H	H	Count (Increment)
H	H	L	X	No Change (Hold)
H	H	X	L	No Change (Hold)

NOTES:
1. For FCT163/163A/163C only.
2. H = HIGH Voltage Level, L = LOW Voltage Level, X = Don't Care.

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ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to V_{CC}	–0.5 to V_{CC}	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES: 2612 tbl 01

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
2. Inputs and V_{CC} terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2612 tbl 02

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: V_{LC} = 0.2V; V_{HC} = V_{CC} – 0.2V
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions(1)			Min.	Typ.(2)	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		COM'L(5)	2.0V	—	—	V
				MIL	3.0V	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level			—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = V_{CC}		—	—	5	µA
			V_I = 2.7V		—	—	5(4)	
I_{IL}	Input LOW Current		V_I = 0.5V		—	—	–5(4)	
			V_I = GND		—	—	–5	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA			—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.(3), V_O = GND			–60	–120	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = –32µA			V_{HC}	V_{CC}	—	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –300µA		V_{HC}	V_{CC}	—	
			I_{OH} = –12mA MIL.		2.4	4.3	—	
			I_{OH} = –15mA COM'L.		2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA			—	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA		—	GND	V_{LC}(4)	
			I_{OL} = 32mA MIL.		—	0.3	0.5	
			I_{OL} = 48mA COM'L.		—	0.3	0.5	

NOTES: 2612 tbl 03

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.
5. Clock pin requires a minimum V_{IH} of 2.7V.

POWER SUPPLY CHARACTERISTICS V_{LC} = 0.2V, V_{HC} = V_{CC} – 0.2V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$		—	0.2	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max., V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max., Outputs Open Load Mode CEP = CET = $\overline{PE}$ = GND $\overline{MR}$ or $\overline{SR}$ = V_{CC} One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open Load Mode f_{CP} = 10MHz 50% Duty Cycle CEP = CET = $\overline{PE}$ = GND $\overline{MR}$ or $\overline{SR}$ = V_{CC} One Bit Toggling at f_i = 5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	1.7	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	—	2.2	6.0	
		V_{CC} = Max., Outputs Open Load Mode f_{CP} = 10MHz 50% Duty Cycle CEP = CET = $\overline{PE}$ = GND $\overline{MR}$ or $\overline{SR}$ = V_{CC} Four Bits Toggling at f_i = 5MHz 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	4.0	7.8[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	5.2	12.8[5]	

2612 tbl 04

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD}(f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

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SWITCHING CHARACTERISTICS OVER OPERATING RANGE

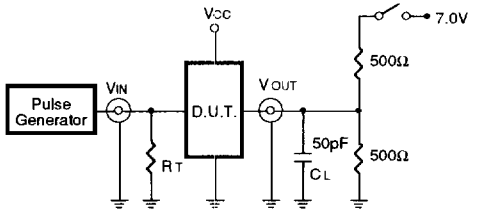
Symbol	Parameter	Condition[1]	IDT54/74FCT161/163				IDT54/74FCT161A/163A				IDT54/74FCT161C/163C				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay CP to Qn ($\overline{PE}$ Input HIGH)	CL = 50pF RL = 500Ω	2.0	11.0	2.0	11.5	2.0	7.2	2.0	7.5	2.0	5.8	2.0	6.3	ns
tPLH tPHL	Propagation Delay CP to Qn ($\overline{PE}$ Input LOW)		2.0	9.5	2.0	10.0	2.0	6.2	2.0	6.5	2.0	5.8	2.0	6.3	ns
tPLH tPHL	Propagation Delay CP to TC		2.0	15.0	2.0	16.5	2.0	9.8	2.0	10.8	2.0	7.4	2.0	8.3	ns
tPLH tPHL	Propagation Delay CET to TC		1.5	8.5	1.5	9.0	1.5	5.5	1.5	5.9	1.5	5.2	1.5	5.6	ns
tPHL	Propagation Delay $\overline{MR}$ to Qn ('161)		2.0	13.0	2.0	14.0	2.0	8.5	2.0	9.1	2.0	6.0	2.0	6.6	ns
tPHL	Propagation Delay $\overline{MR}$ to TC ('161)		2.0	11.5	2.0	12.5	2.0	7.5	2.0	8.2	2.0	7.0	2.0	7.7	ns
tSU	Set-up Time, HIGH or LOW Pn to CP		5.0	—	5.5	—	4.0	—	4.5	—	4.0	—	4.5	—	ns
tH	Hold Time, HIGH or LOW Pn to CP		1.5	—	2.0	—	1.5	—	2.0	—	1.5	—	2.0	—	ns
tSU	Set-up Time, HIGH or LOW $\overline{PE}$ or $\overline{SR}$ to CP		11.5	—	13.5	—	9.5	—	11.5	—	9.5	—	11.5	—	ns
tH	Hold Time, HIGH or LOW $\overline{PE}$ or $\overline{SR}$ to CP		1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
tSU	Set-up Time, HIGH or LOW CEP or CET to CP		11.5	—	13.0	—	9.5	—	11.0	—	9.5	—	11.0	—	ns
tH	Hold Time, HIGH or LOW CEP or CET to CP		0	—	0	—	0	—	0	—	0	—	0	—	ns
tW	Clock Pulse Width (Load) HIGH or LOW		5.0	—	5.0	—	4.0[3]	—	4.0[3]	—	4.0[3]	—	4.0[3]	—	ns
tW	Clock Pulse Width (Count) HIGH or LOW		7.0	—	8.0	—	6.0	—	7.0	—	6.0	—	7.0	—	ns
tW	$\overline{MR}$ Pulse Width, LOW ('161)		5.0	—	5.0	—	4.0[3]	—	4.0[3]	—	4.0[3]	—	4.0[3]	—	ns
tREM	Recovery Time $\overline{MR}$ to CP ('161)		6.0	—	6.0	—	5.0	—	5.0	—	5.0	—	5.0	—	ns

NOTES:
1. See test circuits and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not tested.

2612 tbl 07

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



SWITCH POSITION

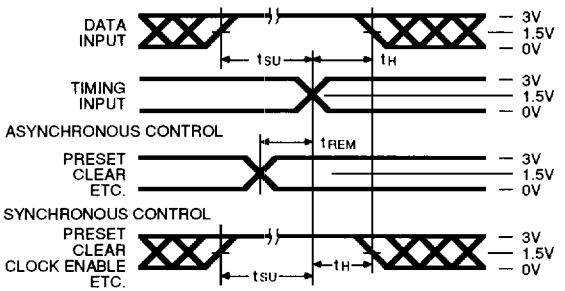
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

2612 tbl 08

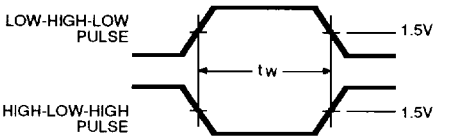
DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



PULSE WIDTH



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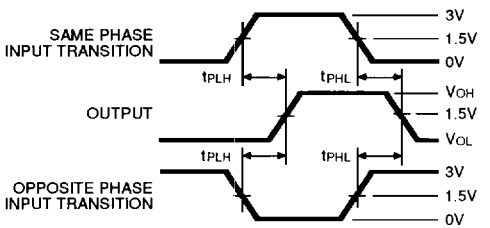
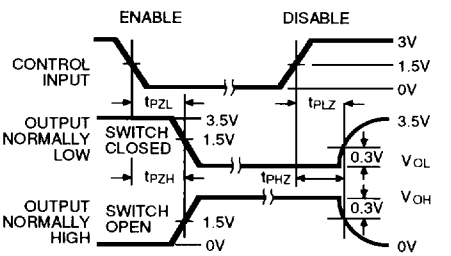


ENABLE AND DISABLE TIMES



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NOTES

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; Z_O ≤ 50Ω; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

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ORDERING INFORMATION