National Semiconductor

93L34
8-Bit Addressable Latch

General Description

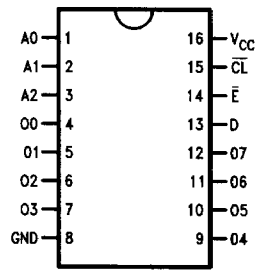
The 93L34 is an 8-bit addressable latch designed for general purpose storage applications in digital systems. It is a multifunctional device capable of storing single line data in eight addressable latches, and being a one-of-eight decoder and demultiplexer with active level HIGH outputs. The device also incorporates an active LOW common clear for resetting all latches, as well as, an active LOW enable.

Features

- Serial to parallel capability
- Eight bits of storage with output of each bit available
- Random (addressable) data entry
- Active high demultiplexing or decoding capability
- Easily expandable
- Common conditional clear

Connection Diagram

Dual-In-Line Package



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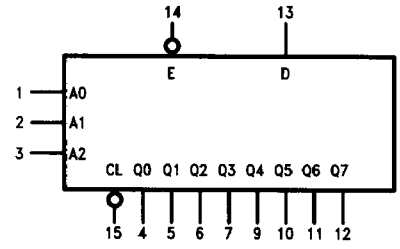
Order Number 93L34DMQB or 93L34FMQB
See NS Package Number J16A or W16A

Logic Symbol



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V_{CC} = Pin 16
GND = Pin 8

Pin Names	Description
A0–A3	Address Inputs
D	Data Input
$\overline{E}$	Enable Input (Active LOW)
$\overline{CL}$	Clear Input (Active LOW)
Q0–Q7	Parallel Latch Outputs

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
Military	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	93L34 (Mil)			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.7	V
I_{OH}	High Level Output Voltage			−400	μA
I_{OL}	Low Level Output Current			4.8	mA
T_A	Free Air Operating Temperature	−55		125	°C
t_s (H)	Setup Time HIGH, D to $\overline{E}$	45			ns
t_h (H)	Hold Time HIGH, D to $\overline{E}$	−5			ns
t_s (L)	Setup Time LOW, D to $\overline{E}$	45			ns
t_h (L)	Hold Time LOW, D to $\overline{E}$	−7			ns
t_s (H) t_s (L)	Setup Time HIGH or LOW A_n to $\overline{E}$	10 10			ns
t_w (L)	$\overline{E}$ Pulse Width LOW	26			ns
t_w (L)	$\overline{CL}$ Pulse Width LOW	35			ns

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −10 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max				0.3	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V	Inputs			20	μA
			$\overline{E}$			30	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.3V	Inputs			−0.4	mA
			$\overline{E}$			−0.6	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)		−2.5		−25	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 3)				21	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs open and all inputs grounded.

Switching Characteristics $V_{CC} = +5.0V$, $T_A = +25°C$ (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	$C_L = 15$ pF		Units
		Min	Max	
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to Q_n		45 42	ns
t_{PLH} t_{PHL}	Propagation Delay D to Q_n		65 45	ns
t_{PLH} t_{PHL}	Propagation Delay A_n to Q_n		66 66	ns
t_{PHL}	Propagation Delay $\overline{CL}$ to Q_n		55	ns

Functional Description

The 93L34 has four modes of operation which are shown in the Mode Select Table. In the addressable latch mode, data on the data line (D) is written into the addressed latch. The addressed latch will follow the Data input with all non-addressed latches remaining in their previous states. In the memory mode, all latches remain in their previous state and are unaffected by the data or address inputs. To eliminate the possibility of entering erroneous data into the latches, the Enable should be held HIGH while the Address lines are changing. In the 1-of-8 decoding or demultiplexing mode, the addressed output will follow the state of the D input with all other outputs in the LOW state. In the clear mode all outputs are LOW and unaffected by the address and data inputs. When operating the 93L34 as an addressable latch, changing more than one bit of the address could impose a transient wrong address. Therefore, this should only be done while in the memory mode.

Mode Select Table

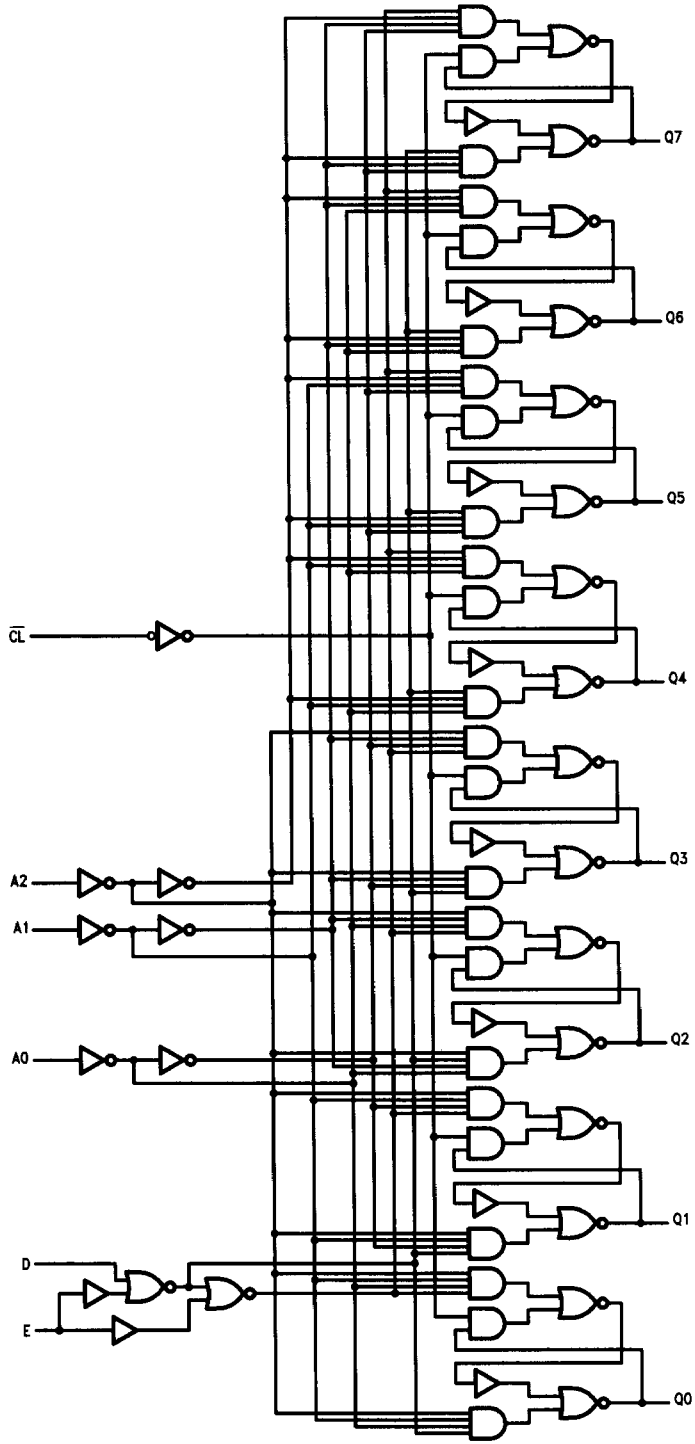
$\overline{E}$	$\overline{CL}$	Mode
L	H	Addressable Latch
H	H	Memory
L	L	Active HIGH 8-Channel Demultiplexer
H	L	Clear

Truth Table

Inputs					Outputs								Mode
$\overline{CL}$	$\overline{E}$	A0	A1	A2	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7	
L	H	X	X	X	L	L	L	L	L	L	L	L	Clear
L	L	L	L	L	D	L	L	L	L	L	L	L	Demultiplex
L	L	H	L	L	L	D	L	L	L	L	L	L	
L	L	L	H	L	L	L	D	L	L	L	L	L	
•	•	•	•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	•	•	•	
L	L	H	H	H	L	L	L	L	L	L	L	L	
H	H	X	X	X	Qt−1	Qt−1	Qt−1	Qt−1	Qt−1	Qt−1	Qt−1	Qt−1	Memory
H	L	L	L	L	D	Qt−1	Qt−1	Qt−1	Qt−1	Qt−1	Qt−1	Qt−1	Addressable
H	L	H	L	L	Qt−1	D	Qt−1	Qt−1	Qt−1	Qt−1	Qt−1	Qt−1	Latch
H	L	L	H	L	Qt−1	Qt−1	D	Qt−1	Qt−1	Qt−1	Qt−1	Qt−1	
•	•	•	•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	•	•	•	
H	L	H	H	H	Qt−1	Qt−1	Qt−1	Qt−1	Qt−1	Qt−1	Qt−1	D	

H = HIGH Voltage Level L = LOW Voltage Level X = Immaterial Qt−1 = Previous Output State

Logic Diagram



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