

FAIRCHILD DIGITAL

CMOS

DECODERS/DEMULTIPLEXERS (Cont'd)

Item	Function	DEVICE NO.	Address Inputs	Active LOW Enable	Output Configuration	Select Delay ns (Typ) V _{DD} = 10V	Enable Delay ns (Typ) V _{DD} = 10V	Logic/Connection Diagram	Package(s)
1	8-Channel Demultiplexer	4051B	3	1	H	125	105	C65	4L,6B,9B
2	BCD-to-7-Segment Latch/Decoder/Dvr	4511B	4	1	H	90	98	C111	4L,6B,9B
3	BCD-to-7-Segment Latch/Decoder/Dvr for Liquid Crystals	4543B	4	—	H or L	200	200	C112	4L,6B,9B
4	BCD-to-7-Segment Latch/Decoder/Dvr w/Ripple Blanking	4734B	4	1	H	90	98	C114	7D,9M

COUNTERS

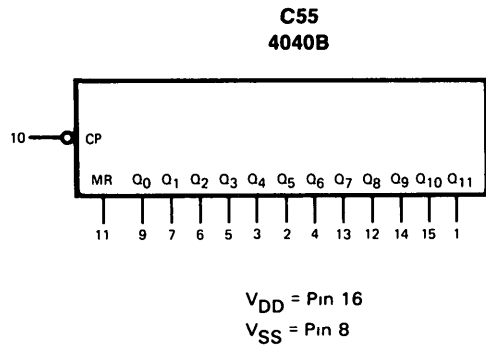
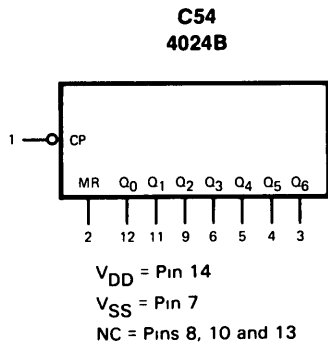
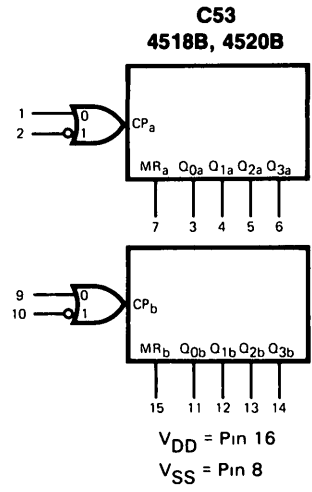
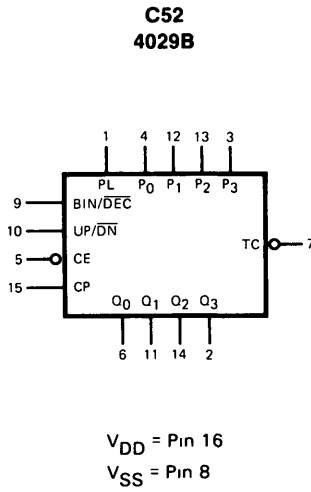
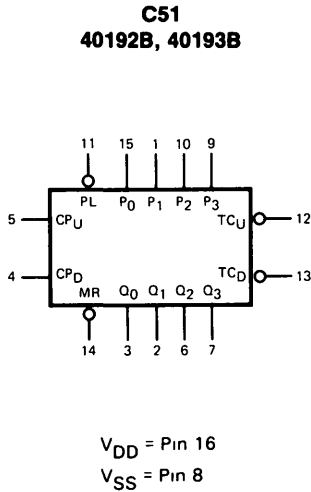
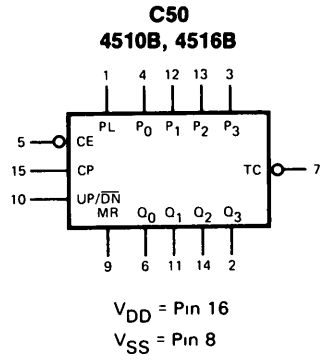
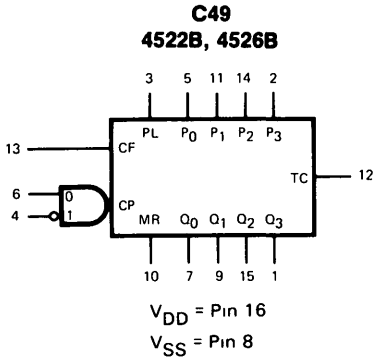
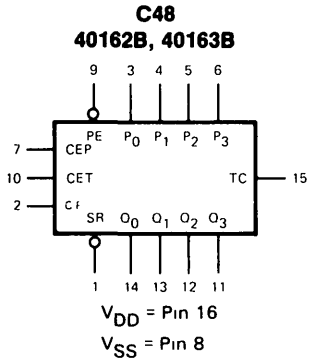
Item	Function	DEVICE NO.	Modulo	Parallel Load ⁽¹⁾	Clock Transition	Max Clock Rate MHz (Typ) V _{DD} = 10V	Clock to Q Output Delay ns (Typ) V _{DD} = 10V	Logic/Connection Diagram	Package(s)
5	4-Bit Sync Count Up	40160B	Decade	S	L→H	12	55	C47	4L,6B,9B
6	4-Bit Sync Count Up	40161B	Binary	S	L→H	12	55	C47	4L,6B,9B
7	4-Bit Sync Count Up	40162B	Decade	S	L→H	12	55	C48	4L,6B,9B
8	4-Bit Sync Count Up	40163B	Binary	S	L→H	12	55	C48	4L,6B,9B
9	4-Bit Sync Count Down	4522B ⁽²⁾	Decade	A	L→H or H→L	10	95	C49	4L,6B,9B
10	4-Bit Sync Count Down	4526B ⁽²⁾	Binary	A	L→H or H→L	10	95	C49	4L,6B,9B
11	4-Bit Sync Count Up/Down	4510B	Decade	A	L→H	12	62	C50	4L,6B,9B
12	4-Bit Sync Count Up/Down	4516B	Binary	A	L→H	12	62	C50	4L,6B,9B
13	4-Bit Sync Count Up/Down	40192B	Decade	A	L→H	80	105	C51	4L,6B,9B

1 A = Asynchronous, S = Synchronous

2 To be announced

FAIRCHILD LOGIC/CONNECTION DIAGRAMS

DIGITAL-CMOS



NOTE The Flatpak versions have the same pinouts (Connection Diagram) as the Dual In-Line Packages