CREE Wolfspeed

V_{DS}	1200 V
I_{DS}	530 A

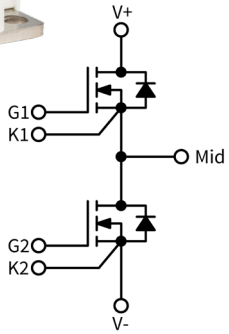
CAB530M12BM3

1200 V, 530 A All-Silicon Carbide Half-Bridge Module

Technical Features

- Industry Standard 62mm Footprint
- Ultra Low Loss, High-Frequency Operation
- Zero Turn-off Tail Current from MOSFET
- Normally-off, Fail-safe Device Operation
- Copper Baseplate and Aluminum Nitride Insulator

Package 61.4 mm X 106.4 mm X 30 mm



Applications

- Railway & Traction
- EV Charging Infrastructure
- Industrial Automation & Testing
- High-Frequency Power Supplies
- Renewable Energy Systems & Grid-Tied Inverters
- Active Front Ends & AC Inverters

System Benefits

- Lightweight, Compact Form-Factor with 62mm-Format Enables System Retrofit
- Increased System Efficiency due to Low Switching & Conduction Losses of SiC

Maximum Parameters (Validated by Design)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
$V_{DS\,max}$	Drain-Source Voltage			1200	V		
$V_{GS\,max}$	Gate-Source Voltage, Maximum Value	-8		+19		Transient, <100 ns	Fig. 32
$V_{GS\,op}$	Gate-Source Voltage, Recommended Op. Value	-4		+15		Static	
I_{DS}	DC Continuous Drain Current		719		A	V_{GS} = 15 V, T_C = 25 °C, T_{VJ} ≤ 175 °C	Fig. 20
			541			V_{GS} = 15 V, T_C = 90 °C, T_{VJ} ≤ 175 °C	
I_{SD}	DC Source-Drain Current		719			V_{GS} = 15 V, T_C = 25 °C, T_{VJ} ≤ 175 °C	
$I_{SD\,BD}$	DC Source-Drain Current (Body Diode)		442			V_{GS} = -4 V, T_C = 25 °C, T_{VJ} ≤ 175 °C	
$I_{DS\,(pulsed)}$	Maximum Pulsed Drain-Source Current			1060		V_{GS} = 15 V; T_{VJ} = 25 °C; t_{Pmax} limited by T_{VJmax}	
$I_{SD\,(pulsed)}$	Maximum Pulsed Diode Current			1060		V_{GS} = 15 V; T_{VJ} = 25 °C; t_{Pmax} limited by T_{VJmax}	
$T_{VJ\,op}$	Maximum Virtual Junction Temperature under Switching Conditions	-40		150	°C	Operation	
				175		Intermittent with Reduced Life	

MOSFET Characteristics (Per Position) (T_{VJ} = 25 ˚C unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	1200			V	V_{GS} = 0 V, T_{VJ} = -40 °C	
$V_{GS(th)}$	Gate Threshold Voltage	1.8	2.5	3.6		V_{DS} = V_{GS}, I_D = 140 mA	
I_{DSS}	Zero Gate Voltage Drain Current		10	250	µA	V_{GS} = 0 V, V_{DS} = 1200 V	
I_{GSS}	Gate-Source Leakage Current			2		V_{GS} = 15 V, V_{DS} = 0 V	
$R_{DS(on)}$	Drain-Source On-State Resistance (Devices Only)		2.67	3.55	mΩ	V_{GS} = 15 V, I_D = 530 A	Fig. 2 Fig. 3
			3.96			V_{GS} = 15 V, I_D = 530 A, T_{VJ} = 150 °C	
g_{fs}	Transconductance		375		S	V_{DS} = 20 V, I_{DS} = 530 A	Fig. 4
			364			V_{DS} = 20 V, I_{DS} = 530 A, T_{VJ} = 150 °C	
E_{On}	Turn-On Switching Energy, T_J = 25 °C T_J = 125 °C T_J = 150 °C		16.8 15.6 16.1		mJ	V_{DS} = 600 V, I_D = 530 A, V_{GS} = -4 V/+15 V, $R_{G(ext)}$ = 1.5 Ω, L = 13.6 µH	Fig. 11 Fig. 13
E_{Off}	Turn-Off Switching Energy, T_J = 25 °C T_J = 125 °C T_J = 150 °C		15.5 14.9 14.9				
$R_{G(int)}$	Internal Gate Resistance		2.9		Ω	V_{AC} = 25 mV, f = 100 kHz	
C_{iss}	Input Capacitance		39.6		nF	V_{GS} = 0 V, V_{DS} = 800 V, V_{AC} = 25 mV, f = 100 kHz	Fig. 9
C_{oss}	Output Capacitance		1.4				
C_{rss}	Reverse Transfer Capacitance		84		pF		
Q_{GS}	Gate to Source Charge		384		nC	V_{DS} = 800 V, V_{GS} = -4 V/+15 V I_D = 530 A Per IEC60747-8-4 pg 21	
Q_{GD}	Gate to Drain Charge		462				
Q_G	Total Gate Charge		1362				
$R_{th\ JC}$	FET Thermal Resistance, Junction to Case		0.065		°C/W		Fig. 17

Diode Characteristics (Per Position) (T_{VJ} = 25 ˚C unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
V_F	Diode Forward Voltage		5.7		V	V_{GS} = -4 V, I_F = 530 A, T_{VJ} = 25 °C	Fig. 7
			5.0			V_{GS} = -4 V, I_F = 530 A, T_{VJ} = 150 °C	
t_{rr}	Reverse Recovery Time		44		ns	V_{GS} = -5 V, I_{SD} = 530 A, V_R = 800 V di_F/dt = 14.0 A/ns, T_{VJ} = 150 °C	Fig. 31
Q_{RR}	Reverse Recovery Charge		8.5		µC		
I_{RRM}	Peak Reverse Recovery Current		300		A		
E_{rr}	Diode Energy T_{VJ} = 25 °C T_{VJ} = 125 °C T_{VJ} = 150 °C		0.52 1.75 2.37		mJ	V_{DS} = 600 V, I_D = 530A, V_{GS} = -5 V/20 V, $R_{G(ext)}$ = 1.5 Ω, L= 13.6 µH	Fig. 14

Module Physical Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
R_{1-3}	Package Resistance, M1 (High-Side)		0.42		mΩ	T_C = 25 °C, I_{SD} = 530 A, Note 1
			0.60			T_C = 150 °C, I_{SD} = 530 A, Note 1
R_{1-2}	Package Resistance, M2 (Low-Side)		0.28			T_C = 25 °C, I_{SD} = 530 A, Note 1
			0.40			T_C = 150 °C, I_{SD} = 530 A, Note 1
L_{Stray}	Stray Inductance		11.1		nH	Between Terminals 2 and 3
T_C	Case Temperature	-40		125	°C	
W	Weight		300		g	
M_S	Mounting Torque	4	5	5.5	N-m	Baseplate, M6-1.0 bolts
		4	5	5.5		Power Terminals, M6-1.0 bolts
V_{isol}	Case Isolation Voltage	5			kV	AC, 50 Hz, 1 min
	Clearance Distance	9			mm	Terminal to Terminal
		30				Terminal to Baseplate
	Creepage Distance	30				Terminal to Terminal
		40				Terminal to Baseplate

Note 1 Total Effective Resistance (Per Switch Position) = MOSFET $R_{DS(on)}$ + Switch Position Package Resistance.

Typical Performance

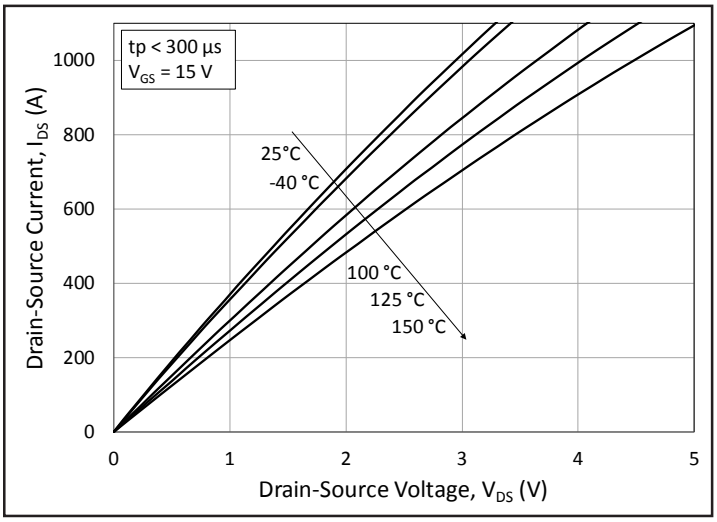


Figure 1. Output Characteristics for Various Junction Temperatures

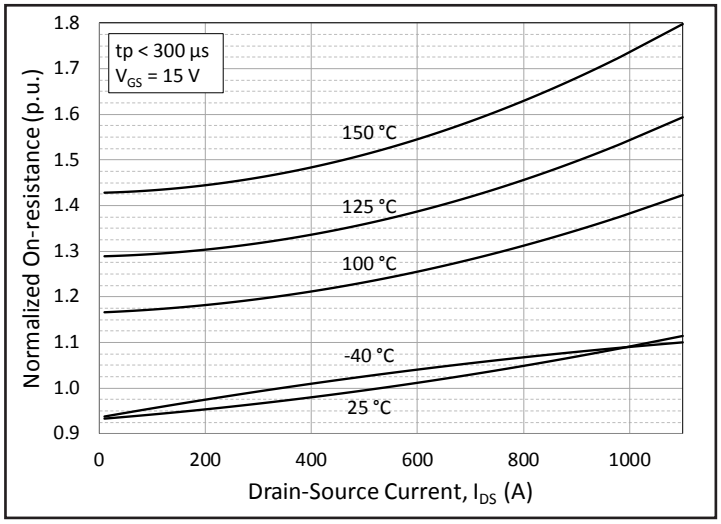


Figure 2. Normalized On-State Resistance vs. Drain Current for Various Junction Temperatures

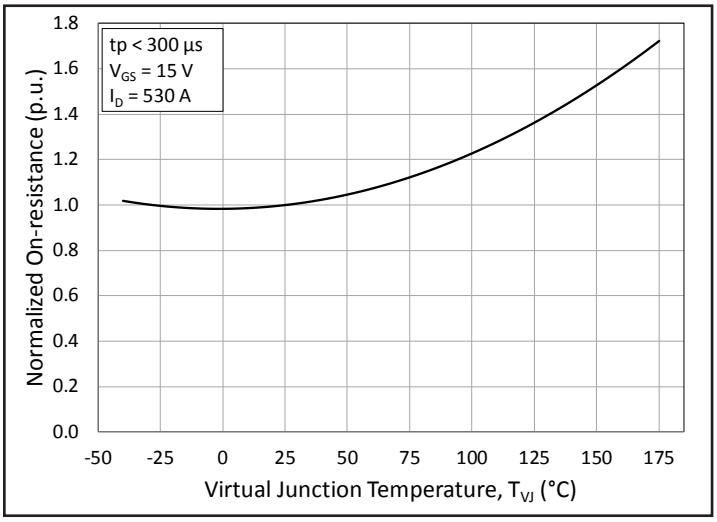


Figure 3. Normalized On-State Resistance vs. Junction Temperature

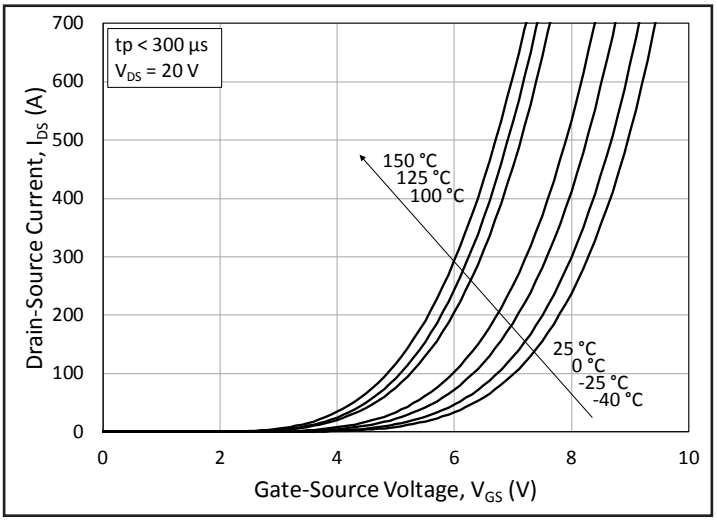


Figure 4. Transfer Characteristic for Various Junction Temperatures

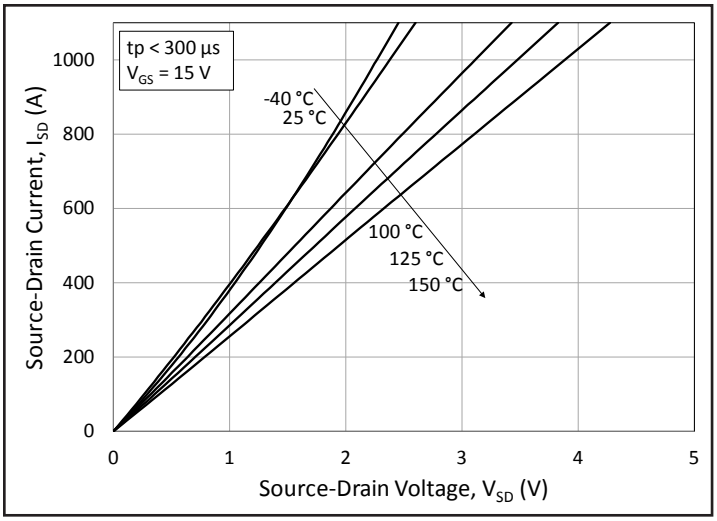


Figure 5. 3rd Quadrant Characteristic vs. Junction Temperatures at V_{GS} = 15 V

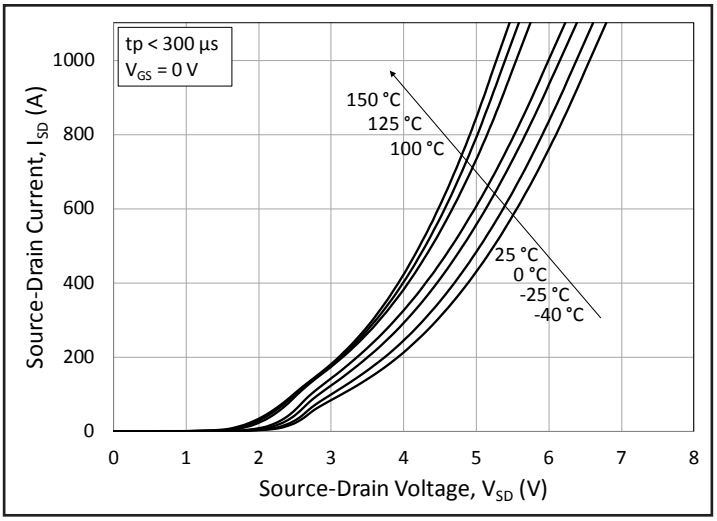


Figure 6. 3rd Quadrant Characteristic vs. Junction Temperatures at V_{GS} = 0 V (Diode)

Typical Performance

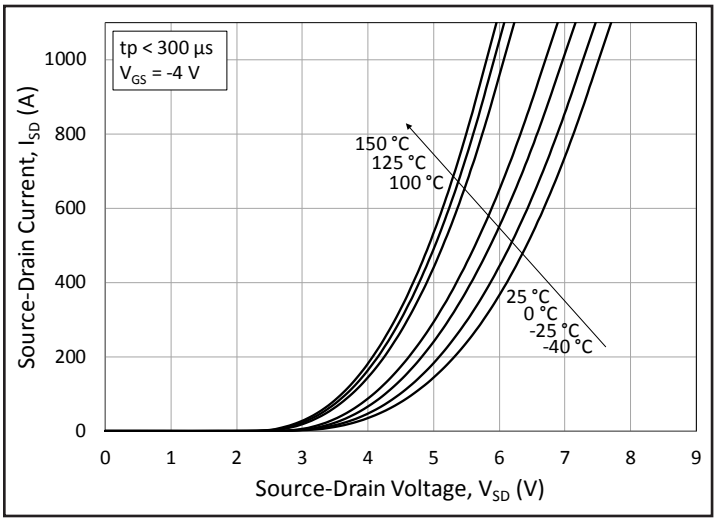


Figure 7. 3rd Quadrant Characteristic vs. Junction Temperatures at V_{GS} = - 4 V (Diode)

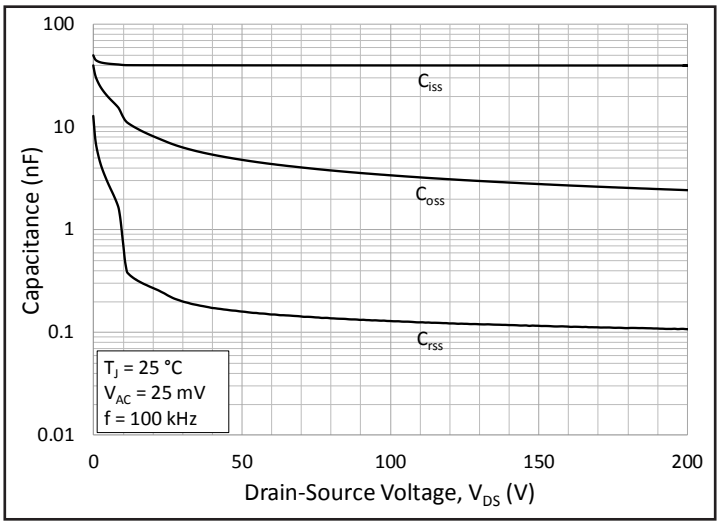


Figure 8. Typical Capacitances vs. Drain to Source Voltage (0 V - 200 V)

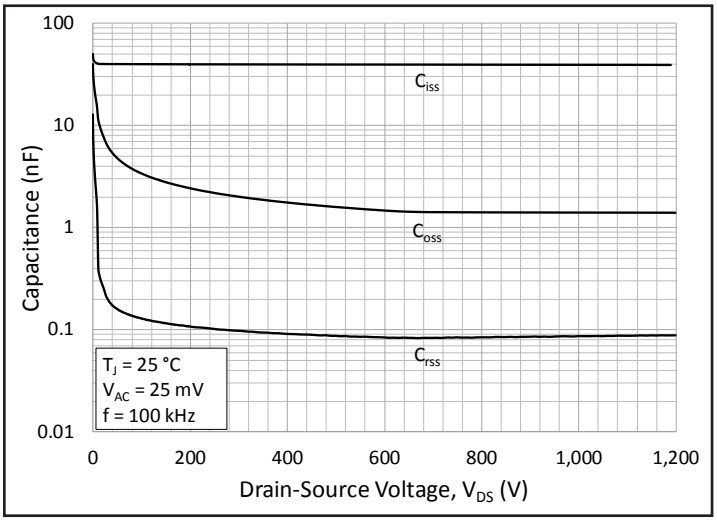


Figure 9. Typical Capacitances vs. Drain to Source Voltage (0 V - 1200 V)

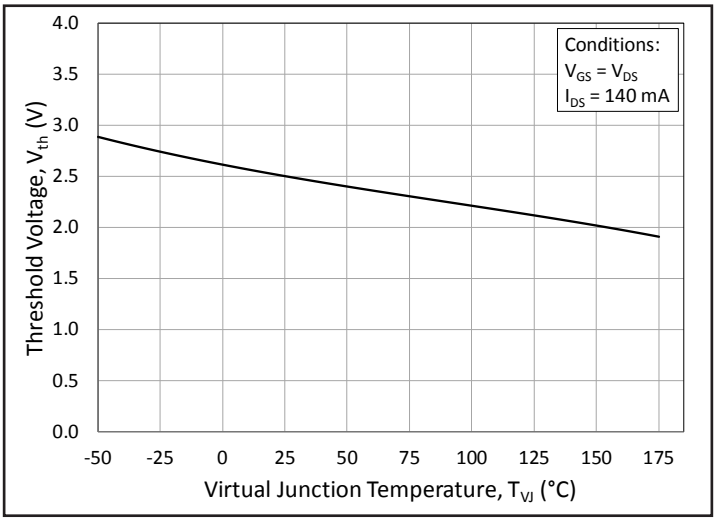


Figure 10. Threshold Voltage vs. Junction Temperature

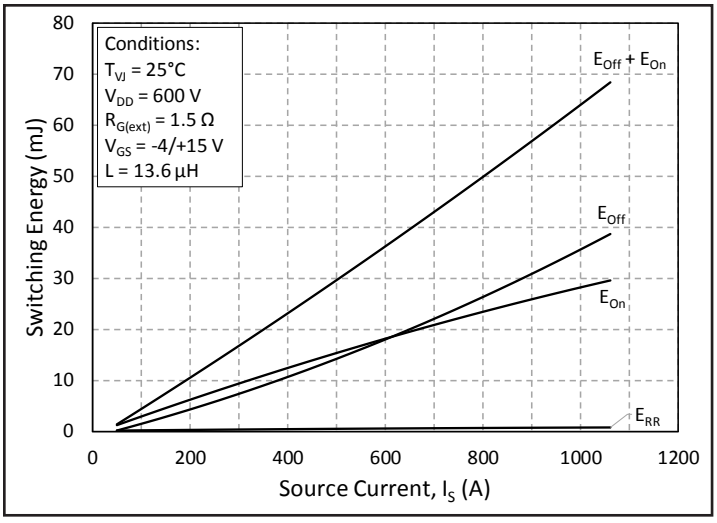


Figure 11. Switching Energy vs. Drain Current (V_{DS} = 600 V)

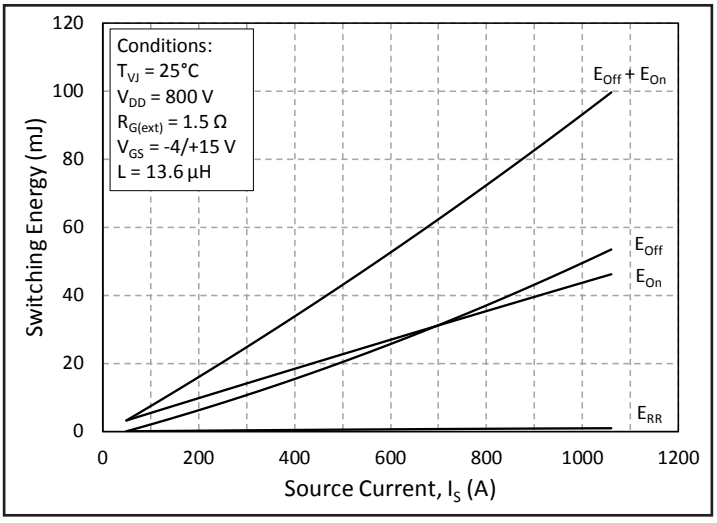


Figure 12. Switching Energy vs. Drain Current (V_{DS} = 800 V)

Typical Performance

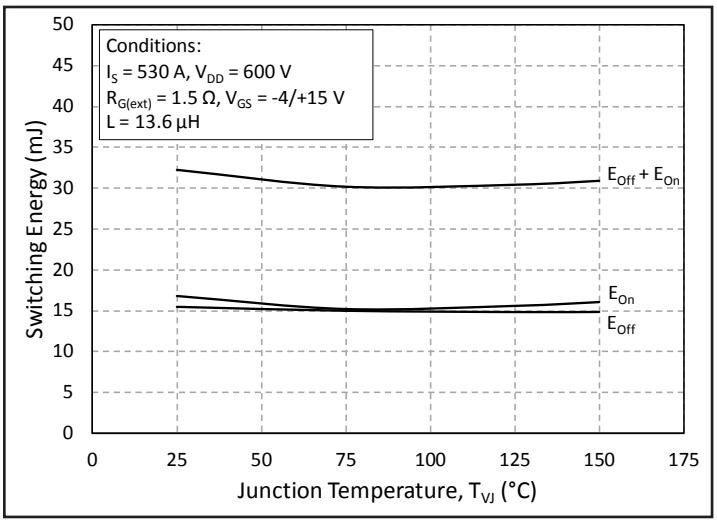


Figure 13. MOSFET Switching Energy vs. Junction Temperature

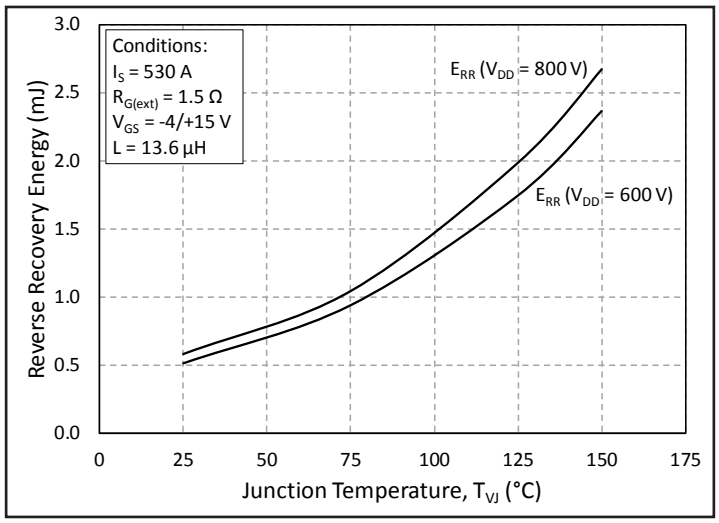


Figure 14. Reverse Recovery Energy vs. Junction Temperature

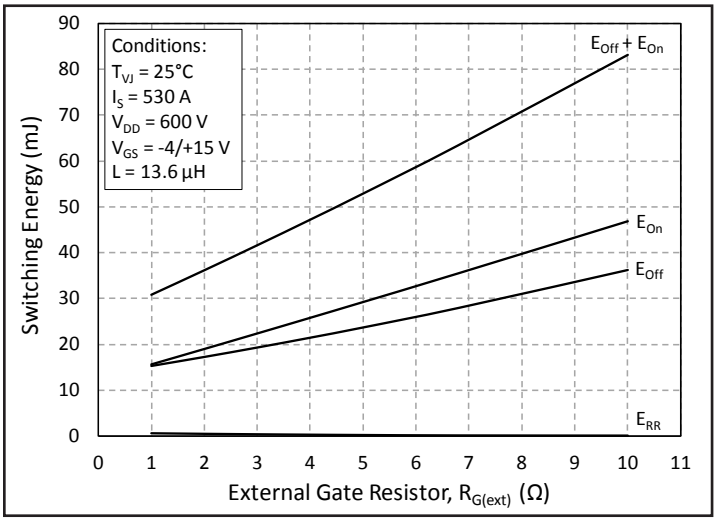


Figure 15. MOSFET Switching Energy vs. External Gate Resistance

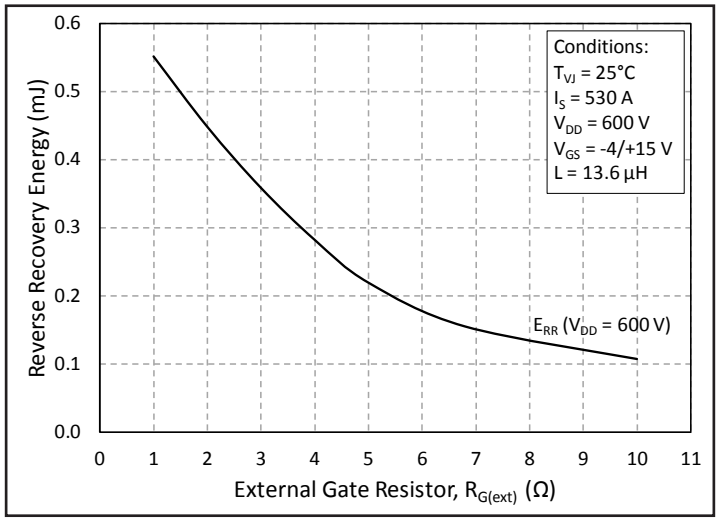


Figure 16. Reverse Recovery Energy vs. External Gate Resistance

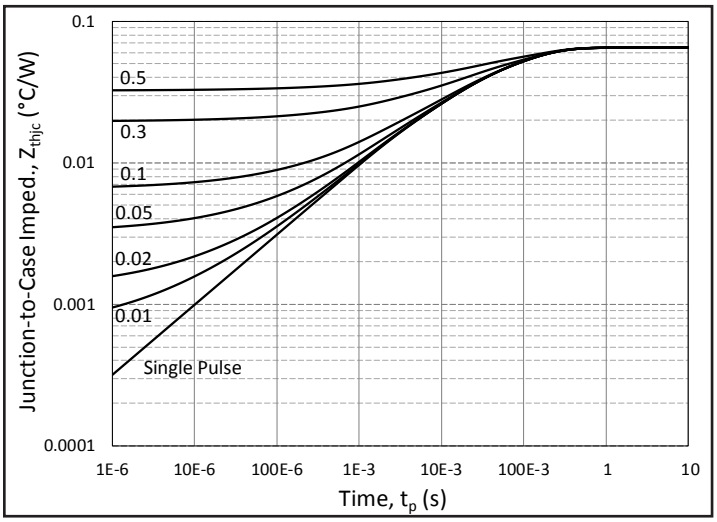


Figure 17. MOSFET Junction to Case Transient Thermal Impedance, $Z_{th\ JC}$ (°C/W)

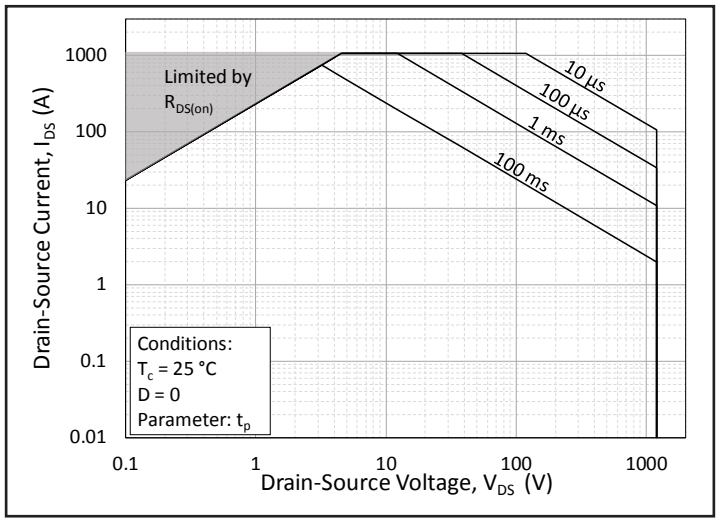


Figure 18. Forward Bias Safe Operating Area (FBSOA)

Typical Performance

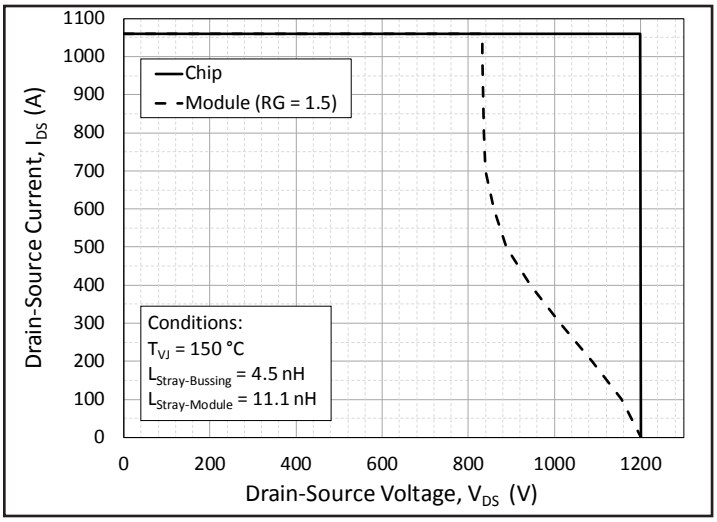


Figure 19. Reverse Bias Safe Operating Area (RBSOA)

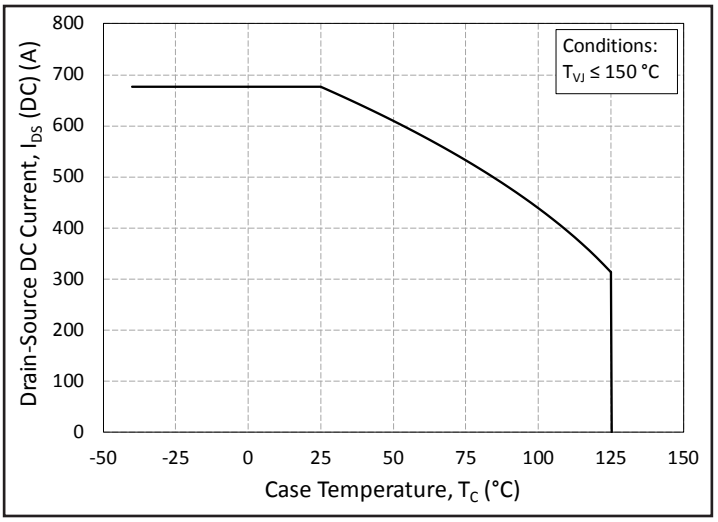


Figure 20. Continuous Drain Current Derating vs. Case Temperature

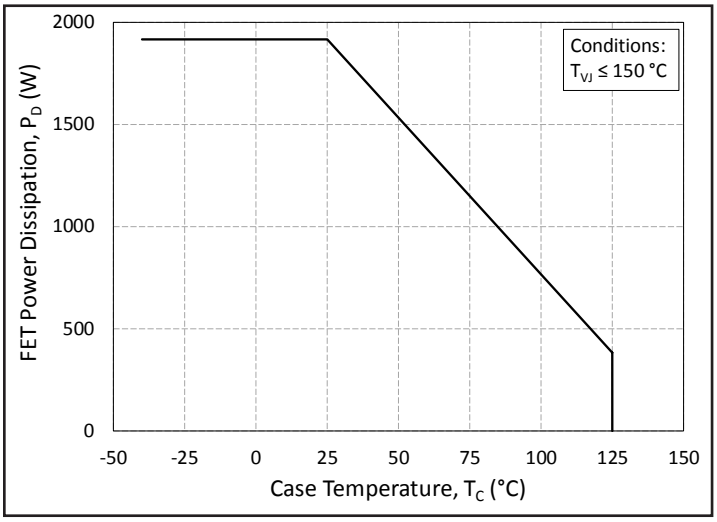


Figure 21. Maximum Power Dissipation Derating vs. Case Temperature

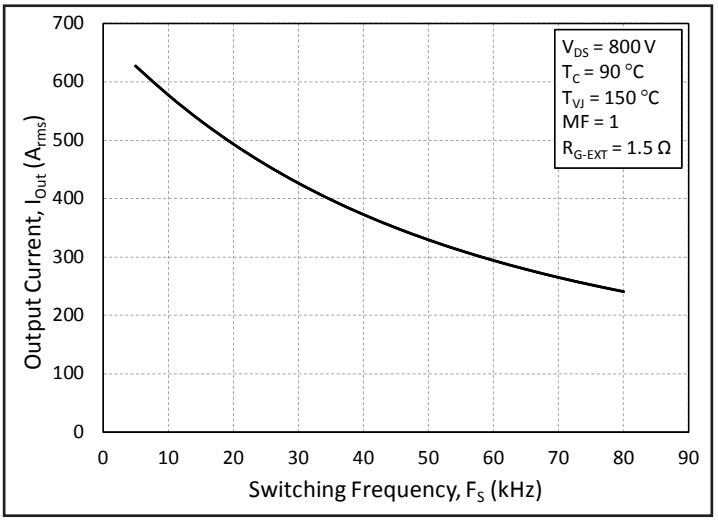


Figure 22. Typical Output Current Capability vs. Switching Frequency (Inverter Application)

Timing Characteristics

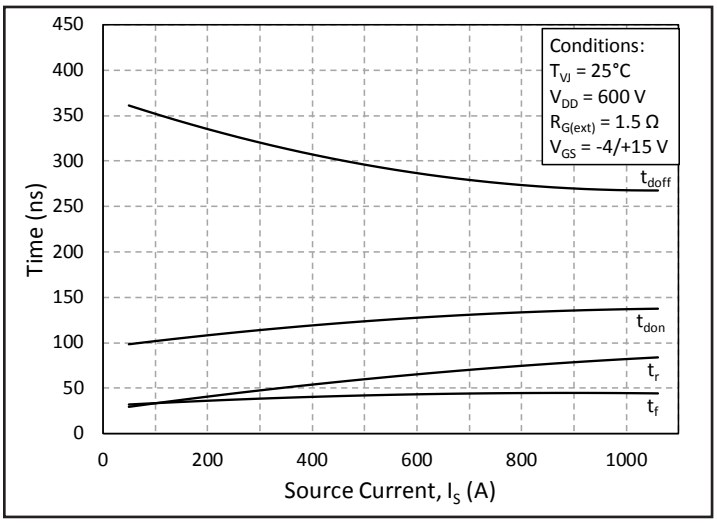


Figure 23. Timing vs. Source Current

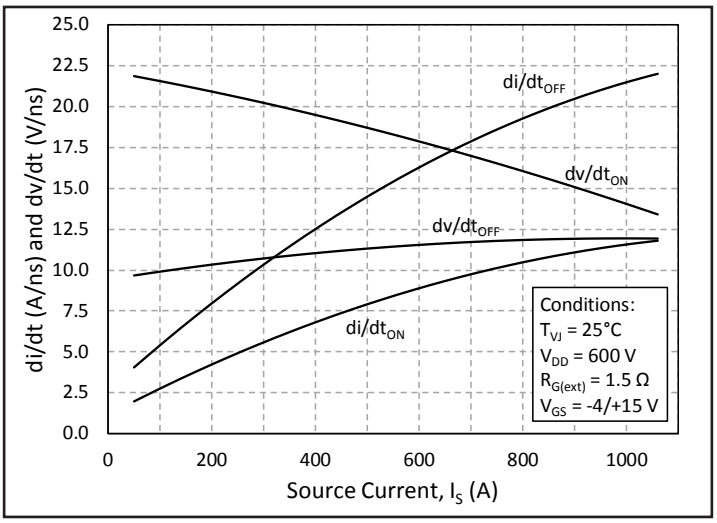


Figure 24. dv/dt and di/dt vs. Source Current

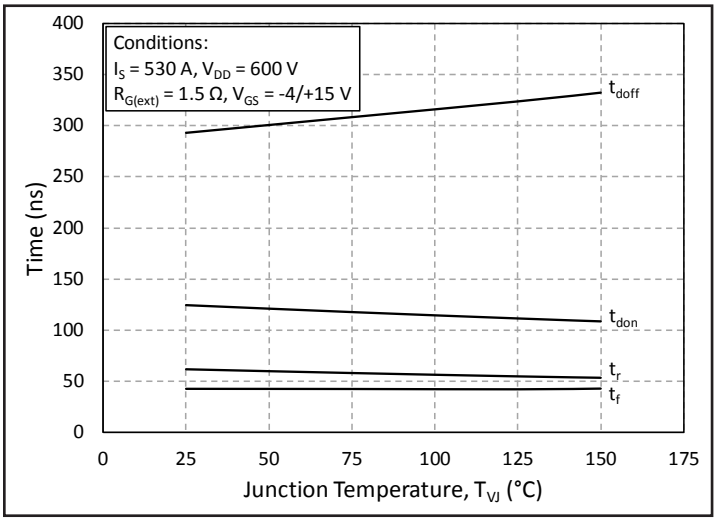


Figure 25. Timing vs. Junction Temperature

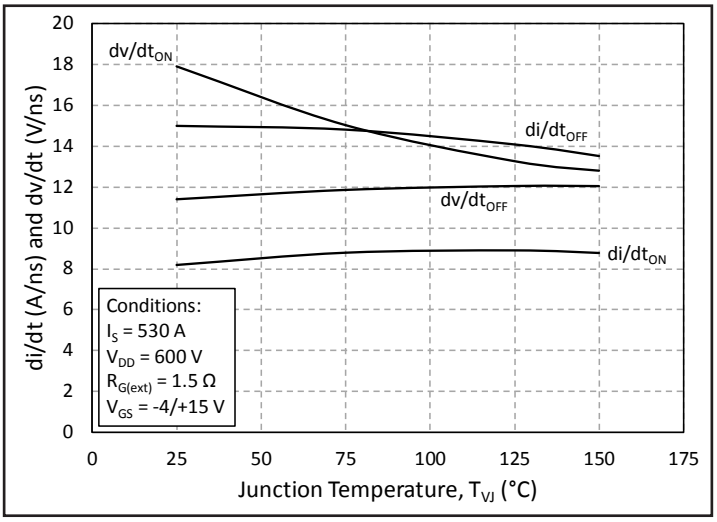


Figure 26. dv/dt and di/dt vs. Junction Temperature

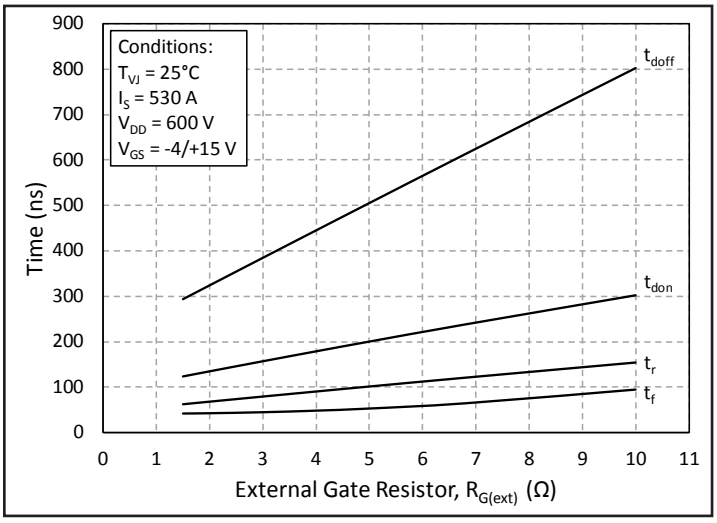


Figure 27. Timing vs. External Gate Resistance

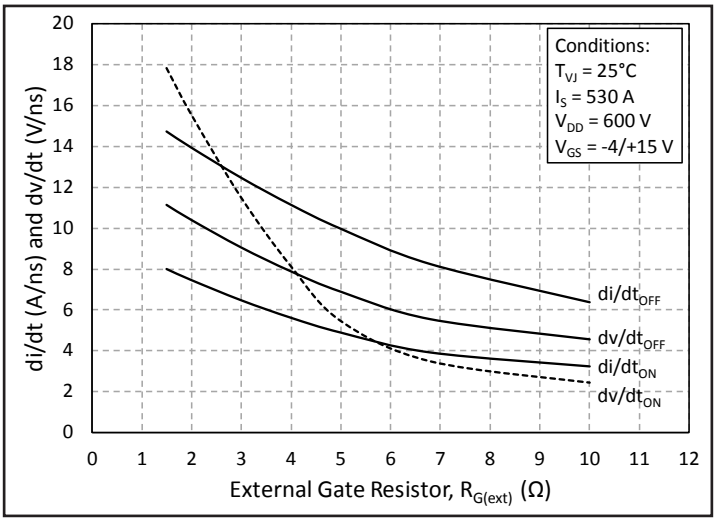


Figure 28. dv/dt and di/dt vs. External Gate Resistance

Definitions

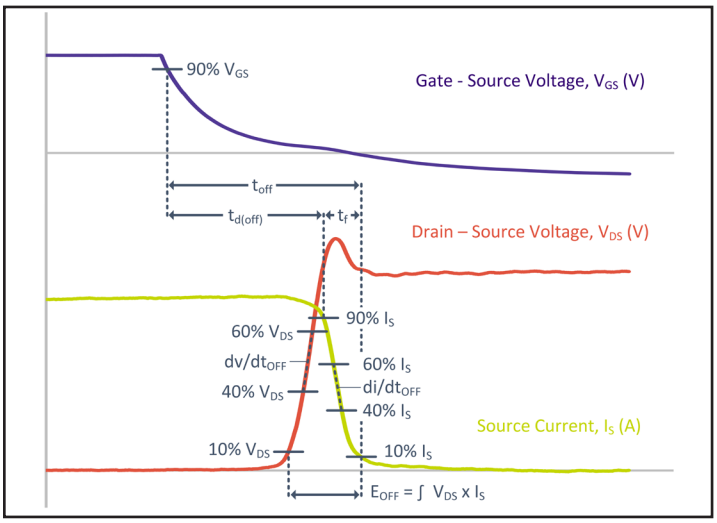


Figure 29. Turn-off Transient Definitions

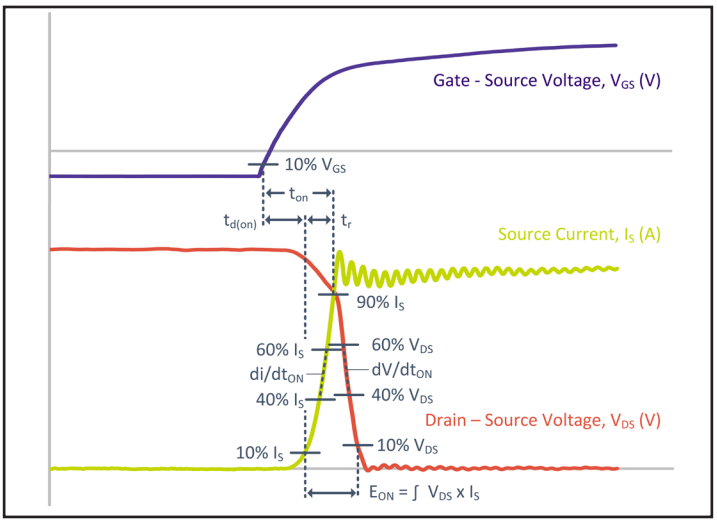


Figure 30. Turn-on Transient Definitions

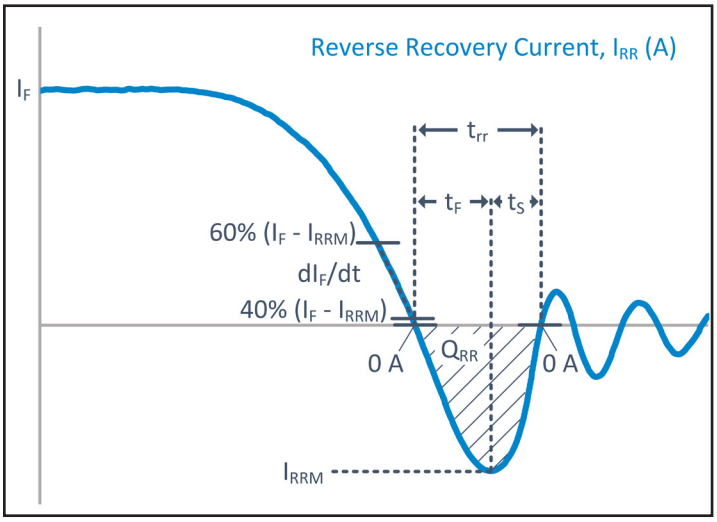


Figure 31. Reverse Recovery Definitions

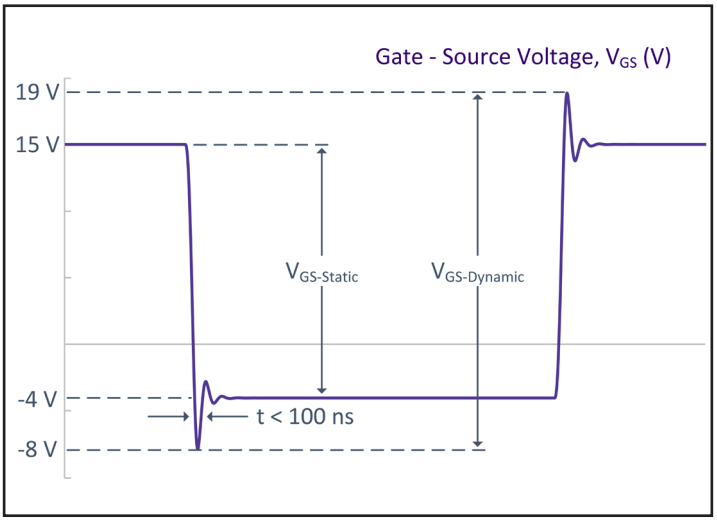
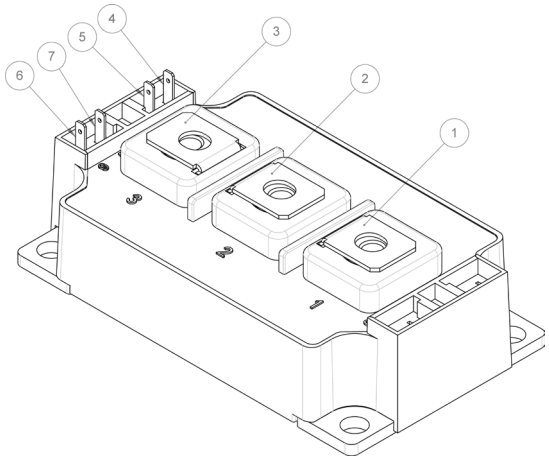
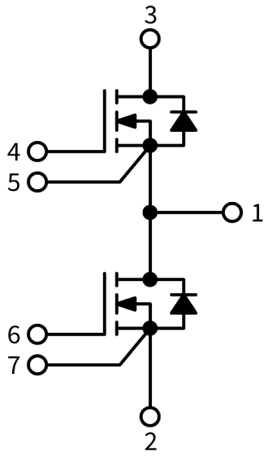


Figure 32. V_{GS} Transient Definitions

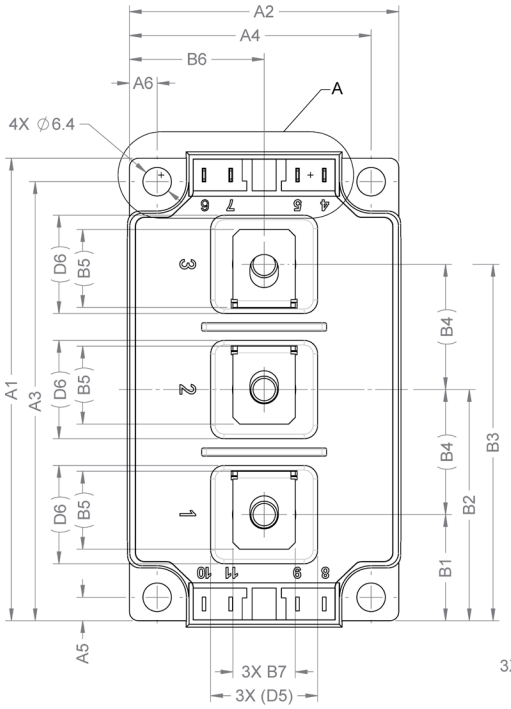
Schematic and Pin Out

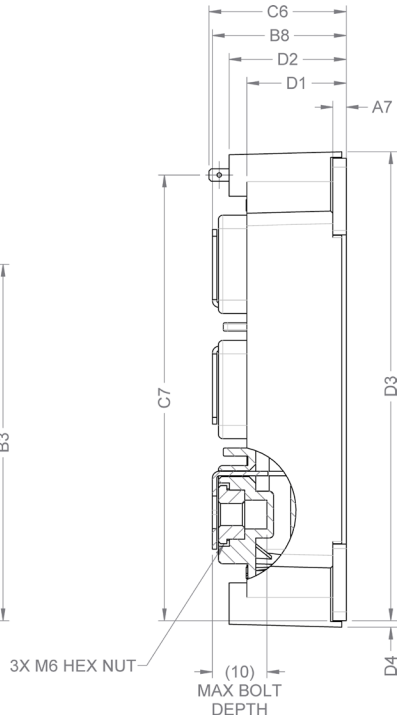




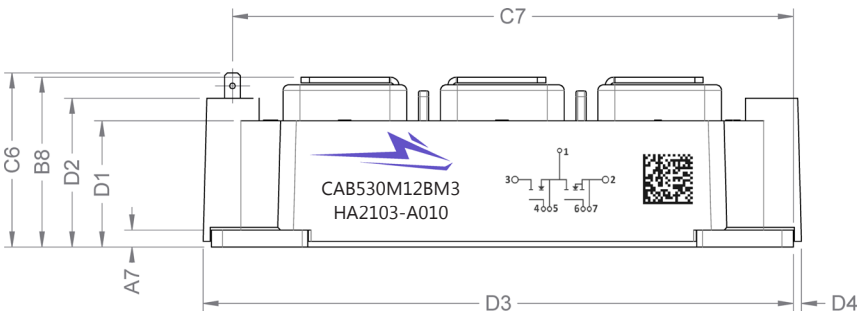
Note 2. The anti-parallel diodes shown in the schematic are MOSFET body diodes.

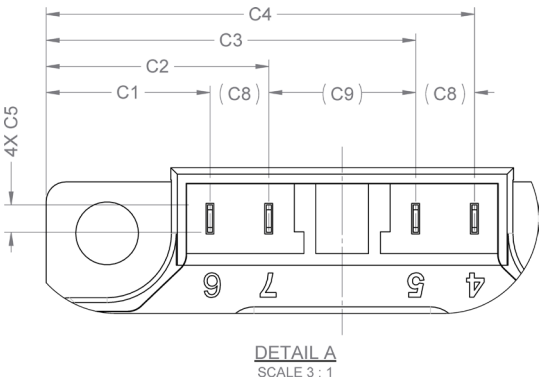
Package Dimensions (mm)





DIMENSION TABLE		
SYMBOL	DIMENSION	TOLERANCE
A1	103.5	±0.30
A2	60.44	±0.30
A3	98.25	±0.30
A4	54.22	±0.30
A5	5.25	±0.30
A6	6.22	±0.30
A7	3	±0.30
B1	23.75	±0.40
B2	51.75	±0.40
B3	79.75	±0.40
B4	(28)	REF.
B5	(17.43)	REF.
B6	30.23	±0.40
B7	(14)	REF.
B8	30.03	±0.40
C1	16.73	±0.40
C2	22.73	±0.40
C3	37.73	±0.40
C4	43.73	±0.40
C5	2.8	±0.40
C6	30.8	±0.50
C7	99.75	±0.40
C8	(6)	REF.
C9	(15)	REF.
D1	22.3	±0.30
D2	26.3	±0.30
D3	104.95	±0.30
D4	1.45	±0.40
D5	(24)	REF.
D6	(22)	REF.





Supporting Links & Tools

- CGD1200HB2P-BM3 Evaluation Gate Driver
- CGD12HB00D: Differential Transceiver Board
- CPWR-AN-35: Thermal Interface Material Application Note
- KIT-CRD-CIL12N-BM: Dynamic Performance Evaluation Board for the BM2 and BM3 Module

Notes

- This product has not been designed or tested for use in, and is not intended for use in, applications implanted into the human body nor in applications in which failure of the product could lead to death, personal injury or property damage, including but not limited to equipment used in the operation of nuclear facilities, life-support machines, cardiac defibrillators or similar emergency medical equipment, aircraft navigation or communication or control systems, or air traffic control systems.

- The SiC MOSFET module switches at speeds beyond what is customarily associated with IGBT-based modules. Therefore, special precautions are required to realize optimal performance. The interconnection between the gate driver and module housing needs to be as short as possible. This will afford optimal switching time and avoid the potential for device oscillation. Also, great care is required to insure minimum inductance between the module and DC link capacitors to avoid excessive VDS overshoot.