

# SN54S135, SN74S135 QUADRUPLE EXCLUSIVE-OR/NOR GATES

SDLS204

DECEMBER 1972—REVISED MARCH 1988

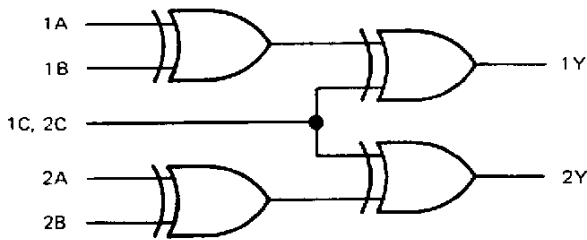
- Fully Compatible with Most TTL and TTL MSI Circuits
- Fully Schottky Clamping Reduces Delay Times . . . 8 ns Typical
- Can Operate as Exclusive-OR Gate (C Input Low) or as Exclusive-NOR Gate (C Input High)

FUNCTION TABLE

INPUTS			OUTPUT
A	B	C	Y
L	L	L	L
L	H	L	H
H	L	L	H
H	H	L	L
L	L	H	H
L	H	H	L
H	L	H	L
H	H	H	H

H = high level, L = low level

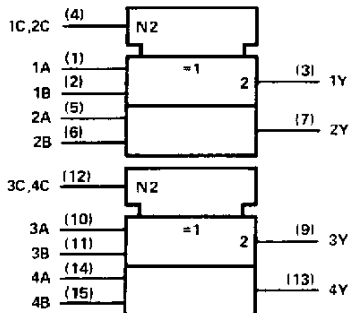
### logic diagram (one half)



### positive logic

$$Y = A \oplus B \oplus C = \overline{A}\overline{B}C + \overline{A}B\overline{C} + A\overline{B}\overline{C} + ABC$$

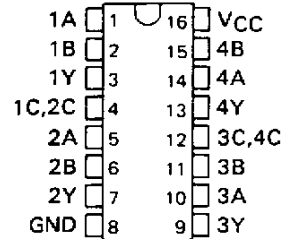
### logic symbol†



†This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12. Pin numbers are for D, J, N, and W packages.

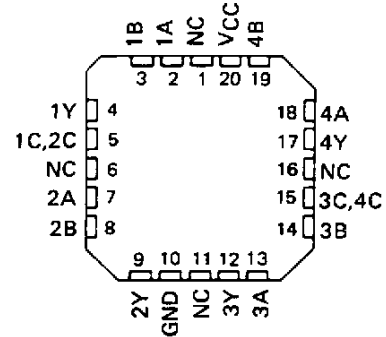
SN54S135 . . . J OR W PACKAGE  
SN74S135 . . . D OR N PACKAGE

(TOP VIEW)



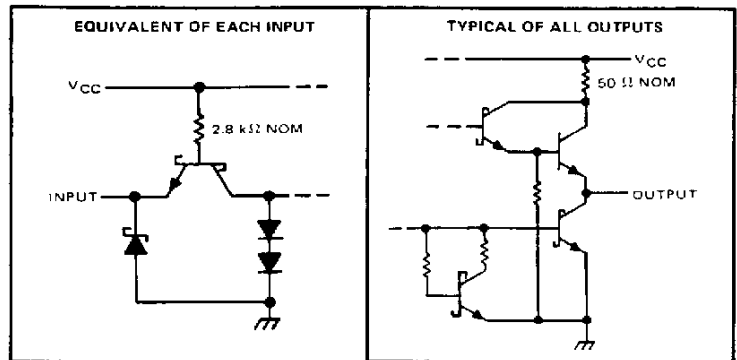
SN54S135 . . . FK PACKAGE

(TOP VIEW)



NC - No internal connection

### schematics of inputs and outputs



Resistor values shown are nominal.

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# SN54S135, SN74S135 QUADRUPLE EXCLUSIVE-OR/NOR GATES

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1)	7 V
Input voltage	5.5 V
Operating free-air temperature range: SN54S135	-55°C to 125°C
SN74S135	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54S135			SN74S135			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, $V_{CC}$	4.5	5	5.5	4.75	5	5.25	V
High-level output current, $I_{OH}$			-1			-1	mA
Low-level output current, $I_{OL}$			20			20	mA
Operating free-air temperature, $T_A$	-65		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
$V_{IH}$ High-level input voltage		2			V
$V_{IL}$ Low-level input voltage				0.8	V
$V_{IK}$ Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.2	V
$V_{OH}$ High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V},$ $V_{IL} = 0.8 \text{ V}, I_{OH} = -1 \text{ mA}$	SN54S' 2.5	3.4		V
		SN74S' 2.7	3.4		
$V_{OL}$ Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V},$ $V_{IL} = 0.8 \text{ V}, I_{OL} = 20 \text{ mA}$			0.5	V
$I_I$ Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1	mA
$I_{IH}$ High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			50	µA
$I_{IL}$ Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.5 \text{ V}$			-2	mA
$I_{OS}$ Short-circuit output current§	$V_{CC} = \text{MAX}$	-40		-100	mA
$I_{CC}$ Supply current	$V_{CC} = \text{MAX},$ See Note 2		65	99	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.

‡ All typical values are at  $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ .

§ Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

NOTE 2:  $I_{CC}$  is measured with the inputs grounded and the outputs open.

switching characteristics,  $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

PARAMETER	FROM (INPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}$	A or B	B or A = L, C = L	8.5	11	13	ns
$t_{PHL}$						
$t_{PLH}$	A or B	B or A = H, C = L	8	9	12	ns
$t_{PHL}$						
$t_{PLH}$	A or B	B or A = L, C = H	10	6.5	15	ns
$t_{PHL}$						
$t_{PLH}$	A or B	B or A = H, C = H	8.5	7	12	ns
$t_{PHL}$						
$t_{PLH}$	C	A = B	8	9.5	12	ns
$t_{PHL}$						
$t_{PLH}$	C	A ≠ B	7.5	7.5	11.5	ns
$t_{PHL}$						

$C_L = 15 \text{ pF}, R_L = 280 \Omega,$   
See Note 3

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

  
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**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
SN54S135J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI	-55 to 125		
SN74S135N	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI	0 to 70		
SN74S135N	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI	0 to 70		
SNJ54S135J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI	-55 to 125		
SNJ54S135J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI	-55 to 125		
SNJ54S135W	OBSOLETE	CFP	W	16		TBD	Call TI	Call TI	-55 to 125		
SNJ54S135W	OBSOLETE	CFP	W	16		TBD	Call TI	Call TI	-55 to 125		

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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**OTHER QUALIFIED VERSIONS OF SN54S135, SN74S135 :**

- Catalog: [SN74S135](#)
- Military: [SN54S135](#)

## NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within MIL STD 1835 GDFP2-F16

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - (C) Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - (D) The 20 pin end lead shoulder width is a vendor option, either half or full width.

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