Low Power HDMI/DVI Transmitter with De-Interlacer and CEC

ADV7541

FEATURES

General
- Low power HDMI/DVI transmitter ideal for portable applications
- De-interlacer operates from 480i to 1080i with no external memory required
- CEC controller and buffer reduces system overhead
- Incorporates HDMI v.1.4 (x.v.Color) technology
- Compatible with DVI v.1.0
- Optional embedded HDCP keys to support HDCP 1.3
- Single 1.8 V supply
- Video/audio inputs accept logic levels from 1.8 V to 3.3 V

Digital video
- 150 MHz operation supports all video and graphics resolutions from 480i to 1080p
- De-interlacer requires no external memory
- Programmable 2-way color space converter
- Supports RGB, YCbCr, and DDR
- Supports ITU656-based embedded syncs
- Auto input video format timing detection (CEA-861E)

Digital audio
- Supports standard S/PDIF for stereo LPCM or compressed audio up to 192 kHz
- 2-channel uncompressed LPCM I²S audio up to 192 kHz

Special features for easy system design
- On-chip MPU with I²C master to perform EDID reading and HDCP operations; reports HDMI events through interrupts and registers
- 5 V tolerant I²C and HPD I/Os, no extra device needed
- No audio master clock needed for supporting S/PDIF and I²S
- 5 V generator for Hot Plug detect in portable applications

APPLICATIONS

Cellular handsets
Digital video cameras
Digital still cameras
Personal media players
Gaming
DVD players and recorders
Digital set-top boxes
HDMI repeaters

FUNCTIONAL BLOCK DIAGRAM

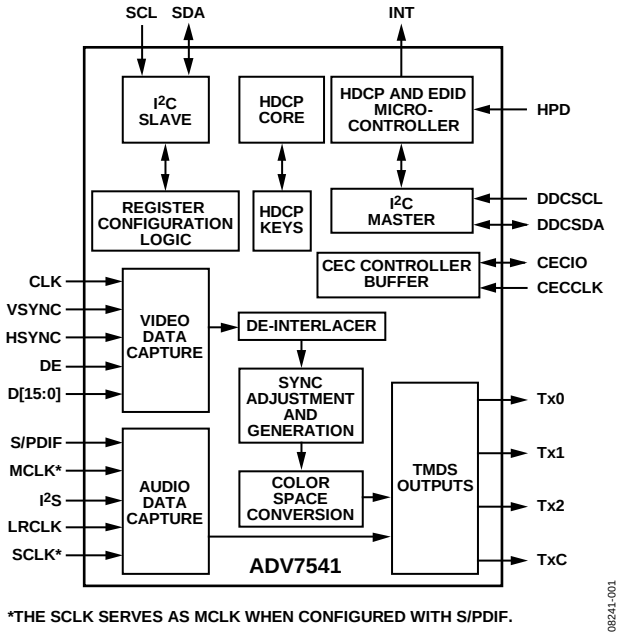

Figure 1.

GENERAL DESCRIPTION

The ADV7541 is a 150 MHz, high definition multimedia interface (HDMI) transmitter. It supports HDTV formats up to 1080p and computer graphic resolutions up to SXGA at 75 Hz.

With the optional inclusion of embedded HDCP keys, the ADV7541 allows the secure transmission of protected content, as specified by the HDCP 1.3 protocol.

The ADV7541 supports x.v.Color™ (Gamut Metadata) for a wider color gamut.

The ADV7541 supports both S/PDIF and 2-channel I²S audio. Its high fidelity, 2-channel I²S can transmit stereo at up to a 192 kHz sampling rate. The S/PDIF can carry stereo LPCM audio or compressed audio including Dolby® Digital and DTS®.

The ADV7541 helps to reduce system design complexity and cost by incorporating such features as an I²C® master for EDID reading and 5 V tolerance on I²C and Hot Plug™ detect pins.

Fabricated in an advanced CMOS process, the ADV7541 is available in a space-saving, 49-ball WLCSP surface-mount package. This package is RoHS compliant and specified to operate from −25°C to +85°C.

Rev. A

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113

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REVISION HISTORY

6/10—Rev. 0 to Rev. A

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7/09—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

AVDD = DVDD = 1.8 V.

Table 1.

Parameter		Temp	Test Level[1]	Min	Typ	Max	Unit	Test Conditions/ Comments
DIGITAL INPUTS								
Data Clock								
CLK to Input Jitter		25°C	IV		2		ns	
Data Inputs (Video and Audio)								
Input Voltage, High	V_{IH}	Full	VI	1.4		3.5	V	
Input Voltage, Low	V_{IL}	Full	VI	−0.3		+0.7	V	
Input Capacitance		25°C	VIII		1.0	1.5	pF	
I^2C Lines (DDCSDA, DDCSCL, SDA, SCL)								
Input Voltage, High	V_{IH}	Full	VI	1.4		5.0	V	
Input Voltage, Low	V_{IL}	Full	VI	−0.3		+0.8	V	
CECIO and CECCLK								
Input Voltage, High	V_{IH}	Full	VI	1.4		3.5	V	
Input Voltage, Low	V_{IL}	Full	VI	−0.3		+0.7	V	
DIGITAL OUTPUTS								
Output Voltage, High	V_{OH}	Full	VI	V_{DD} − 0.1			V	
Output Voltage, Low	V_{OL}	Full	VI			0.4	V	
THERMAL CHARACTERISTICS								
Thermal Resistance								
Junction-to-Case	θ_{JC}	Full	V		20		°C/W	
Junction-to-Ambient	θ_{JA}	Full	V		43		°C/W	
Ambient Temperature	T_A	Full	V	0	25	85	°C	
DC SPECIFICATIONS								
Input Leakage Current	I_{IL}	25°C	VI	−1		+1	µA	
POWER SUPPLY								
1.8 V Supply Voltage (DVDD, AVDD)		Full	IV	1.7	1.8	1.9	V	
1.8 V Supply Voltage Noise Limit								
DVDD		Full	IV			64	mV rms	
AVDD		Full	IV			2	mV rms	
Power-Down Current		25°C	IV		10		µA	
Transmitter Total Power								
De-Interlacer Off		Full	VI			125	mW	1080p, typical random pattern with CSC off
De-Interlacer On		Full	VI			295	mW	1080i in, 1080p out, typical random pattern with CSC off
AC SPECIFICATIONS								
TMDS Output Clock Frequency		25°C	IV	20		150	MHz	
TMDS Output Clock Duty Cycle		25°C	IV	48		52	%	
Input Video Clock Frequency		Full	IV			150	MHz	
Input Video Data Setup Time	t_{VSU}	Full	IV	1			ns	
Input Video Data Hold Time	t_{VHLD}	Full	IV	0.7			ns	
TMDS Differential Swing		25°C	VII	800	1000	1200	mV	
Differential Output Timing								
Low-to-High Transition Time		25°C	VII	75	175		ps	
High-to-Low Transition Time		25°C	VII	75	175		ps	
VSYNC and HSYNC Delay from DE Falling Edge		25°C	IV		1		UI[2]	
VSYNC and HSYNC Delay to DE Rising Edge		25°C	IV		1		UI[2]	

Parameter		Temp	Test Level[1]	Min	Typ	Max	Unit	Test Conditions/ Comments
AUDIO AC TIMING[3]								
SCLK Duty Cycle								
When N Divide-By-2 is Even		Full	IV	40	50	60	%	
When N Divide-By-2 is Odd		Full	IV	49	50	51	%	
I^2S, S/PDIF Setup	t_{ASU}	Full	IV	2			ns	
I^2S, S/PDIF Hold Time	t_{AHLD}	Full	IV	2			ns	
LRCLK Setup Time	t_{ASU}	Full	IV	2			ns	
LRCLK Hold Time	t_{AHLD}	Full	IV	2			ns	
CEC								
CECCLK Frequency[4]		Full	VIII	1	12	100	MHz	
CECCLK Accuracy		Full	VIII	−2		+2	%	
I^2C Interface								
SCL Clock Frequency		Full	IV			400[5]	kHz	
SDA Setup Time	t_{DSU}	Full	IV	100			ns	
SDA Hold Time	t_{DHO}	Full	IV	100			ns	
Setup for Start	t_{STASU}	Full	IV	0.6			µs	
Hold Time for Start	t_{STAH}	Full	IV	0.6			µs	
Setup for Stop	t_{STOSU}	Full	IV	0.6			µs	
Bus Free Between Stop and Start	t_{BUF}	Full	IV	1.3			µs	
SCL High	t_{HIGH}	Full	IV	0.6			µs	
SCL Low	t_{LOW}	Full	IV	1.3			µs	

[1] See Explanation of Test Levels section.
[2] UI = unit interval.
[3] Only applies to S/PDIF if external MCLK used.
[4] 12 MHz crystal for default register settings.
[5] I^2C data rates of 100 kHz and 400 kHz supported.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Digital Inputs: I^2C (DDCSDA, DDCSCL, SDA, SCL) and HPD	+5.5 V to −0.3 V
Digital Inputs: Video/Audio Inputs (CECIO, CECCLK)	+3.63 V to −0.3 V
Digital Output Current	20 mA
Operating Temperature Range	−40°C to +100°C
Storage Temperature Range	−65°C to +150°C
Maximum Junction Temperature	150°C
Maximum Case Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

EXPLANATION OF TEST LEVELS

I. 100% production tested.

II. 100% production tested at 25°C and sample tested at specified temperatures.

III. Sample tested only.

IV. Parameter is guaranteed by design and characterization testing.

V. Parameter is a typical value only.

VI. 100% production tested at 25°C; guaranteed by design and characterization testing.

VII. Limits defined by HDMI specification; guaranteed by design and characterization testing.

VIII. Parameter is guaranteed by design.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

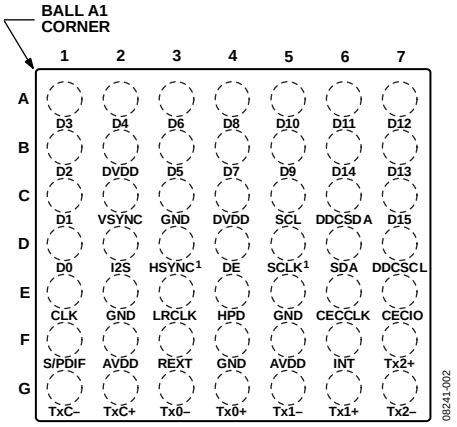

Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
C7, B6, B7, A7, A6, A5, B5, A4, B4, A3, B3, A2, A1, B1, C1, D1	D[15:0]	I	Video Data Input. Digital input in RGB or YCbCr format. Supports typical CMOS logic levels from 1.8 V up to 3.3 V.
E1	CLK	I	Video Clock Input. Supports typical CMOS logic levels from 1.8 V up to 3.3 V.
D4	DE	I	Data Enable Bit for Digital Video. Supports typical CMOS logic levels from 1.8 V up to 3.3 V.
C2	VSYNC	I	Vertical Sync Input. Supports typical CMOS logic levels from 1.8 V up to 3.3 V.
D3	HSYNC	I	Horizontal Sync Input. Supports typical CMOS logic levels from 1.8 V to 3.3 V.
F3	REXT	I	Sets Internal Reference Currents. Place 3.92 kΩ resistor (1% tolerance) between this pin and ground.
E4	HPD	I	Hot Plug Detect Signal. This indicates to the interface whether the receiver is connected. 1.8 V to 5.0 V CMOS logic level.
D2	I2S	I	I^2S Audio Data Inputs. These represent the two channels of audio available through I^2S. Supports typical CMOS logic levels from 1.8 V up to 3.3 V.
F1	S/PDIF	I	S/PDIF (Sony/Philips Digital Interface) Audio Input. This is the audio input from a Sony/Philips digital interface. Supports typical CMOS logic levels from 1.8 V up to 3.3 V.
D5	SCLK	I	I^2S Audio Clock. Supports typical CMOS logic levels from 1.8 V up to 3.3 V. The SCLK pin serves as MCLK when configured with S/PDIF.
E3	LRCLK	I	Left/Right Channel Selection. Supports typical CMOS logic levels from1.8 V up to 3.3 V.
G1, G2	TxC−/TxC+	O	Differential Clock Output. Differential clock output at pixel clock rate; TMDS logic level.
G7, F7	Tx2−/Tx2+	O	Differential Output Channel 2. Differential output of the red data at 10× the pixel clock rate; TMDS logic level.
G5, G6	Tx1−/Tx1+	O	Differential Output Channel 1. Differential output of the green data at 10× the pixel clock rate; TMDS logic level.
G3, G4	Tx0−/Tx0+	O	Differential Output Channel 0. Differential output of the blue data at 10× the pixel clock rate; TMDS logic level.
F6	INT	O	Interrupt. CMOS logic level. A 2 kΩ pull-up resistor to interrupt the microcontroller I/O supply is recommended.
F2, F5	AVDD	P	1.8 V Power Supply for TMDS Outputs.
B2, C4	DVDD	P	1.8 V Power Supply for Digital and I/O Power Supply. These pins supply power to the digital logic and I/Os. They should be filtered and as quiet as possible.

Pin No.	Mnemonic	Type[1]	Description
C3, E2, E5, F4	GND	P	Ground. The ground return for all circuitry on-chip. It is recommended that the ADV7541 be assembled on a single, solid ground plane with careful attention given to ground current paths.
D6	SDA	C	Serial Port Data I/O. This pin serves as the serial port data I/O slave for register access. Supports CMOS logic levels from 1.8 V to 3.3 V.
C5	SCL	C	Serial Port Data Clock. This pin serves as the serial port data clock slave for register access. Supports CMOS logic levels from 1.8 V to 3.3 V.
C6	DDCSDA	C	Serial Port Data I/O to Receiver. This pin serves as the master to the DDC bus. 5 V CMOS logic level.
D7	DDCSCL	C	Serial Port Data Clock to Receiver. This pin serves as the master clock for the DDC bus. 5 V CMOS logic level.
E7	CECIO	C	CEC I/O.
E6	CECCLK	C	CEC external clock. Can be from 1 MHz to 100 MHz.

[1] I = input, O = output, P = power supply, and C = control.

APPLICATIONS INFORMATION

DESIGN RESOURCES

Analog Devices, Inc., offers the following design resources:

- Evaluation kits
- Reference design schematics
- Hardware and software guides
- Software driver reference code
- HDMI compliance pretest services
- Other support documentation is available under the nondisclosure agreement (NDA) from ATV_VideoTx_Apps@analog.com.

Other references include the following:

EIA/CEA-861E, which describes audio and video infoframes as well as the E-EDID structure for HDMI. It is available from Consumer Electronics Association (CEA).

The *HDMI v.1.4,* a defining document for HDMI Version 1.4, and the *HDMI Compliance Test Specification Version 1.4* are available from HDMI Licensing, LLC.

OUTLINE DIMENSIONS

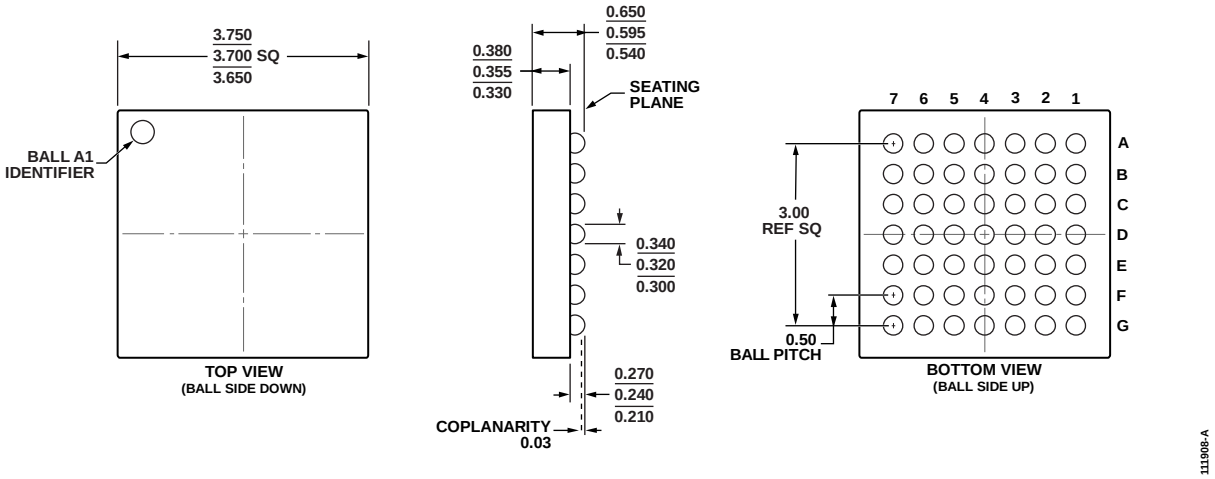

Figure 3. 49-Ball Wafer Level Chip Scale Package [WLCSP]
(CB-49-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADV7541BCBZ-2RL	−25°C to +85°C	49-Ball Wafer Level Chip Scale Package [WLCSP] with HDCP Keys	CB-49-2
ADV7541BCBZ-P-2RL	−25°C to +85°C	49-Ball Wafer Level Chip Scale Package [WLCSP] with No HDCP Keys	CB-49-2
EVAL-ADV7541-CKZ		Evaluation Kit (with HDCP Keys)	
EVAL-ADV7541P-CKZ		Evaluation Kit (with No HDCP Keys)	

[1] Z = RoHS Compliant Part.

NOTES

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NOTES

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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