January 2001 File Number 4062.9

2.5GHz/600MHz Dual Frequency Synthesizer

The Intersil 2.4GHz PRISM® chip set is a highly integrated six-chip solution for RF modems employing Direct Sequence Spread Spectrum (DSSS) signaling. The HFA3524 600MHz Dual Frequency Synthesizer is one of the six chips in the PRISM chip set (see the Typical Application Diagram).

The HFA3524 is a monolithic, integrated dual frequency synthesizer, including prescaler, is to be used as a local oscillator for RF and first IF of a dual conversion transceiver.

The HFA3524 contains a dual modulus prescaler. A 32/33 or 64/65 prescaler can be selected for the RF synthesizer and a 8/9 or a 16/17 prescaler can be selected for the IF synthesizer. Using a digital phase locked loop technique, the HFA3524 can generate a very stable, low noise signal for the RF and IF local oscillator. Serial data is transferred into the HFA3524 via a three wire interface (Data, Enable, Clock). Supply voltage can range from 2.7V to 5.5V. The HFA3524 features very low current consumption of 13mA at 3V.

Features

- 2.7V to 5.5V Operation
- Low Current Consumption
- Selectable Powerdown Mode I_{CC} = 1µA Typical at 3V
- Dual Modulus Prescaler, 32/33 or 64/65
- Selectable Charge Pump High Z State Mode

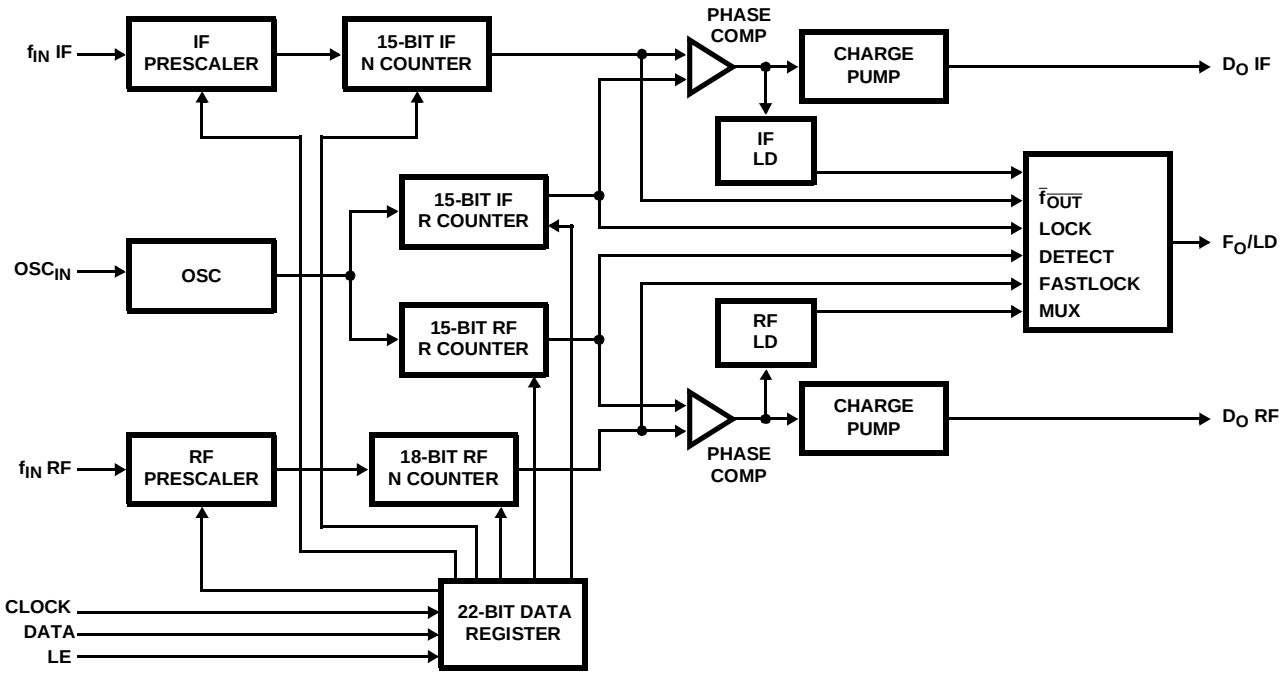
Applications

- Systems Targeting IEEE 802.11 Standard
- PCMCIA Wireless Transceiver
- Wireless Local Area Network Modems
- TDMA Packet Protocol Radios
- Part 15 Compliant Radio Links
- Portable Battery Powered Equipment

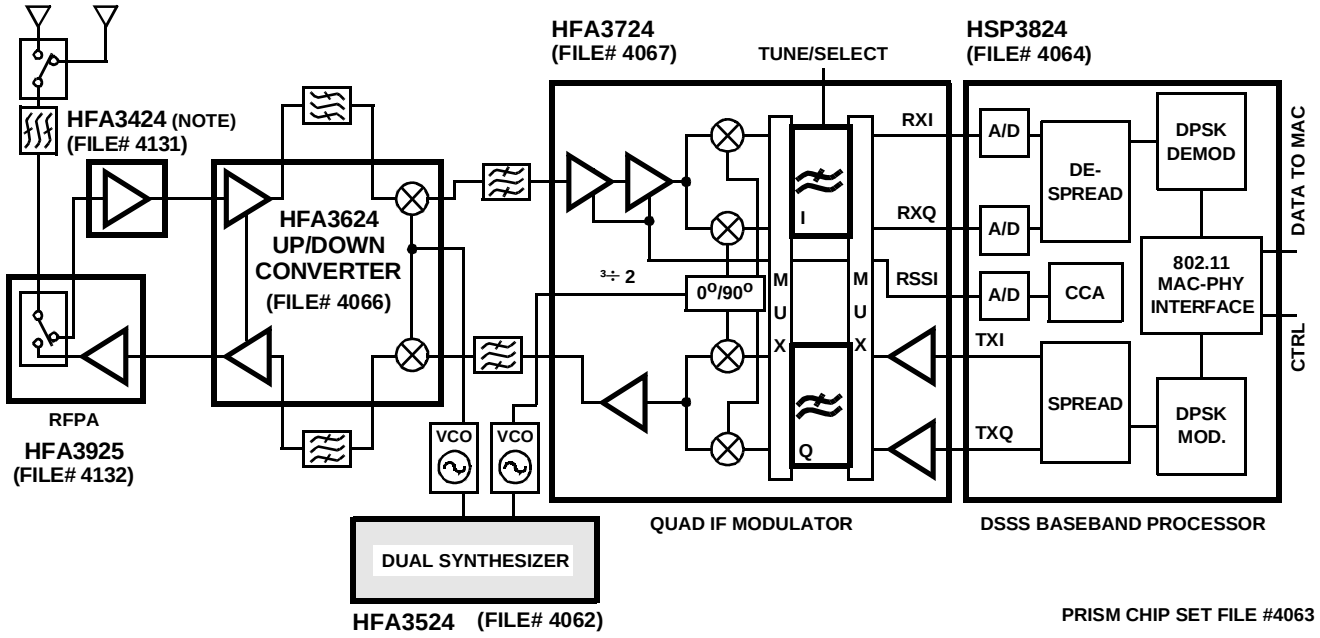
Ordering Information

PART NUMBER	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
HFA3524IA	-40 to 85	20 Ld TSSOP	M20.173
HFA3524IA96	-40 to 85	Tape and Reel	

Functional Block Diagram



Typical Application Diagram



NOTE: Required for systems targeting 802.11 specifications.

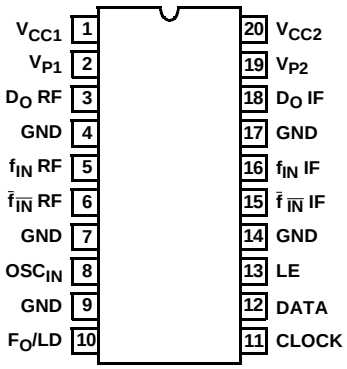
TYPICAL TRANSCEIVER APPLICATION CIRCUIT USING THE HFA352

For additional information on the PRISM chip set, see us on the web http://www.intersil.com/prism.

The four-digit file numbers are shown in Typical Application Diagram, and correspond to the appropriate circuit.

Pinout

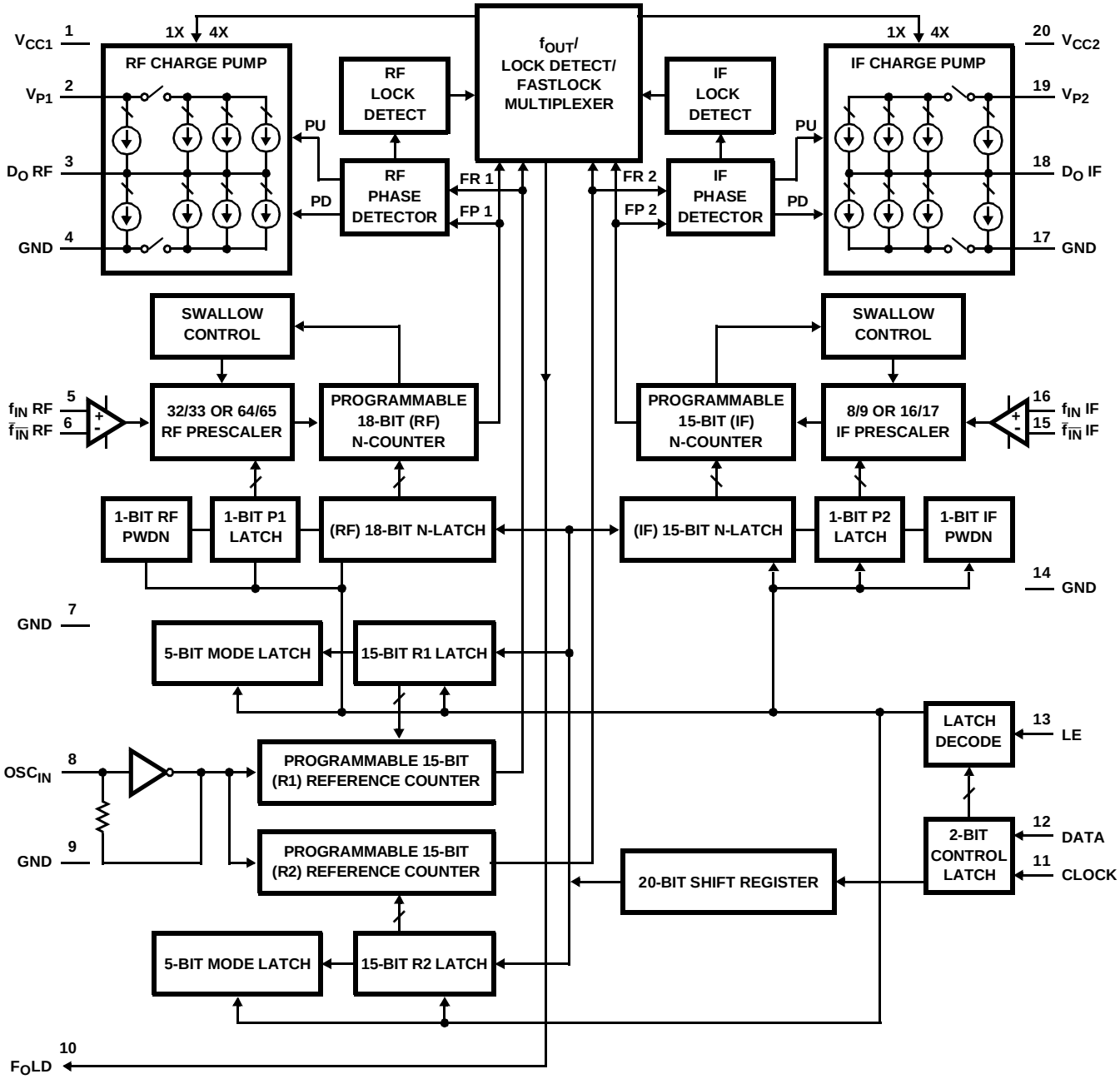
HFA3524 (TSSOP)
TOP VIEW



Pin Descriptions

PIN NUMBER	PIN NAME	I/O	DESCRIPTION
1	V_{CC1}	-	Power supply voltage input. Input may range from 2.7V to 5.5V. V_{CC1} must equal V_{CC2}. Bypass capacitors should be placed as close as possible to this pin and be connected directly to the ground plane.
2	V_{P1}	-	Power Supply for RF charge pump. Must be > V_{CC}.
3	D_O RF	O	Internal charge pump output. For connection to a loop filter for driving the input of an external V_{CO}.
4	GND	-	Ground.
5	f_{IN} RF	I	RF prescaler input. Small signal input from the V_{CO}.
6	$\overline{f}_{IN}$ RF	I	RF prescaler complimentary input. A bypass capacitor should be placed as close as possible to this pin and be connected directly to the ground plane. Capacitor is optional with some loss of sensitivity.
7	GND	-	Ground.
8	OSC_{IN}	I	Oscillator input. The input has a V_{CC}/2 input threshold and can be driven from an external CMOS or TTL logic gate.
9	GND	-	Ground.
10	F_O/LD	O	Multiplexed output of the RF/IF programmable or reference dividers, RF/IF lock detect signals and Fastlock mode. CMOS output (see Programmable Modes).
11	Clock	I	High impedance CMOS Clock input. Data for the various counters is clocked in on the rising edge, into the 22-bit shift register.
12	Data	I	Binary serial data input. Data entered MSB first. The last two bits are the control bits. High impedance CMOS input.
13	LE	I	Load enable CMOS input. When LE goes HIGH, data stored in the shift registers is loaded into one of the 4 appropriate latches (control bit dependent).
14	GND	-	Ground.
15	$\overline{f}_{IN}$ IF	I	IF prescaler complimentary input. A bypass capacitor should be placed as close as possible to this pin and be connected directly to the ground plane. Capacitor is optional with some loss of sensitivity.
16	f_{IN} IF	I	IF prescaler input. Small signal input from the V_{CO}.
17	GND	-	Ground.
18	D_O IF	O	IF charge pump output. For connection to a loop filter for driving the input of an external V_{CO}.
19	V_{P2}	-	Power Supply for IF charge pump. Must be >V_{CC}.
20	V_{CC2}	-	Power supply voltage input Input may range from 2.7V to 5.5V. V_{CC2} must equal V_{CC1}. Bypass capacitors should be placed as close as possible to this pin and be connected directly to the ground plane.

Block Diagram



NOTES:

1. V_{CC1} supplies power to the RF prescaler, N-counter and phase detector. V_{CC2} supplies power to the IF prescaler, N-counter and phase detector, RF and IF R-counters along with the OSC_{IN} buffer and all digital circuitry. V_{CC1} and V_{CC2} are separated by a diode and must be run at the same voltage level.
2. V_{P1} and V_{P2} can be run independently as long as $V_P \geq V_{CC}$.

Absolute Maximum Ratings

Power Supply Voltage
- V_{CC} . . . . . -0.3V to +6.5V
- V_P . . . . . -0.3V to +6.5V

Voltage on Any Pin with GND = 0V (V_I) . . . . . -0.3V to +6.5V

Operating Conditions

Power Supply Voltage
- V_{CC} . . . . . 2.7V to 5.5V
- V_P . . . . . V_{CC} to +5.5V

Temperature (T_A) . . . . . -40^oC to 85^oC

Thermal Information

Thermal Resistance (Typical, Note 3) θ_{JA} ($^oC/W$)
- TSSOP Package 130

Maximum Storage Temperature Range (T_S) . . . . . -55^oC to 150^oC

Maximum Lead Temperature (Soldering 4s) (T_L) . . . . . 260^oC
(TSSOP - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

3. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

V_{CC} = 3.0V, V_P = 3.0V, $-40^oC < T_A < 85^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	HFA3524			UNITS
			MIN	TYP	MAX	
Power Supply Current	I_{CC}					
RF + IF		V_{CC} = 2.7V to 5.5V	-	13	-	mA
RF Only		V_{CC} = 2.7V to 5.5V	-	10	-	mA
Powerdown Current	$I_{CC-PWDN}$	V_{CC} = 3.0V	-	1	25	µA
Operating Frequency	f_{IN} RF		0.5	-	2.5	GHz
Operating Frequency	f_{IN} IF		45	-	600	MHz
Oscillator Frequency	f_{OSC}		5	-	44	MHz
Maximum Phase Detector Frequency	f_ϕ		10	-	-	MHz
RF Input Sensitivity	Pf_{IN} RF	V_{CC} = 3.0V	-15	-	+4	dBm
		V_{CC} = 5.0V	-10	-	+4	dBm
IF Input Sensitivity	Pf_{IN} IF	V_{CC} = 2.7V to 5.5V	-10	-	+4	dBm
Oscillator Sensitivity	V_{OSC}	OSC_{IN}	0.5	-	-	V_{P-P}
High Level Input Voltage	V_{IH}	(Note)	$0.8V_{CC}$	-	-	V
Low Level Input Voltage	V_{IL}	(Note)	-	-	$0.2V_{CC}$	V
High Level Input Current	I_{IH}	$V_{IH} = V_{CC}$ = 5.5V (Note)	-1.0	-	1.0	µA
Low Level Input Current	I_{IL}	V_{IL} = 0V, V_{CC} = 5.5V (Note)	-1.0	-	1.0	µA
Oscillator Input Current	I_{IH}	$V_{IH} = V_{CC}$ = 5.5V	-	-	100	µA
Oscillator Input Current	I_{IL}	V_{IL} = 0V, V_{CC} = 5.5V	-100	-	-	µA
High Level Output Voltage	V_{OH}	I_{OH} = -500µA	V_{CC} -0.4	-	-	V
High Level Output Voltage	V_{OH}	I_{OH} = -1mA	-	-	-	V
Low Level Output Voltage	V_{OL}	I_{OL} = 500µA	-	-	0.4	V
Low Level Output Voltage	V_{OL}	I_{OL} = 1mA	-	-	-	V
Data to Clock Set Up Time	t_{CS}	See Data Input Timing	50	-	-	ns
Data to Clock Hold Time	t_{CH}	See Data Input Timing	10	-	-	ns
Clock Pulse Width High	t_{CWH}	See Data Input Timing	50	-	-	ns
Clock Pulse Width Low	t_{CWL}	See Data Input Timing	50	-	-	ns
Clock to Load Enable Set Up Time	t_{ES}	See Data Input Timing	50	-	-	ns
Load Enable Pulse Width	t_{EW}	See Data Input Timing	50	-	-	ns

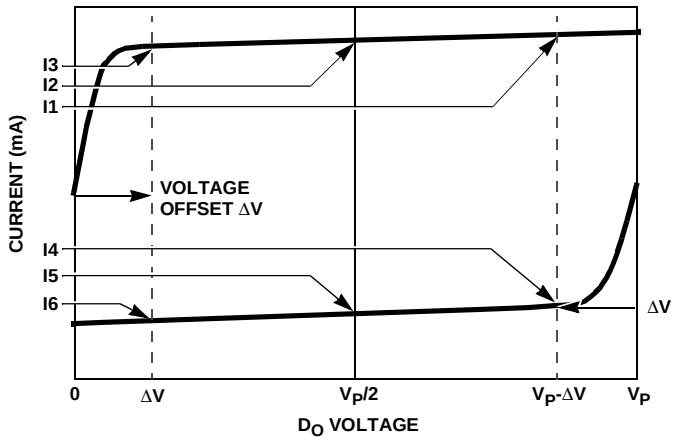
NOTE: Clock, Data and LE does not include f_{IN} RF, f_{IN} IF and OSC_{IN}.

Charge Pump Specifications V_{CC} = 3.0V, V_P = 3.0V, -40°C < T_A < 85°C, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	HFA3524			UNITS
			MIN	TYP	MAX	
Charge Pump Output Current	$I_{DO-SOURCE}$	$V_{DO} = V_P/2$, I_{CPO} = HIGH (Note 4)	-	-5.0	-	mA
	$I_{DO-SINK}$	$V_{DO} = V_P/2$, I_{CPO} = HIGH (Note 4)	-	5.0	-	mA
	$I_{DO-SOURCE}$	$V_{DO} = V_P/2$, I_{CPO} = LOW (Note 4)	-	-1.25	-	mA
	$I_{DO-SINK}$	$V_{DO} = V_P/2$, I_{CPO} = LOW (Note 4)	-	1.25	-	mA
Charge Pump High Z State Current	$I_{DO-HIGH\ Z}$	$0.5V \le V_{DO} \le V_P - 0.5$, -40°C < T < 85°C	-2.5	-	2.5	nA
CP Sink vs Source Mismatch (Note 5)	$I_{DO-SINK}$ vs $I_{DO-SOURCE}$	$V_{DO} = V_P/2$, T_A = 25°C	-	3	10	%
CP Current vs Voltage (Note 6)	I_{DO} vs V_{DO}	$0.5V \le V_{DO} \le V_P - 0.5$, T < 25°C	-	10	15	%
CP Current vs Temperature (Note 7)	I_{DO} vs T	$V_{DO} = V_P/2$, -40°C < T < 85°C	-	10	-	%

NOTES:

4. See Programmable Modes for I_{CPO} description.
5. I_{DO} vs V_{DO} = Charge Pump Output Current magnitude variation vs Voltage = [1/2 •{|I1| - |I3|}]/[1/2 • {|I1| + |I3|}] • 100% and [1/2 • |I4| - |I6|]/[1/2 • {|I4| + |I6|}] • 100%.
6. $I_{DO-SINK}$ vs $I_{DO-SOURCE}$ = Charge Pump Output Current Sink vs Source Mismatch = [|I2| - |I5|]/[1/2 • {|I2| + |I5|}] • 100%.
7. I_{DO} vs T_A = Charge Pump Output Current magnitude variation vs Temperature = [|I2 at temp| - |I2 at 25°C|]/|I2 at 25°C| • 100% and [|I5 at temp| - |I5 at 25°C|]/|I5 at 25°C| • 100%.



I1 = CP sink current at $V_{DO} = V_P - \Delta V$
I2 = CP sink current at $V_{DO} = V_P/2$
I3 = CP sink current at $V_{DO} = \Delta V$
I4 = CP source current at $V_{DO} = V_P - \Delta V$
I5 = CP source current at $V_{DO} = V_P/2$
I6 = CP source current at $V_{DO} = \Delta V$

FIGURE 1. CHARGE PUMP CURRENT SPECIFICATION DEFINITIONS

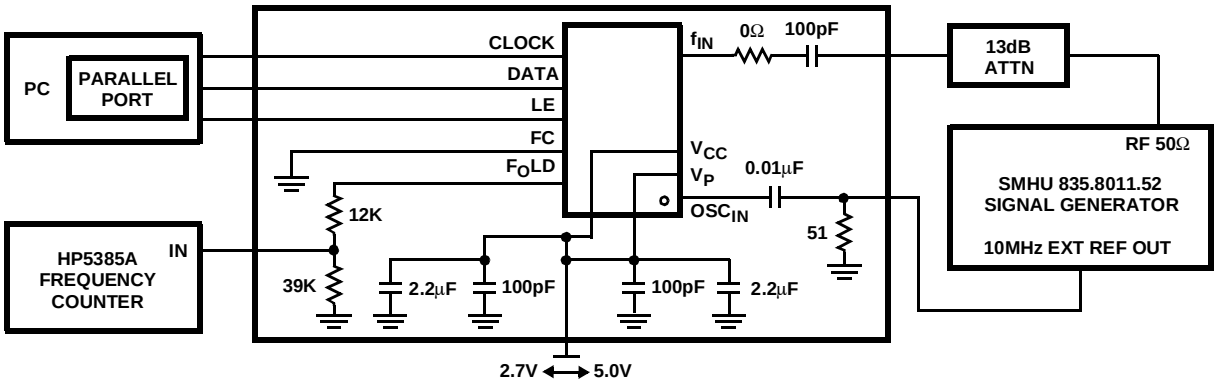


FIGURE 2. RF SENSITIVITY TEST BLOCK DIAGRAM

Typical HFA3524 Performance Curves

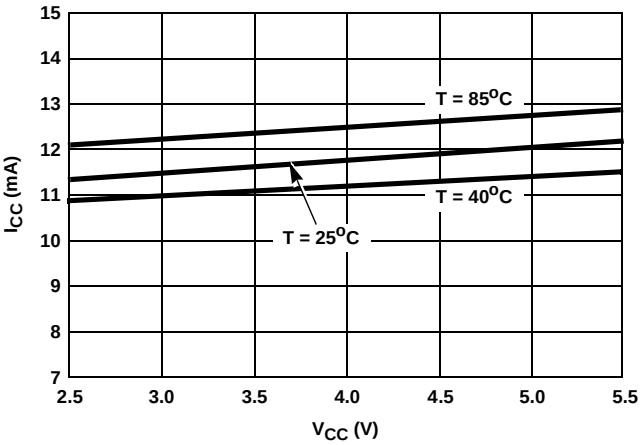


FIGURE 3. I_{CC} vs V_{CC}

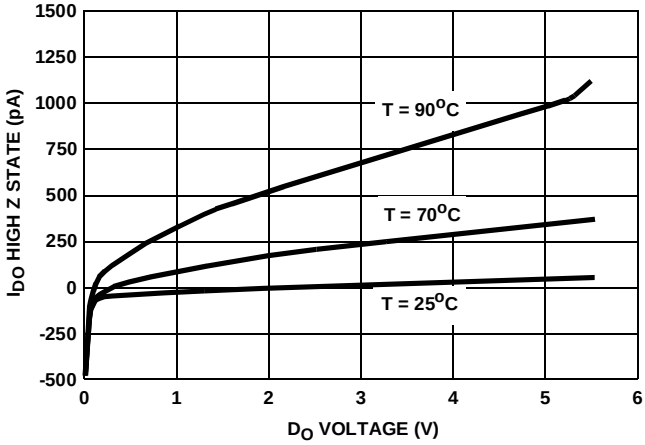


FIGURE 4. I_{DO} HIGH Z STATE vs D_O VOLTAGE

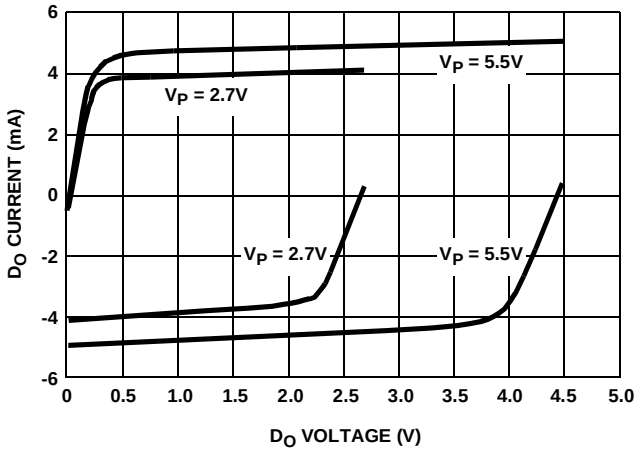


FIGURE 5. CHARGE PUMP CURRENT vs D_O VOLTAGE
I_{CP} = HIGH

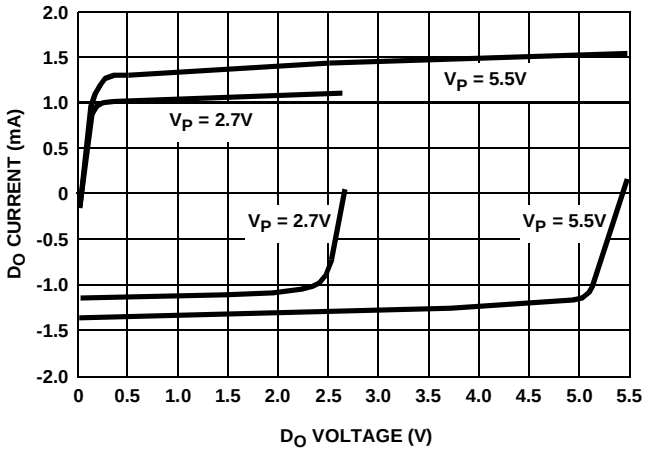
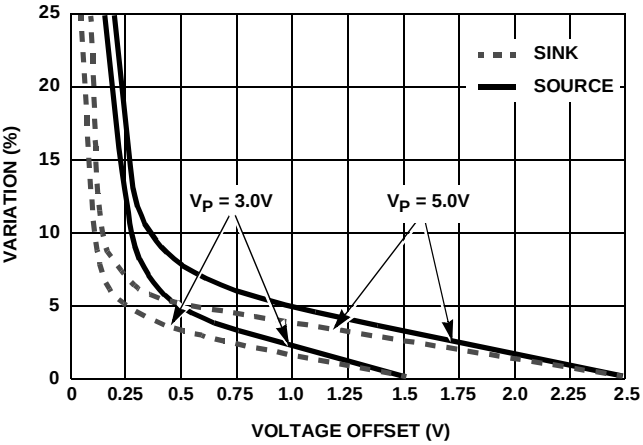


FIGURE 6. CHARGE PUMP CURRENT vs D_O VOLTAGE
I_{CP} = LOW



NOTE: See charge pump current specification definitions.

FIGURE 7. CHARGE PUMP CURRENT VARIATION

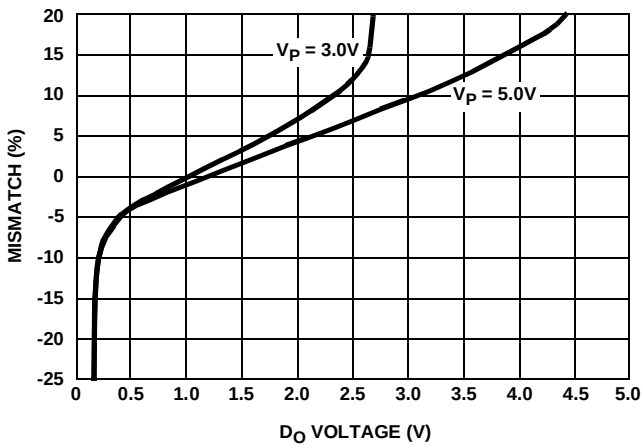
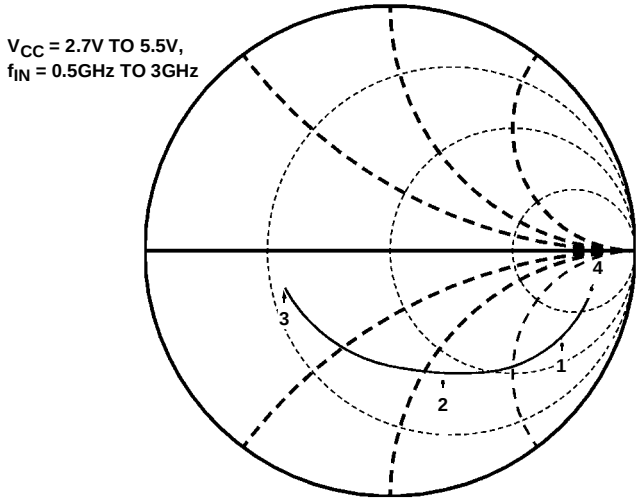


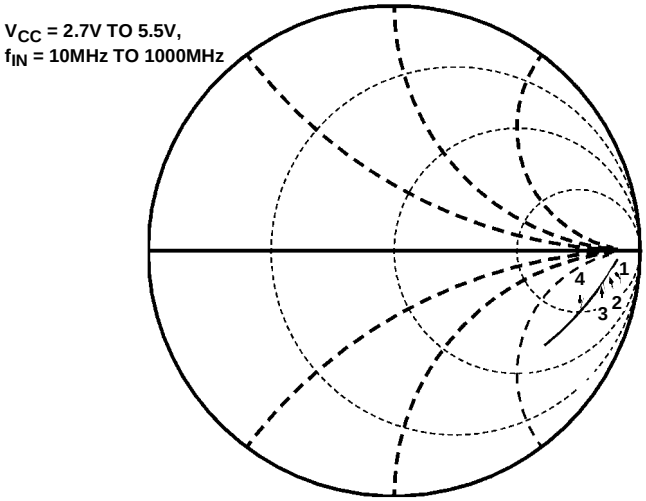
FIGURE 8. SINK vs SOURCE MISMATCH vs D_O VOLTAGE

Typical HFA3524 Performance Curves (Continued)



Marker 1 = 1GHz, Real = 101, Imaginary = -144
Marker 2 = 2GHz, Real = 37, Imaginary = -54
Marker 3 = 3GHz, Real = 22, Imaginary = -2
Marker 4 = 500MHz, Real = 209, Imaginary = -232

FIGURE 9. RF INPUT IMPEDANCE



Marker 1 = 100MHz, Real = 589, Imaginary = -209
Marker 2 = 200MHz, Real = 440, Imaginary = -286
Marker 3 = 300MHz, Real = 326, Imaginary = -287
Marker 4 = 500MHz, Real = 202, Imaginary = -234

FIGURE 10. IF INPUT IMPEDANCE

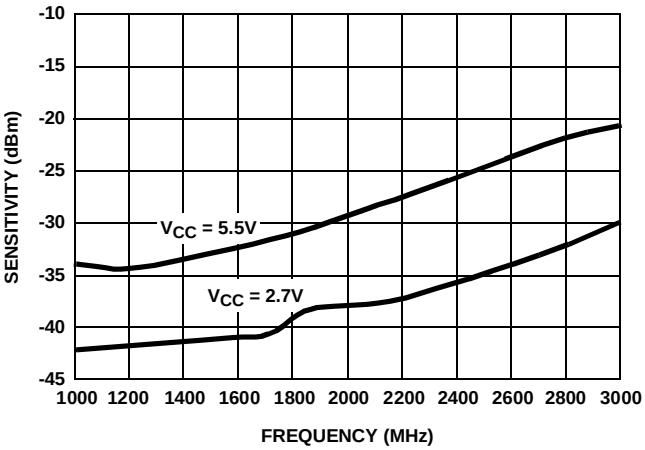


FIGURE 11. RF SENSITIVITY vs FREQUENCY

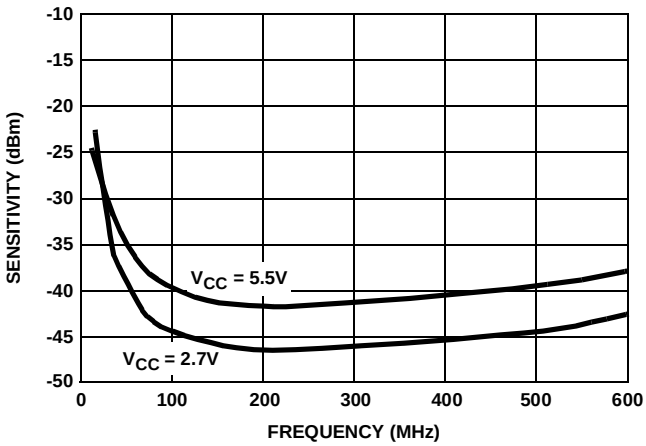


FIGURE 12. IF INPUT SENSITIVITY vs FREQUENCY

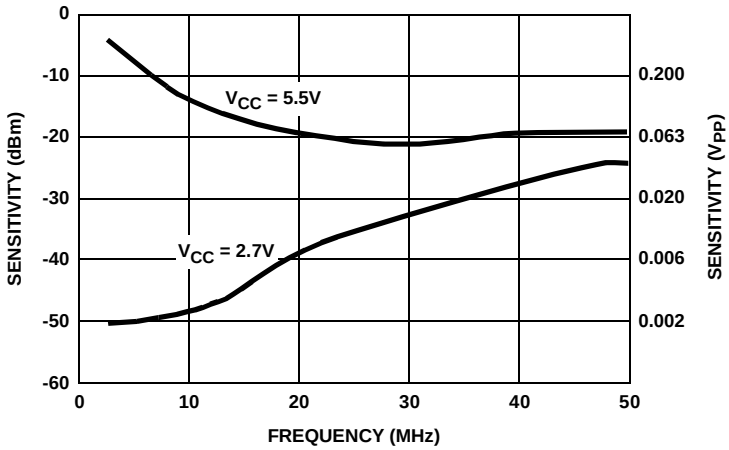


FIGURE 13. OSCILLATOR INPUT SENSITIVITY vs FREQUENCY

Functional Description

The simplified block diagram in Figure 14 shows the 22-bit data register, two 15-bit R Counters and the 15-bit and 18-bit N Counters (intermediate latches are not shown). The data stream is clocked (on the rising edge of Clock) into the DATA input, MSB first. The last two bits are the Control Bus. The DATA is transferred into the counters as follows:

CONTROL BITS		DATA LOCATION
C1	C2	
0	0	IR R Counter
0	1	RF R Counter
1	0	IF N Counter
1	1	RF N Counter

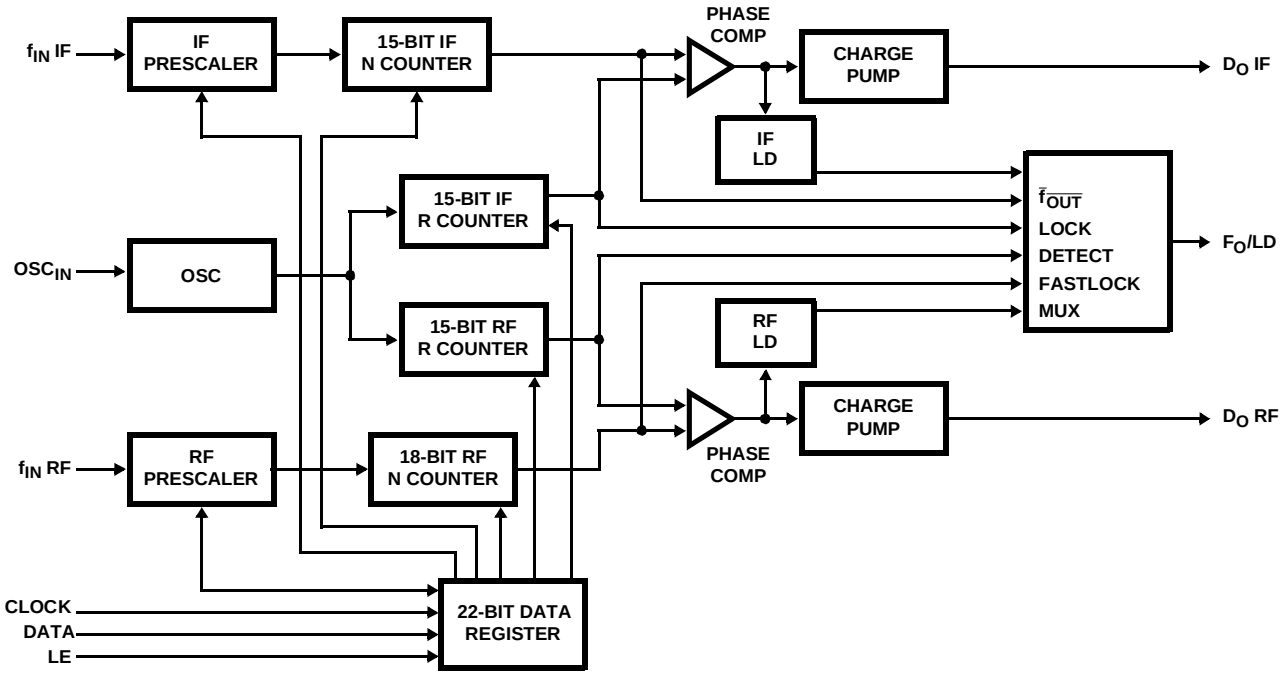
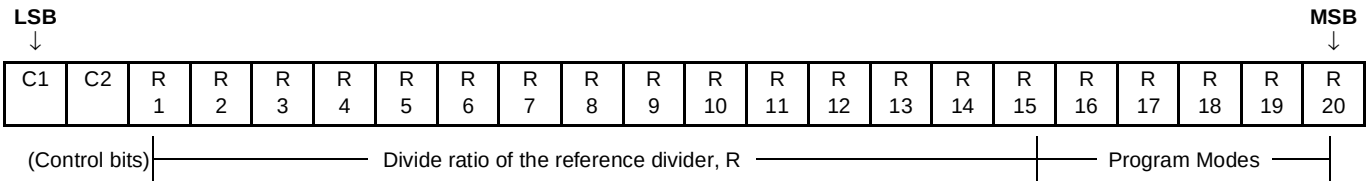


FIGURE 14. SIMPLIFIED BLOCK DIAGRAM

Programmable Reference Dividers (IF and RF R Counters)

If the Control Bits are 00 or 01 (00 for IF and 01 for RF) data is transferred from the 22-bit shift register into a latch which sets the 15-bit R Counter. Serial data format is shown below.



15-BIT PROGRAMMABLE REFERENCE DIVIDER RATIO (R COUNTER)

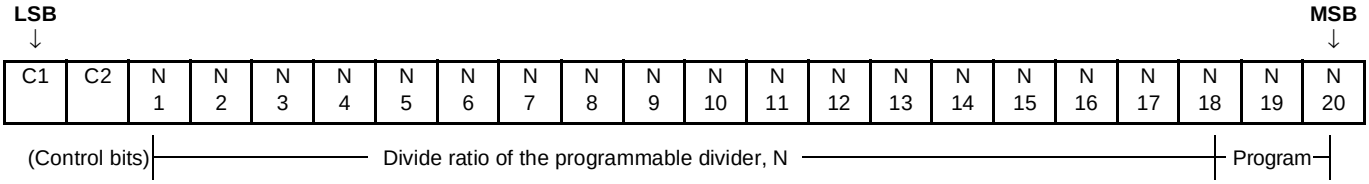
DIVIDE RATIO	R 15	R 14	R 13	R 12	R 11	R 10	R 9	R 8	R 7	R 6	R 5	R 4	R 3	R 2	R 1
3	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
32767	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

NOTES:

8. Divide ratios less than 3 are prohibited.
9. Divide ratio: 3 to 32767.
10. R1 to R15: These bits select the divide ratio of the programmable reference divider.
11. Data is shifted in MSB first.

Programmable Divide (N Counter)

The N counter consists of the 7-bit swallow counter (A counter) and the 11-bit programmable counter (B counter). If the Control Bits are 10 or 11 (10 for IF counter and 11 for RF counter) data is transferred from the 22-bit shift register into a 4-bit or 7-bit latch (which sets the Swallow (A) Counter) and an 11-bit latch (which sets the 11-bit programmable (B) Counter), MSB first. Serial data format is shown below. For the IF N counter bits 5, 6, and 7 are don't care bits. The RF N counter does not have don't care bits.



7-Bit Swallow Counter Divide Ratio (A Counter)

RF

DIVIDE RATIO A	N 7	N 6	N 5	N 4	N 3	N 2	N 1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
•	•	•	•	•	•	•	•
127	1	1	1	1	1	1	1

NOTES:

12. Divide ratio 0 to 127.

13. B ≥ A.

IF

DIVIDE RATIO A	N 7	N 6	N 5	N 4	N 3	N 2	N 1
0	X	X	X	0	0	0	0
1	X	X	X	0	0	0	1
•	•	•	•	•	•	•	•
15	X	X	X	1	1	1	1

X = Don't care condition.

11-BIT PROGRAMMABLE COUNTER DIVIDE RATIO (B COUNTER

DIVIDE RATIO B	N 18	N 17	N 16	N 15	N 14	N 13	N 12	N 11	N 10	N 9	N 8
3	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	1	0	0
•	•	•	•	•	•	•	•	•	•	•	•
2047	1	1	1	1	1	1	1	1	1	1	1

NOTES:

14. Divide ratio 3 to 2047 (divide ratios less than 3 are prohibited).

15. B ≥ A.

Pulse Swallow Function

$f_{VCO} = [(P \times B) + A] \times f_{OSC}/R$

f_{VCO}: Output frequency of external voltage controlled oscillator (VCO)

B: Preset divide ratio of binary 11-bit programmable counter (3 to 2047)

A: Preset divide ratio of binary 7-bit swallow counter ($0 \le A \le 127$ {RF}, $0 \le A \le 15$ {IF}, $A \le B$)

f_{OSC}: Output frequency of the external reference frequency oscillator

R: Preset divide ratio of binary 15-bit programmable reference counter (3 to 32767)

P: Preset modulus of dual modulus prescaler (for IF: P = 8 or 16; for RF: P = 32 or 64)

Programmable Modes

Several modes of operation can be programmed with bits R16-R19 including the phase detector polarity, charge pump High Z State and the output of the F_O/LD pin. The prescaler and powerdown modes are selected with bits N19 and N20. The programmable modes are shown in Table 1. Truth table for the programmable modes and F_O/LD output are shown in Table 2 and Table 3.

TABLE 1. PROGRAMMABLE MODES

C1	C2	R16	R17	R18	R19	R20
0	0	IF Phase Detector Polarity	IF I_{CPO}	IF D_O High Z	IF LD	IF F_O
0	1	RF Phase Detector Polarity	RF I_{CPO}	RF D_O High Z	RF LD	RF F_O

C1	C2	N19	N20
1	0	IF Prescaler	Powerdown IF
1	1	RF Prescaler	Powerdown RF

TABLE 2. MODE SELECT TRUTH TABLE

	ΦD POLARITY	D_O HIGH Z STATE	(NOTE 16) I_{CPO}	IF PRESCALER	RF PRESCALER	(NOTE 17) POWERDOWN
0	Negative	Normal Operation	LOW	8/9	32/33	Powered Up
1	Positive	High Z State	HIGH	16/17	64/65	Powered Down

NOTES:

16. The I_{CPO} LOW current state = 1/4 x I_{CPO} HIGH current.

17. Activation of the IF PLL or RF PLL powerdown modes result in the disabling of the respective N counter divider and debiasing of its respective f_{IN} inputs (to a high impedance state). Powerdown forces the respective charge pump and phase comparator logic to a High Z State condition. The R counter functionality does not become disabled until both IF and RF powerdown bits are activated. The OSC_{IN} pin reverts to a high impedance state when this condition exists. The control register remains active and capable of loading and latching in data during all of the powerdown modes.

TABLE 3. THE F_O/LD (PIN 10) OUTPUT TRUTH TABLE

RF R [19] (RF LD)	IF R [19] (IF LD)	RF R [20] (RF F_O)	IF R [20] (IF F_O)	F_O OUTPUT STATE
0	0	0	0	Disabled (Note 18)
0	1	0	0	IF Lock Detect (Note 19)
1	0	0	0	RF Lock Detect (Note 19)
1	1	0	0	RF/IF Lock Detect (Note 19)
X	0	0	1	IF Reference Divider Output
X	0	1	0	RF Reference Divider Output
X	1	0	1	IF Programmable Divider Output
X	1	1	0	RF Programmable Divider Output
0	0	1	1	Fastlock (Note 20)
0	1	1	1	For Internal Use Only
1	0	1	1	For Internal Use Only
1	1	1	1	For Internal Use Only
1	1	1	1	Counter Reset (Note 21)

X = Don't care condition

NOTES:

18. When the F_O/LD output is disabled, it is actively pulled to a low logic state.

19. Lock detect output provided to indicate when the VCO frequency is in "lock". When the loop is locked and a lock detect mode is selected, the pins output is HIGH, with narrow pulses LOW. In the RF/IF lock detect mode a locked condition is indicated when RF and IF are both locked.

20. The Fastlock mode utilizes the F_O/LD output pin to switch a second loop filter damping resistor to ground during fastlock operation. Activation of Fastlock occurs whenever the RF loop's lcpo magnitude bit #17 is selected HIGH (while the #19 and #20 mode bits are set for Fastlock).

21. The Counter Reset mode bits R19 and R20 when activated reset all counters. Upon removal of the Reset bits, the N counter resumes counting in "close" alignment with the R counter. (The maximum error is one prescaler cycle.) If the Reset bits are activated, the R counter is also forced to Reset, allowing smooth acquisition upon powering up.

Phase Detector Polarity

Depending upon VCO characteristics, R16 bit should be set accordingly, (see Figure 15).

- When VCO characteristics are positive like (1), R16 should be set HIGH.
- When VCO characteristics are negative like (2), R16 should be set LOW.

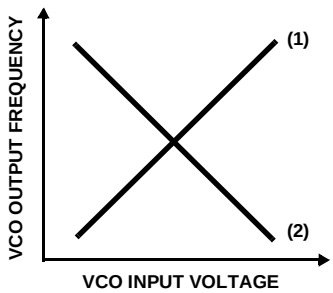
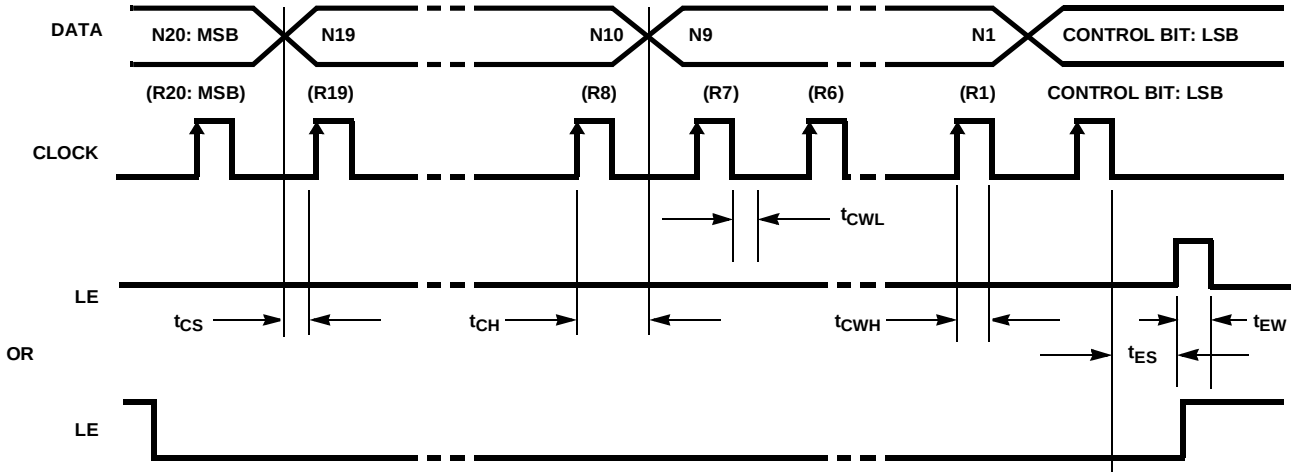


FIGURE 15. VCO CHARACTERISTICS



NOTES:

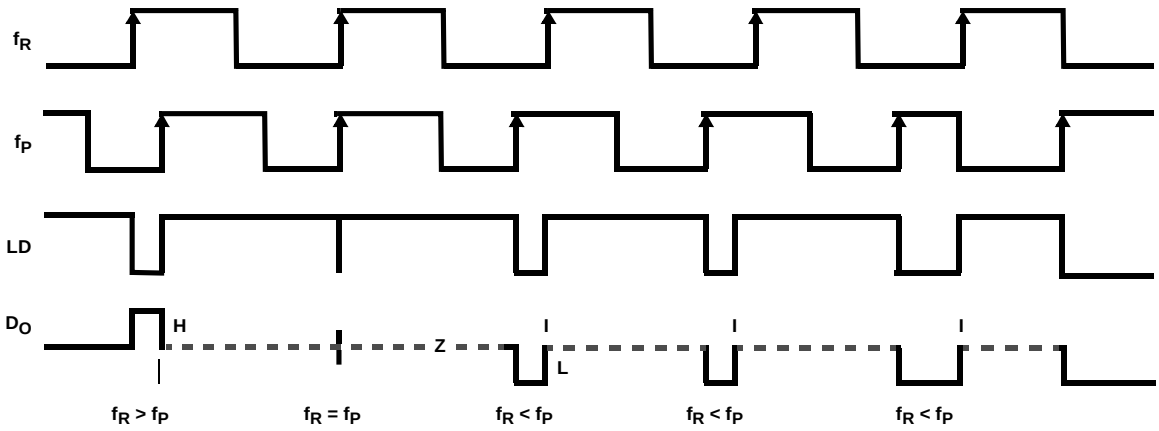
22. Parenthesis data indicates programmable reference divider data.

23. Data shifted into register on clock rising edge.

24. Data is shifted in MSB first.

Test Conditions: The Serial Data Input Timing is tested using a symmetrical waveform around $V_{CC}/2$. The test waveform has an edge rate of 0.6V/ns with amplitudes of 2.2V at V_{CC} = 2.7V and 2.6V at V_{CC} = 5.5V.

FIGURE 16. SERIAL DATA INPUT TIMING



NOTES:

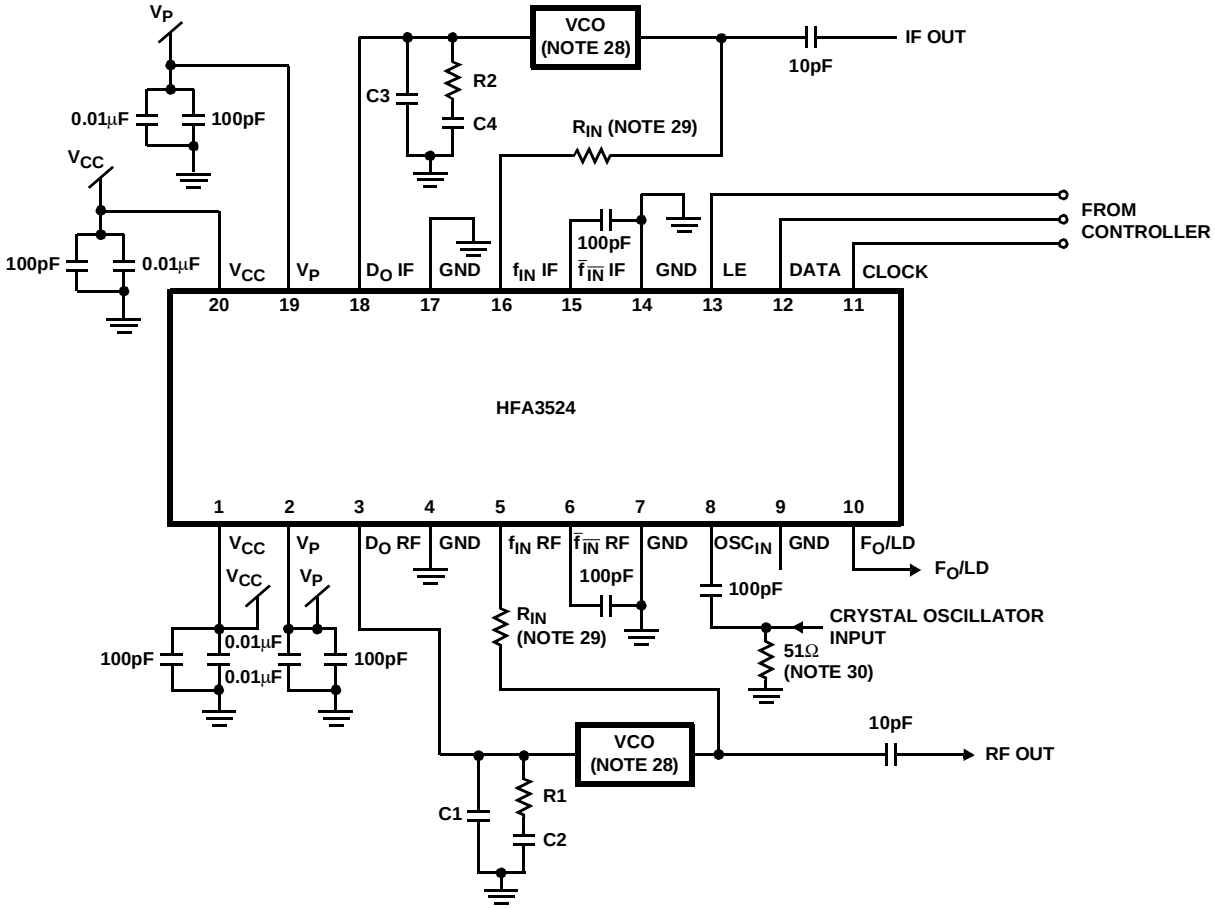
25. Phase difference detection range: -2π to $+2\pi$

26. The minimum width pump up and pump down current pulses occur at the D_O pin when the loop is locked.

27. R16 = HIGH.

FIGURE 17. PHASE COMPARATOR AND INTERNAL CHARGE PUMP CHARACTERISTICS

Typical Application Example



NOTES:

28. VCO is assumed AC coupled.
29. R_{IN} increases impedance so that VCO output power is provided to the load rather than the PLL. Typical values are 10Ω to 200Ω depending on the VCO power level. f_{IN} RF impedance ranges from 40Ω to 100Ω. f_{IN} IF impedances are higher.
30. 50Ω termination is often used on test boards to allow use of external reference oscillator. For most typical products a CMOS clock is used and no terminating resistor is required. OSC_{IN} may be AC or DC coupled. AC coupling is recommended because the input circuit provides its own bias (see Figure 16).
31. Proper use of grounds and bypass capacitors is essential to achieve a high level of performance. Crosstalk between pins can be reduced by careful board layout.
32. This is a static sensitive device. It should be handled only at static free work stations.

FIGURE 18.

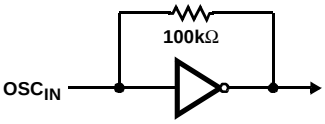


FIGURE 19.

Typical Locked Detect Circuit

A lock detect circuit is needed in order to provide a steady LOW signal when the PLL is in the locked state. A typical circuit is shown in Figure 20.

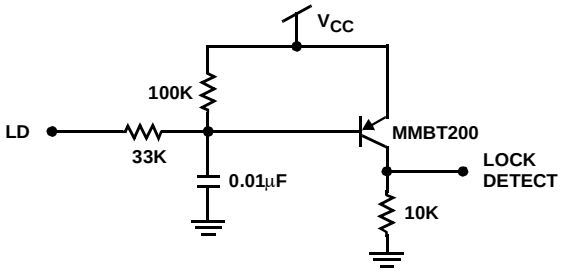


FIGURE 20.

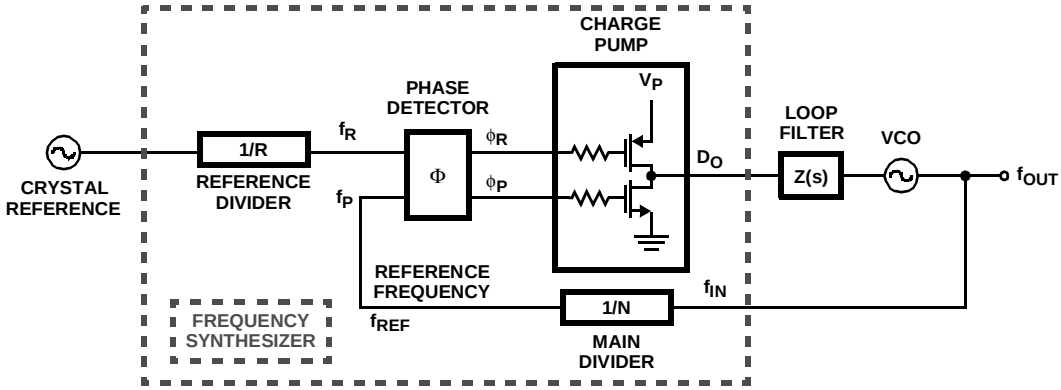


FIGURE 21. BASIC CHARGE PUMP PHASE LOCKED LOOP

Application Information

A block diagram of the basic phase locked loop is shown in Figure 21.

Loop Gain Equations

A linear control system model of the phase feedback for a PLL in the locked state is shown in Figure 22. The open loop gain is the product of the phase comparator gain ($K\phi$), the VCO gain (K_{VCO}/s), and the loop filter gain Z(s) divided by the gain of the feedback counter modulus (N). The passive loop filter configuration used is displayed in Figure 23, while the complex impedance of the filter is given in Equation 2.

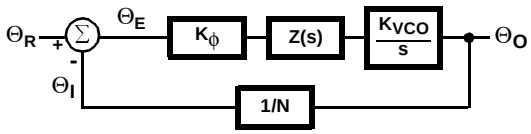


FIGURE 22. PLL LINEAR MODEL

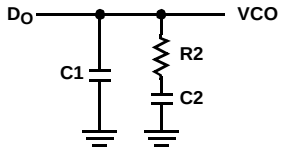


FIGURE 23. PASSIVE LOOP FILTER

$$\text{Open loop gain} = H(s)\,G(s) = \Theta_I/\Theta_E = K_\phi\,Z(s)\,K_{VCO}/Ns \quad \text{(EQ. 1)}$$

$$Z(s) = \frac{s(C2 \bullet R2) + 1}{s^2(C1 \bullet C2 \bullet R2) + sC1 + sC2} \quad \text{(EQ. 2)}$$

The time constants which determine the pole and zero frequencies of the filter transfer function can be defined as:

$$T1 = R2 \bullet \frac{C1 \bullet C2}{C1 + C2} \quad \text{(EQ. 3A)}$$

and

$$T2 = R2 \bullet C2 \quad \text{(EQ. 3B)}$$

The 3rd order PLL Open Loop Gain can be calculated in terms of frequency, ω, the filter time constants T1 and T2, and the design constants K_ϕ, K_{VCO}, and N.

$$|G(s) \bullet H(s)|_{s = j \bullet w} = \frac{-K\phi \bullet K_{VCO}(1 + j\omega \bullet T2)}{\omega^2 C1 \bullet N(1 + j\omega \bullet T1)} \bullet \frac{T1}{T2} \quad \text{(EQ. 4)}$$

From Equation 3 we can see that the phase term will be dependent on the single pole and zero such that the phase margin is determined in Equation 5.

$$\phi(\omega) = \tan^{-1}(\omega \bullet T2) - \tan^{-1}(\omega \bullet T1) + 180^o \quad \text{(EQ. 5)}$$

A plot of the magnitude and phase of G(s)H(s) for a stable loop, is shown in Figure 24 with a solid trace. The parameter ϕ_P shows the amount of phase margin that exists at the point the gain drops below zero (the cutoff frequency wp of the loop). In a critically damped system, the amount of phase margin would be approximately 45 degrees.

If we were now to redefine the cut off frequency, wp', as double the frequency which gave us our original loop bandwidth, wp, the loop response time would be approximately halved. Because the filter attenuation at the comparison frequency also diminishes, the spurs would have increased by approximately 6dB. In the proposed Fastlock scheme, the higher spur levels and wider loop filter conditions would exist only during the initial lock-on phase - just long enough to reap the benefits of locking faster. The objective would be to open up the loop bandwidth but not introduce any additional complications or compromises related to our original design criteria. We would ideally like to momentarily shift the curve of Figure 24 over to a different cutoff frequency, illustrated by the dotted line, without affecting the relative open loop gain and phase relationships. To maintain the same gain/phase relationship at twice the original cutoff frequency, other terms in the gain and phase Equations 4 and 5 will have to compensate by the corresponding "1/w" or "$1/w^2$" factor. Examination of Equations 3 and 5 indicates the damping resistor variable R2 could be chosen to compensate the "w" terms for the phase margin. This implies that another resistor of equal value to R2 will need to be switched in

parallel with R2 during the initial lock period. We must also insure that the magnitude of the open loop gain, H(s)G(s) is equal to zero at wp' = 2wp. K_{VCO}, Kϕ, N, or the net product of these terms can be changed by a factor of 4, to counteract the w^2 term present in the denominator of Equation 3. The Kϕ term was chosen to complete the transformation because it can readily be switched between 1X and 4X values. This is accomplished by increasing the charge pump output current from 1mA in the standard mode to 4mA in Fastlock.

Fastlock Circuit Implementation

A diagram of the Fastlock scheme as implemented in Intersil Corporations HFA3524 PLL is shown in Figure 25. When a new frequency is loaded, and the RF Icp_O bit is set high, the charge pump circuit receives an input to deliver 4 times the normal current per unit phase error while an open drain NMOS on chip device switches in a second R2 resistor element to ground. The user calculates the loop filter component values for the normal steady state considerations. The device configuration ensures that as long as a second identical damping resistor is wired in appropriately, the loop will lock faster without any additional stability considerations to account for. Once locked on the correct frequency, the user can return the PLL to standard low noise operation by sending an instruction with the RF Icp_O bit set low. This transition does not affect the charge on the loop filter capacitors and is enacted synchronous with the charge pump output. This creates a nearly seamless change between Fastlock and standard mode.

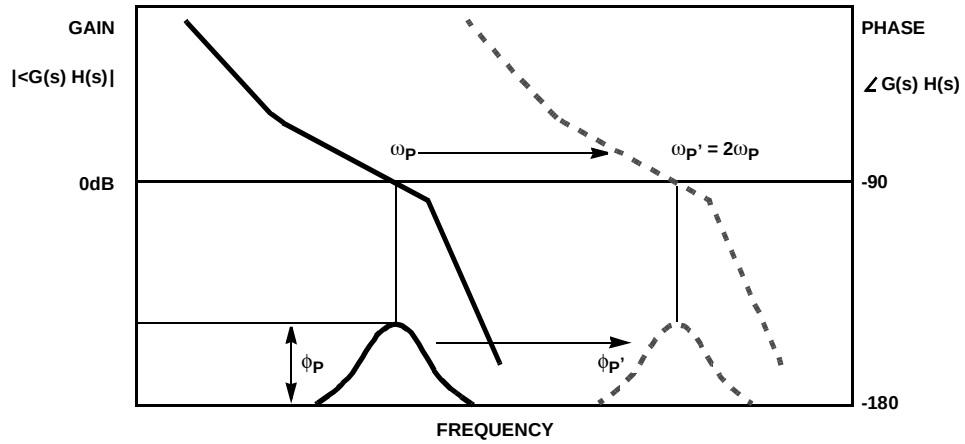


FIGURE 24. OPEN LOOP RESPONSE BODE PLOT

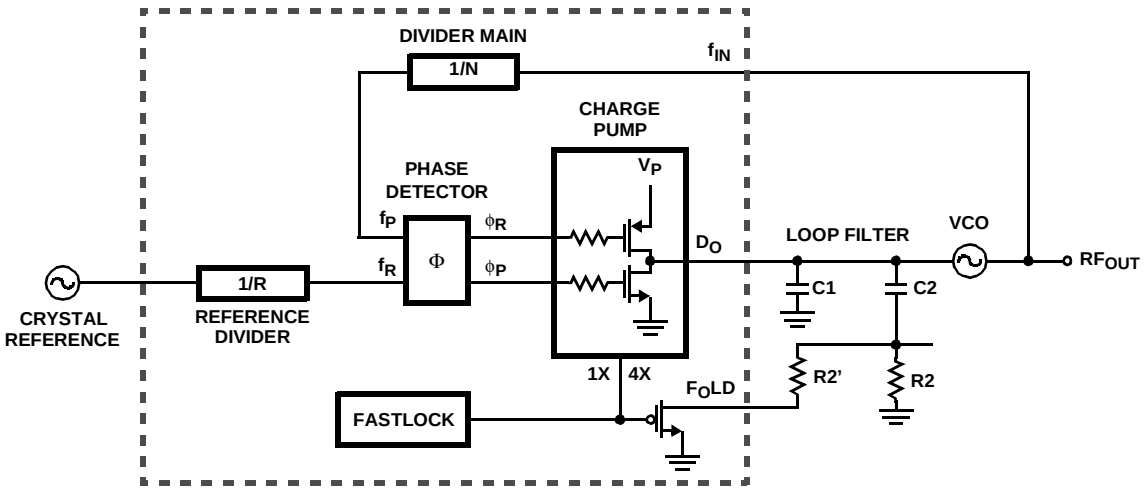


FIGURE 25. FASTLOCK CIRCUIT IMPLEMENTATION