



# 400ksps, +5V, 8-/4-Channel, 10-Bit ADCs with +2.5V Reference and Parallel Interface

**MAX1060/MAX1064**

## General Description

The MAX1060/MAX1064 low-power, 10-bit analog-to-digital converters (ADCs) feature a successive-approximation ADC, automatic power-down, fast wake-up (2 $\mu$ s), an on-chip clock, +2.5V internal reference, and a high-speed, byte-wide parallel interface. The devices operate with a single +5V analog supply and feature a V<sub>LOGIC</sub> pin that allows them to interface directly with a +2.7V to +5.5V digital supply.

Power consumption is only 10mW (V<sub>DD</sub> = V<sub>LOGIC</sub>) at a 400ksps max sampling rate. Two software-selectable power-down modes enable the MAX1060/MAX1064 to be shut down between conversions; accessing the parallel interface returns them to normal operation. Powering down between conversions can cut supply current to under 10 $\mu$ A at reduced sampling rates.

Both devices offer software-configurable analog inputs for unipolar/bipolar and single-ended/pseudo-differential operation. In single-ended mode, the MAX1060 has eight input channels and the MAX1064 has four input channels (four and two input channels, respectively, when in pseudo-differential mode).

Excellent dynamic performance and low power, combined with ease of use and small package size, make these converters ideal for battery-powered and data-acquisition applications or for other circuits with demanding power consumption and space requirements.

The MAX1060 is available in a 28-pin QSOP package, while the MAX1064 comes in a 24-pin QSOP. For pin-compatible +3V, 10-bit versions, refer to the MAX1061/MAX1063 data sheet.

## Applications

Industrial Control Systems	Data Logging
Energy Management	Patient Monitoring
Data-Acquisition Systems	Touch Screens

## Ordering Information

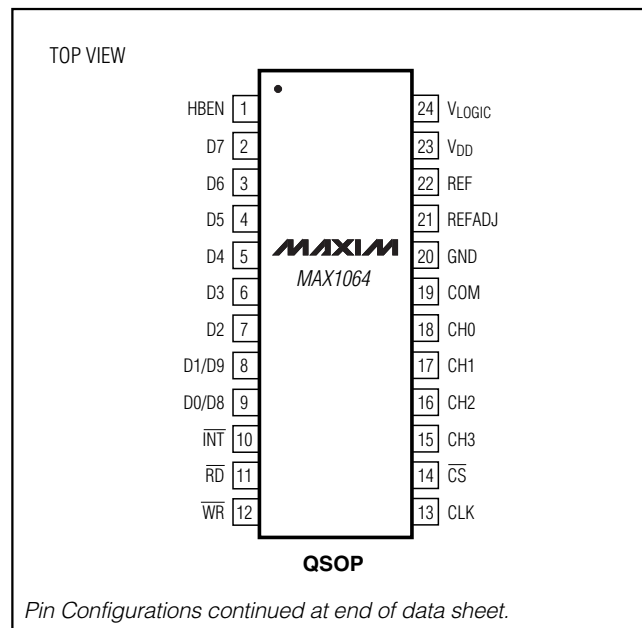
PART	TEMP RANGE	PIN-PACKAGE	INL (LSB)
MAX1060ACEI	0°C to +70°C	28 QSOP	$\pm 0.5$
MAX1060BCEI	0°C to +70°C	28 QSOP	$\pm 1$
MAX1060AEEI	-40°C to +85°C	28 QSOP	$\pm 0.5$
MAX1060BEEI	-40°C to +85°C	28 QSOP	$\pm 1$

Ordering Information continued at end of data sheet.

## Features

- ◆ 10-Bit Resolution,  $\pm 0.5$  LSB Linearity
- ◆ +5V Single-Supply Operation
- ◆ User-Adjustable Logic Level (+2.7V to +5.5V)
- ◆ Internal +2.5V Reference
- ◆ Software-Configurable Analog Input Multiplexer
  - 8-Channel Single Ended/
  - 4-Channel Pseudo-Differential (MAX1060)
  - 4-Channel Single Ended/
  - 2-Channel Pseudo-Differential (MAX1064)
- ◆ Software-Configurable Unipolar/Bipolar Analog Inputs
- ◆ Low Current
  - 2.5mA (400ksps)
  - 1.0mA (100ksps)
  - 400 $\mu$ A (10ksps)
  - 2 $\mu$ A (Shutdown)
- ◆ Internal 6MHz Full-Power Bandwidth Track/Hold
- ◆ Byte-Wide Parallel (8 + 2) Interface
- ◆ Small Footprint
  - 28-Pin QSOP (MAX1060)
  - 24-Pin QSOP (MAX1064)

## Pin Configurations



# 400ksps, +5V, 8-/4-Channel, 10-Bit ADCs with +2.5V Reference and Parallel Interface

## ABSOLUTE MAXIMUM RATINGS

V <sub>DD</sub> to GND .....	-0.3V to +6V	Continuous Power Dissipation (T <sub>A</sub> = +70°C)	
V <sub>LOGIC</sub> to GND .....	-0.3V to +6V	24-Pin QSOP (derate 9.5mW/°C above +70°C).....	762mW
CH0-CH7, COM to GND .....	-0.3V to (V <sub>DD</sub> + 0.3V)	28-Pin QSOP (derate 8.0mW/°C above +70°C).....	667mW
REF, REFADJ to GND.....	-0.3V to (V <sub>DD</sub> + 0.3V)	Operating Temperature Ranges	
Digital Inputs to GND .....	-0.3V to +6V	MAX1060_C_/MAX1064_C_ .....	0°C to +70°C
Digital Outputs (D0-D9, INT) to GND .....	-0.3V to (V <sub>LOGIC</sub> + 0.3V)	MAX1060_E_/MAX1064_E_ .....	-40°C to +85°C
		Storage Temperature Range .....	-65°C to +150°C
		Lead Temperature (soldering, 10s) .....	+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

(V<sub>DD</sub> = V<sub>LOGIC</sub> = +5V ±10%, COM = GND, REFADJ = V<sub>DD</sub>, V<sub>REF</sub> = +2.5V, 4.7μF capacitor at REF pin, f<sub>CLK</sub> = 7.6MHz (50% duty cycle), T<sub>A</sub> = T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
<b>DC ACCURACY</b> (Note 1)							
Resolution	RES		10			Bits	
Relative Accuracy (Note 2)	INL	MAX106_A			±0.5	LSB	
		MAX106_B			±1		
Differential Nonlinearity	DNL	No missing codes over temperature			±1	LSB	
Offset Error					±2	LSB	
Gain Error		(Note 3)			±2	LSB	
Gain Temperature Coefficient				±2.0		ppm/°C	
Channel-to-Channel Offset Matching				±0.1		LSB	
<b>DYNAMIC SPECIFICATIONS</b> (f <sub>IN(sine wave)</sub> = 50kHz, V <sub>IN</sub> = 2.5V <sub>P-P</sub> , 400ksps, external f <sub>CLK</sub> = 7.6MHz, bipolar input mode)							
Signal-to-Noise Plus Distortion	SINAD			60		dB	
Total Harmonic Distortion (Including 5th-Order Harmonic)	THD			-72		dB	
Spurious-Free Dynamic Range	SFDR			72		dB	
Intermodulation Distortion	IMD	f <sub>IN1</sub> = 49kHz, f <sub>IN2</sub> = 52kHz		76		dB	
Channel-to-Channel Crosstalk		f <sub>IN</sub> = 175kHz, V <sub>IN</sub> = 2.5V <sub>P-P</sub> (Note 4)		-78		dB	
Full-Linear Bandwidth		SINAD > 56dB		350		kHz	
Full-Power Bandwidth		-3dB rolloff		6		MHz	
<b>CONVERSION RATE</b>							
Conversion Time (Note 5)	t <sub>CONV</sub>	External clock mode		2.1		μs	
		External acquisition/internal clock mode		2.5	3.0		3.5
		Internal acquisition/internal clock mode		3.2	3.6		4
T/H Acquisition Time	t <sub>ACQ</sub>				400	ns	
Aperture Delay		External acquisition or external clock mode		25		ns	
Aperture Jitter		External acquisition or external clock mode		<50		ps	
		Internal acquisition/internal clock mode		<200			
External Clock Frequency	f <sub>CLK</sub>		0.1		7.6	MHz	
Duty Cycle			30		70	%	

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MAX1060/MAX1064

## ELECTRICAL CHARACTERISTICS (continued)

( $V_{DD} = V_{LOGIC} = +5V \pm 10\%$ ,  $COM = GND$ ,  $REFADJ = V_{DD}$ ,  $V_{REF} = +2.5V$ ,  $4.7\mu F$  capacitor at REF pin,  $f_{CLK} = 7.6MHz$  (50% duty cycle),  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ C$ .)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>ANALOG INPUTS</b>						
Analog Input Voltage Range, Single Ended and Differential (Note 6)	$V_{IN}$	Unipolar, $V_{COM} = 0$	0		$V_{REF}$	V
		Bipolar, $V_{COM} = V_{REF} / 2$	$-V_{REF} / 2$		$+V_{REF} / 2$	
Multiplexer Leakage Current		On-/off-leakage current, $V_{IN} = 0$ or $V_{DD}$		$\pm 0.01$	$\pm 1$	$\mu A$
Input Capacitance	$C_{IN}$			12		pF
<b>INTERNAL REFERENCE</b>						
REF Output Voltage			2.49	2.5	2.51	V
REF Short-Circuit Current				15		mA
REF Temperature Coefficient	$TC_{REF}$	$T_A = 0^\circ C$ to $+70^\circ C$		$\pm 20$		ppm/ $^\circ C$
REFADJ Input Range		For small adjustments		$\pm 100$		mV
REFADJ High Threshold		To power down the internal reference	$V_{DD} - 1.0$			V
Load Regulation		0 to 0.5mA output load (Note 7)		0.2		mV/mA
Capacitive Bypass at REFADJ				0.01	1	$\mu F$
Capacitive Bypass at REF			4.7		10	$\mu F$
<b>EXTERNAL REFERENCE AT REF</b>						
REF Input Voltage Range	$V_{REF}$		1.0		$V_{DD} + 50mV$	V
Shutdown REF Input Current	$I_{REF}$	$V_{REF} = 2.5V$ , $f_{SAMPLE} = 400ksps$		200	300	$\mu A$
		Shutdown mode			2	
<b>DIGITAL INPUTS AND OUTPUTS</b>						
Input Voltage High	$V_{IH}$	$V_{LOGIC} = 4.5V$	4.0			V
		$V_{LOGIC} = 2.7V$	2.0			
Input Voltage Low	$V_{IL}$	$V_{LOGIC} = 4.5V$ or $2.7V$			0.8	V
Input Hysteresis	$V_{HYS}$			200		mV
Input Leakage Current	$I_{IN}$	$V_{IN} = 0$ or $V_{DD}$		$\pm 0.1$	$\pm 1$	$\mu A$
Input Capacitance	$C_{IN}$			15		pF
Output Voltage Low	$V_{OL}$	$I_{SINK} = 1.6mA$			0.4	V
Output Voltage High	$V_{OH}$	$I_{SOURCE} = 1mA$	$V_{LOGIC} - 0.5$			V
Tri-State Leakage Current	$I_{LEAKAGE}$	$\overline{CS} = V_{DD}$		$\pm 0.1$	$\pm 1$	$\mu A$
Tri-State Output Capacitance	$C_{OUT}$	$\overline{CS} = V_{DD}$		15		pF

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## ELECTRICAL CHARACTERISTICS (continued)

( $V_{DD} = V_{LOGIC} = +5V \pm 10\%$ ,  $COM = GND$ ,  $REFADJ = V_{DD}$ ,  $V_{REF} = +2.5V$ ,  $4.7\mu F$  capacitor at REF pin,  $f_{CLK} = 7.6MHz$  (50% duty cycle),  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ C$ .)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
<b>POWER REQUIREMENTS</b>							
Analog Supply Voltage	$V_{DD}$			4.5		5.5	V
Digital Supply Voltage	$V_{LOGIC}$			2.7		$V_{DD} + 0.3$	V
Positive Supply Current	$I_{DD}$	Operating mode, $f_{SAMPLE} = 400ksps$	Internal reference		2.9	3.4	mA
			External reference		2.5	2.9	
		Standby mode	Internal reference		1.0	1.2	
			External reference		0.5	0.8	
Shutdown mode				2	10	$\mu A$	
$V_{LOGIC}$ Current	$I_{LOGIC}$	$C_L = 20pF$	$f_{SAMPLE} = 400ksps$			200	$\mu A$
			Nonconverting		2	10	
Power-Supply Rejection	PSR	$V_{DD} = 5V \pm 10\%$ , full-scale input			$\pm 0.3$	$\pm 0.9$	mV

## TIMING CHARACTERISTICS

( $V_{DD} = V_{LOGIC} = +5V \pm 10\%$ ,  $COM = GND$ ,  $REFADJ = V_{DD}$ ,  $V_{REF} = +2.5V$ ,  $4.7\mu F$  capacitor at REF pin,  $f_{CLK} = 7.6MHz$  (50% duty cycle),  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ C$ .)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CLK Period	$t_{CP}$		132			ns
CLK Pulse Width High	$t_{CH}$		40			ns
CLK Pulse Width Low	$t_{CL}$		40			ns
Data Valid to $\overline{WR}$ Rise Time	$t_{DS}$		40			ns
$\overline{WR}$ Rise to Data Valid Hold Time	$t_{DH}$		0			ns
$\overline{WR}$ to CLK Fall Setup Time	$t_{CWS}$		40			ns
CLK Fall to $\overline{WR}$ Hold Time	$t_{CWH}$		40			ns
$\overline{CS}$ to CLK or $\overline{WR}$ Setup Time	$t_{CSWS}$		60			ns
CLK or $\overline{WR}$ to $\overline{CS}$ Hold Time	$t_{CSWH}$		0			ns
$\overline{CS}$ Pulse Width	$t_{CS}$		100			ns
$\overline{WR}$ Pulse Width	$t_{WR}$	(Note 8)	60			ns

# 400ksps, +5V, 8-/4-Channel, 10-Bit ADCs with +2.5V Reference and Parallel Interface

MAX1060/MAX1064

## TIMING CHARACTERISTICS (continued)

( $V_{DD} = V_{LOGIC} = +5V \pm 10\%$ ,  $COM = GND$ ,  $REFADJ = V_{DD}$ ,  $V_{REF} = +2.5V$ ,  $4.7\mu F$  capacitor at REF pin,  $f_{CLK} = 7.6MHz$  (50% duty cycle),  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ C$ .)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{CS}$ Rise to Output Disable	$t_{TC}$	$C_{LOAD} = 20pF$ , Figure 1	10		60	ns
$\overline{RD}$ Rise to Output Disable	$t_{TR}$	$C_{LOAD} = 20pF$ , Figure 1	10		40	ns
$\overline{RD}$ Fall to Output Data Valid	$t_{DO}$	$C_{LOAD} = 20pF$ , Figure 1	10		50	ns
HBEN Rise to Output Data Valid	$t_{DO1}$	$C_{LOAD} = 20pF$ , Figure 1	10		50	ns
HBEN Fall to Output Data Valid	$t_{DO1}$	$C_{LOAD} = 20pF$ , Figure 1	10		80	ns
$\overline{RD}$ Fall to $\overline{INT}$ High Delay	$t_{INT1}$	$C_{LOAD} = 20pF$ , Figure 1			50	ns
$\overline{CS}$ Fall to Output Data Valid	$t_{DO2}$	$C_{LOAD} = 20pF$ , Figure 1			100	ns

**Note 1:** Tested at  $V_{DD} = +5V$ ,  $COM = GND$ , unipolar single-ended input mode.

**Note 2:** Relative accuracy is the deviation of the analog value at any code from its theoretical value after offset and gain errors have been removed.

**Note 3:** Offset nulled.

**Note 4:** On channel is grounded; sine wave applied to off channels.

**Note 5:** Conversion time is defined as the number of clock cycles times the clock period; clock has 50% duty cycle.

**Note 6:** Input voltage range referenced to negative input. The absolute range for the analog inputs is from GND to  $V_{DD}$ .

**Note 7:** External load should not change during conversion for specified accuracy.

**Note 8:** When bit 5 is set low for internal acquisition,  $\overline{WR}$  must not return low until after the first falling clock edge of the conversion.

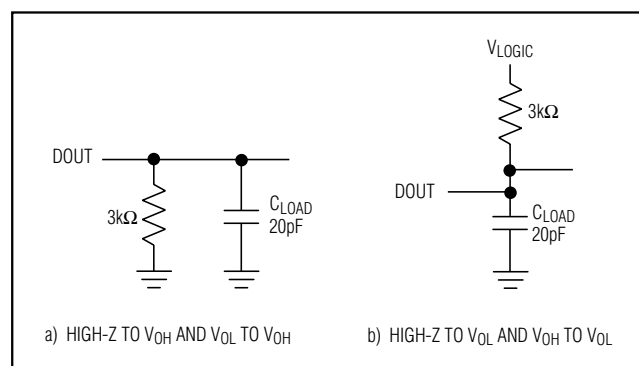
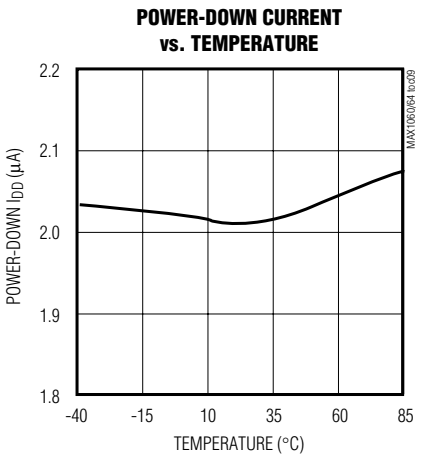
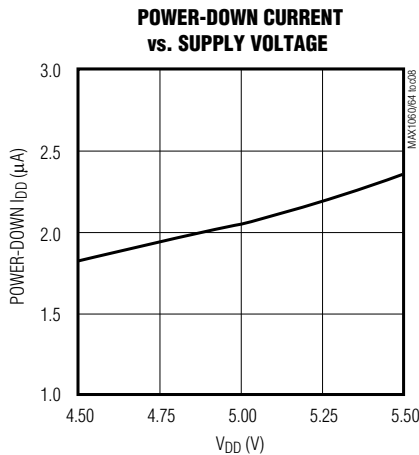
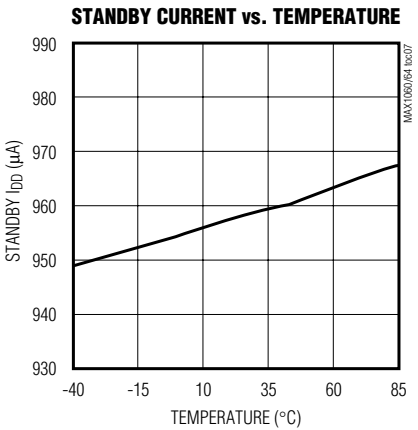
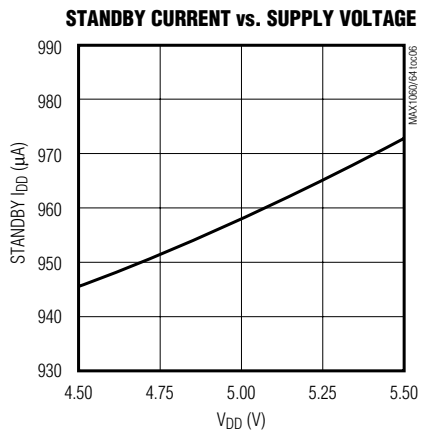
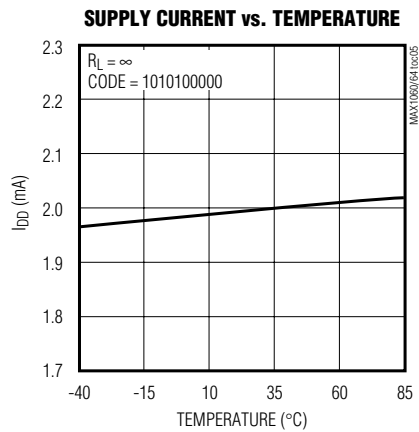
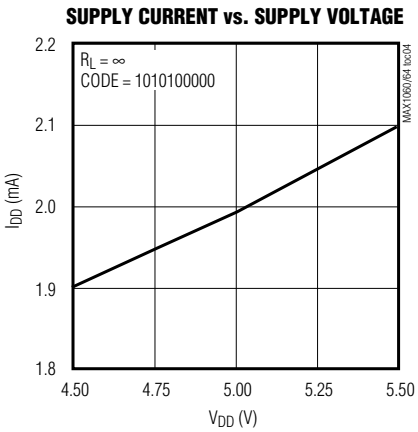
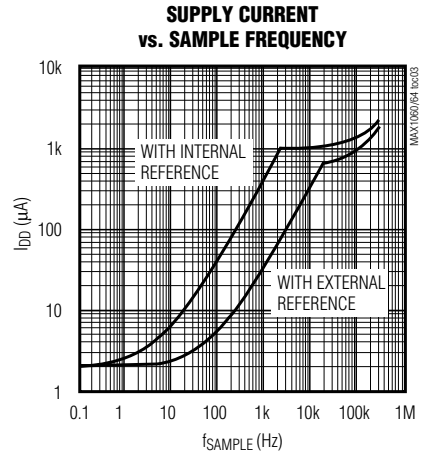
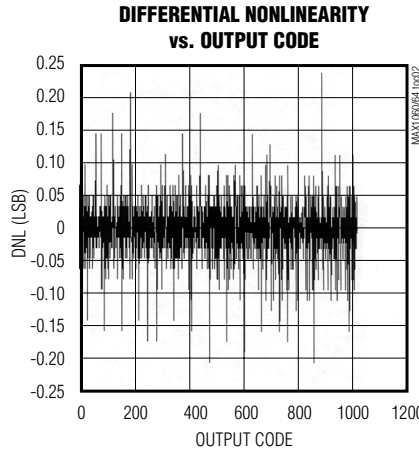
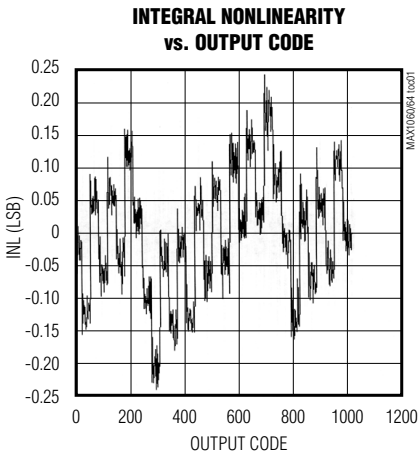


Figure 1. Load Circuits for Enable/Disable Times

# 400kps, +5V, 8-/4-Channel, 10-Bit ADCs with +2.5V Reference and Parallel Interface

## Typical Operating Characteristics

( $V_{DD} = V_{LOGIC} = +5V$ ,  $V_{REF} = +2.500V$ ,  $f_{CLK} = 7.6MHz$ ,  $C_L = 20pF$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)

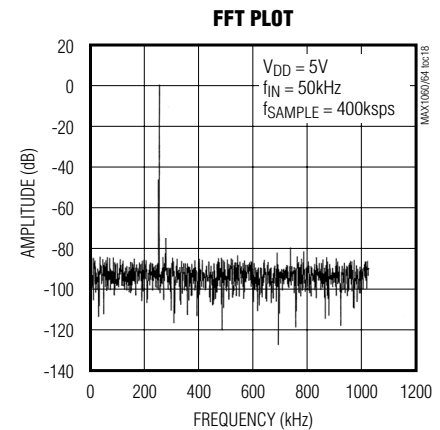
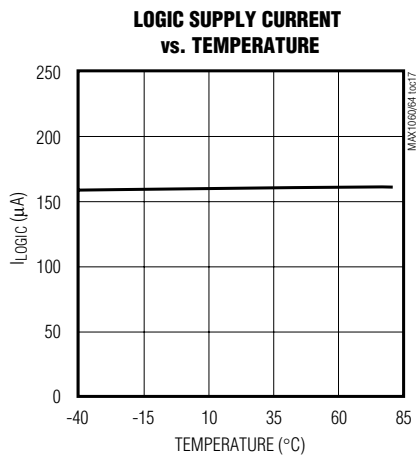
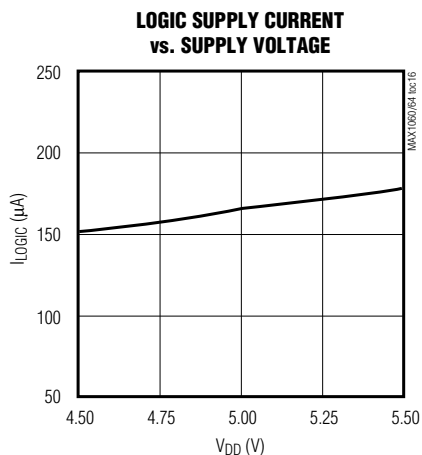
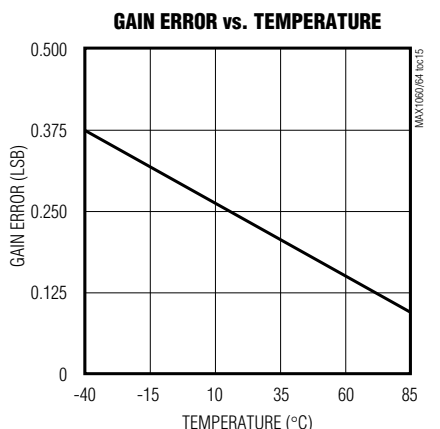
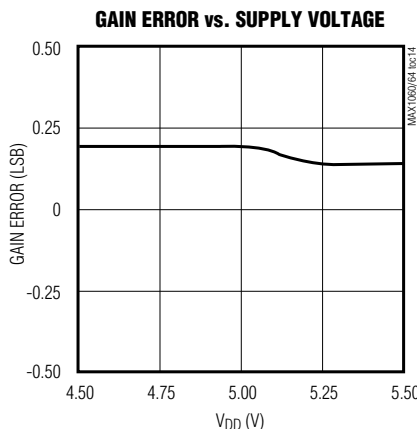
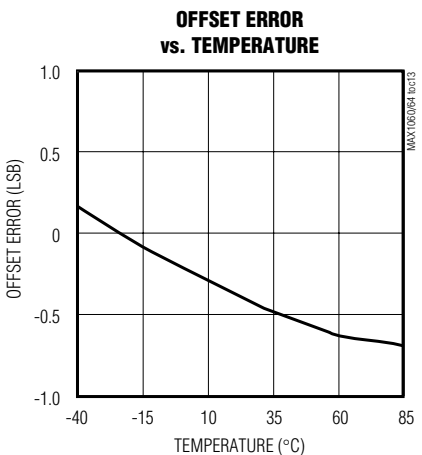
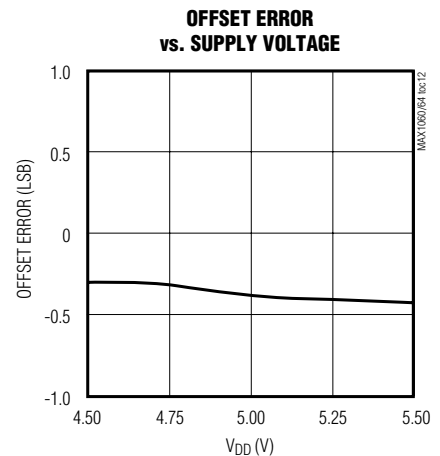
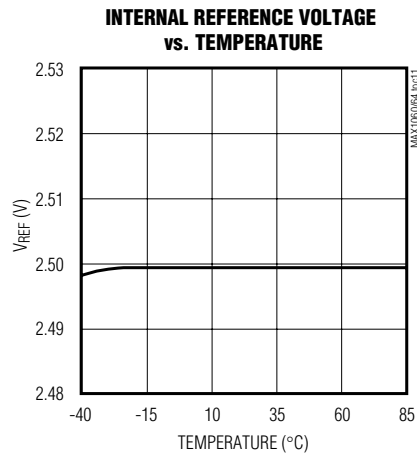
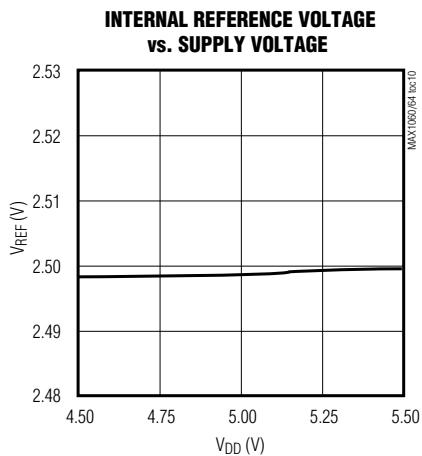


# 400kps, +5V, 8-/4-Channel, 10-Bit ADCs with +2.5V Reference and Parallel Interface

## Typical Operating Characteristics (continued)

( $V_{DD} = V_{LOGIC} = +5V$ ,  $V_{REF} = +2.500V$ ,  $f_{CLK} = 7.6MHz$ ,  $C_L = 20pF$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)

MAX1060/MAX1064



# 400ksp/s, +5V, 8-/4-Channel, 10-Bit ADCs with +2.5V Reference and Parallel Interface

## Pin Description

PIN		NAME	FUNCTION
MAX1060	MAX1064		
1	1	HBEN	High Byte Enable. Used to multiplex the 10-bit conversion result. 1: 2 MSBs are multiplexed on the data bus. 0: 8 LSBs are available on the data bus.
2	2	D7	Tri-State Digital I/O Line (D7)
3	3	D6	Tri-State Digital I/O Line (D6)
4	4	D5	Tri-State Digital I/O Line (D5)
5	5	D4	Tri-State Digital I/O Line (D4)
6	6	D3	Tri-State Digital I/O Line (D3)
7	7	D2	Tri-State Digital I/O Line (D2)
8	8	D1/D9	Tri-State Digital I/O Line (D1, HBEN = 0; D9, HBEN = 1)
9	9	D0/D8	Tri-State Digital I/O Line (D0, HBEN = 0; D8, HBEN = 1)
10	10	$\overline{\text{INT}}$	$\overline{\text{INT}}$ goes low when the conversion is complete and the output data is ready.
11	11	$\overline{\text{RD}}$	Active-Low Read Select. If $\overline{\text{CS}}$ is low, a falling edge on $\overline{\text{RD}}$ enables the read operation on the data bus.
12	12	$\overline{\text{WR}}$	Active-Low Write Select. When $\overline{\text{CS}}$ is low in internal acquisition mode, a rising edge on $\overline{\text{WR}}$ latches in configuration data and starts an acquisition plus a conversion cycle. When $\overline{\text{CS}}$ is low in external acquisition mode, the first rising edge on $\overline{\text{WR}}$ ends acquisition and starts a conversion.
13	13	CLK	Clock Input. In external clock mode, drive CLK with a TTL-/CMOS-compatible clock. In internal clock mode, connect this pin to either $V_{\text{DD}}$ or GND.
14	14	$\overline{\text{CS}}$	Active-Low Chip Select. When $\overline{\text{CS}}$ is high, digital outputs (D7–D0) are high impedance.
15	—	CH7	Analog Input Channel 7
16	—	CH6	Analog Input Channel 6
17	—	CH5	Analog Input Channel 5
18	—	CH4	Analog Input Channel 4
19	15	CH3	Analog Input Channel 3
20	16	CH2	Analog Input Channel 2
21	17	CH1	Analog Input Channel 1
22	18	CH0	Analog Input Channel 0
23	19	COM	Ground Reference for Analog Inputs. Sets zero-code voltage in single-ended mode and must be stable to $\pm 0.5$ LSB during conversion.
24	20	GND	Analog and Digital Ground
25	21	REFADJ	Bandgap Reference Output/Bandgap Reference Buffer Input. Bypass to GND with a $0.01\mu\text{F}$ capacitor. When using an external reference, connect REFADJ to $V_{\text{DD}}$ to disable the internal bandgap reference.
26	22	REF	Bandgap Reference Buffer Output/External Reference Input. Add a $4.7\mu\text{F}$ capacitor to GND when using the internal reference.
27	23	$V_{\text{DD}}$	Analog +5V Power Supply. Bypass with a $0.1\mu\text{F}$ capacitor to GND.
28	24	$V_{\text{LOGIC}}$	Digital Power Supply. $V_{\text{LOGIC}}$ powers the digital outputs of the data converter and can range from +2.7V to ( $V_{\text{DD}} + 300\text{mV}$ ).



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MAX1060/MAX1064

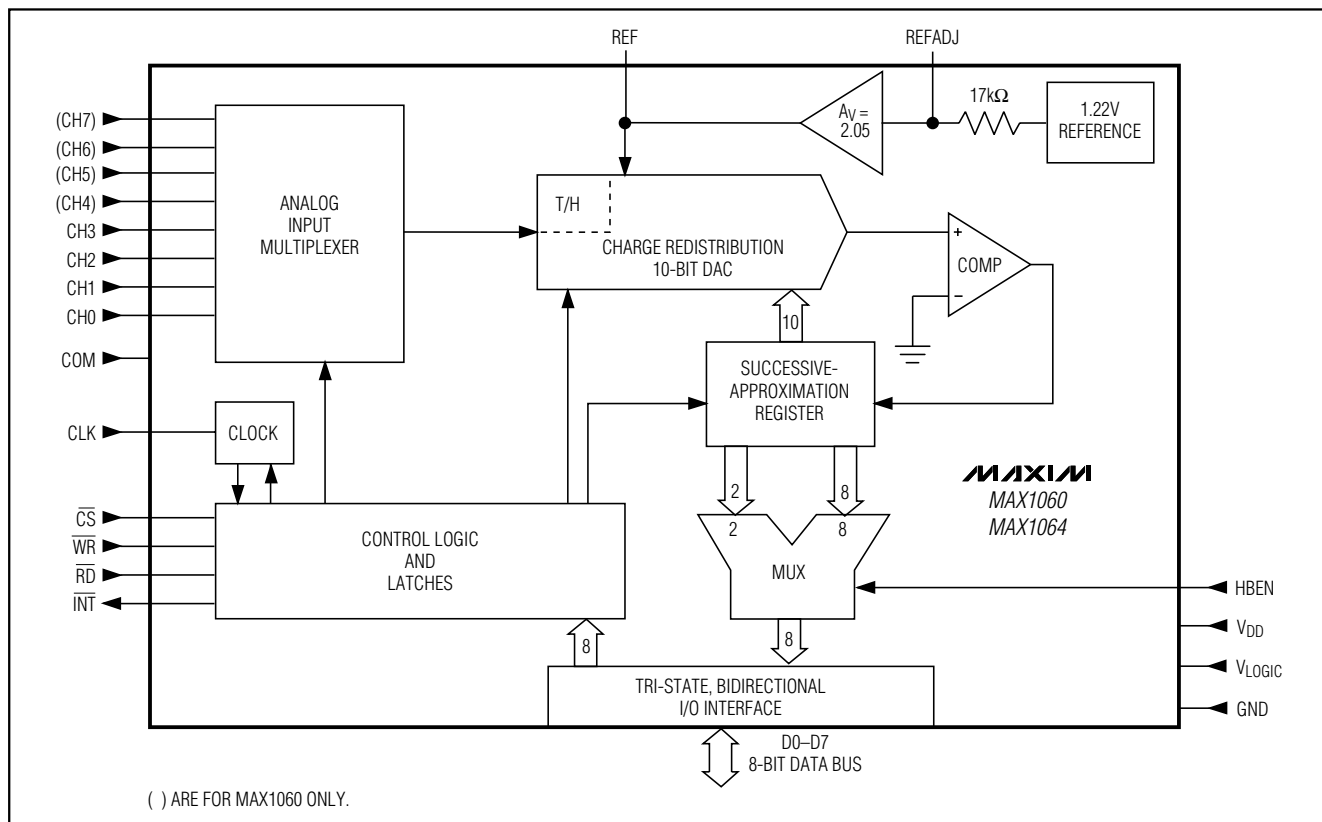


Figure 2. Simplified Functional Diagram of 8-/4-Channel MAX1060/MAX1064

## Detailed Description

### Converter Operation

The MAX1060/MAX1064 ADCs use a successive-approximation (SAR) conversion technique and an input track-and-hold (T/H) stage to convert an analog input signal to a 10-bit digital output. Their parallel (8 + 2) output format provides an easy interface to standard microprocessors ( $\mu$ Ps). Figure 2 shows the simplified internal architecture of the MAX1060/MAX1064.

### Single-Ended and Pseudo-Differential Operation

The sampling architecture of the ADC's analog comparator is illustrated in the equivalent input circuits in Figures 3a and 3b. In single-ended mode,  $IN+$  is internally switched to channels CH0–CH7 for the MAX1060 (Figure 3a) and to CH0–CH3 for the MAX1064 (Figure 3b), while  $IN-$  is switched to COM (Table 3). In differential mode,  $IN+$  and  $IN-$  are selected from analog input pairs (Table 4).

In differential mode,  $IN-$  and  $IN+$  are internally switched to either of the analog inputs. This configuration is pseudo-differential in that only the signal at  $IN+$  is sampled. The return side ( $IN-$ ) must remain stable within  $\pm 0.5$  LSB ( $\pm 0.1$  LSB for best performance) with respect to GND during a conversion. To accomplish this, connect a  $0.1\mu\text{F}$  capacitor from  $IN-$  (the selected input) to GND.

During the acquisition interval, the channel selected as the positive input ( $IN+$ ) charges capacitor  $CHOLD$ . At the end of the acquisition interval, the T/H switch opens, retaining the charge on  $CHOLD$  as a sample of the signal at  $IN+$ .

The conversion interval begins with the input multiplexer switching  $CHOLD$  from the positive input ( $IN+$ ) to the negative input ( $IN-$ ). This unbalances node zero at the comparator's positive input. The capacitive digital-to-analog converter (DAC) adjusts during the remainder of the conversion cycle to restore node zero to 0V within the limits of 10-bit resolution. This action is equivalent to transferring a  $12\text{pF} [(V_{IN+}) - (V_{IN-})]$  charge from  $CHOLD$  to the binary-weighted capacitive DAC, which in turn forms a digital representation of the analog input signal.

# 400kps, +5V, 8-/4-Channel, 10-Bit ADCs with +2.5V Reference and Parallel Interface

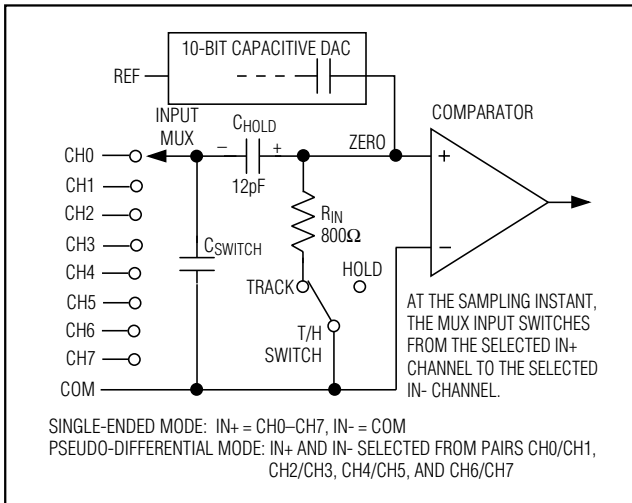


Figure 3a. MAX1060 Simplified Input Structure

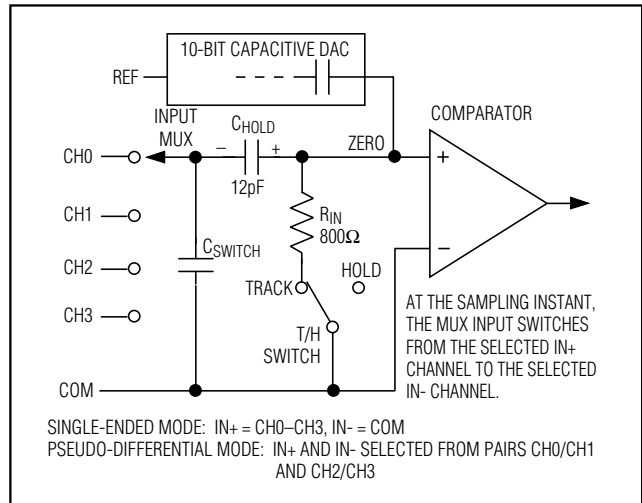


Figure 3b. MAX1064 Simplified Input Structure

### Analog Input Protection

Internal protection diodes, which clamp the analog input to  $V_{DD}$  and  $GND$ , allow each input channel to swing within  $(GND - 300mV)$  to  $(V_{DD} + 300mV)$  without damage. However, for accurate conversions near full scale, neither input should exceed  $(V_{DD} + 50mV)$  or be less than  $(GND - 50mV)$ .

If an off-channel analog input voltage exceeds the supplies by more than 50mV, limit the forward-bias input current to 4mA.

### Track/Hold

The MAX1060/MAX1064 T/H stage enters its tracking mode on the rising edge of  $\overline{WR}$ . In external acquisition mode, the part enters its hold mode on the next rising edge of  $\overline{WR}$ . In internal acquisition mode, the part enters its hold mode on the fourth falling edge of the clock after writing the control byte. Note that, in internal clock mode, this is approximately 1μs after writing the control byte.

In single-ended operation,  $IN-$  is connected to  $COM$  and the converter samples the positive (+) input. In pseudo-differential operation,  $IN-$  connects to the negative input (-) and the difference of  $|(IN+) - (IN-)|$  is sampled. At the beginning of the next conversion, the positive input connects back to  $IN+$  and  $CHOLD$  charges to the input signal.

The time required for the T/H stage to acquire an input signal depends on how quickly its input capacitance is charged. If the input signal's source impedance is high, the acquisition time lengthens and more time must be allowed between conversions. The acquisition time,

$t_{ACQ}$ , is the maximum time the device takes to acquire the signal and is also the minimum time required for the signal to be acquired. Calculate this with the following equation:

$$t_{ACQ} = 7(R_S + R_{IN})C_{IN}$$

where  $R_S$  is the source impedance of the input signal,  $R_{IN}$  (800Ω) is the input resistance, and  $C_{IN}$  (12pF) is the input capacitance of the ADC. Source impedances below 3kΩ have no significant impact on the MAX1060/MAX1064s' AC performance.

Higher source impedances can be used if a 0.01μF capacitor is connected to the individual analog inputs. Along with the input impedance, this capacitor forms an RC filter, limiting the ADC's signal bandwidth.

### Input Bandwidth

The MAX1060/MAX1064 T/H stage offers a 350kHz full-linear and a 6MHz full-power bandwidth. These features make it possible to digitize high-speed transients and measure periodic signals with bandwidths exceeding the ADC's sampling rate by using undersampling techniques. To avoid aliasing high-frequency signals into the frequency band of interest, anti-alias filtering is recommended.

### Starting a Conversion

Initiate a conversion by writing a control byte that selects the multiplexer channel and configures the MAX1060/MAX1064 for either unipolar or bipolar operation. A write pulse ( $\overline{WR} + \overline{CS}$ ) can either start an acquisition interval or initiate a combined acquisition plus conversion. The sampling interval occurs at the end of

## 400ksps, +5V, 8-/4-Channel, 10-Bit ADCs with +2.5V Reference and Parallel Interface

the acquisition interval. The ACQMOD (acquisition mode) bit in the input control byte (Table 1) offers two options for acquiring the signal: an internal and an external acquisition. The conversion period lasts for 13 clock cycles in either the internal or external clock or acquisition mode. Writing a new control byte during a conversion cycle aborts the conversion and starts a new acquisition interval.

### Internal Acquisition

Select internal acquisition by writing the control byte with the ACQMOD bit cleared (ACQMOD = 0). This causes the write pulse to initiate an acquisition interval whose duration is internally timed. Conversion starts when this acquisition interval (three external clock cycles or approximately 1 $\mu$ s in internal clock mode) ends (Figure 4). When the internal acquisition is combined with the internal clock, the aperture jitter can be as high as 200ps. Internal clock users wishing to achieve the 50ps jitter specification should always use external acquisition mode.

### External Acquisition

Use external acquisition mode for precise control of the sampling aperture and/or dependent control of acquisition and conversion times. The user controls acquisition and start-of-conversion with two separate write pulses. The first pulse, written with ACQMOD = 1, starts an

acquisition interval of indeterminate length. The second write pulse, written with ACQMOD = 0 (all other bits in the control byte are unchanged), terminates acquisition and starts conversion on  $\overline{WR}$  rising edge (Figure 5).

The address bits for the input multiplexer must have the same values on the first and second write pulses. Power-down mode bits (PD0, PD1) can assume new values on the second write pulse (see the *Power-Down Modes* section). Changing other bits in the control byte corrupts the conversion.

### Reading a Conversion

A standard interrupt signal,  $\overline{INT}$ , is provided to allow the MAX1060/MAX1064 to flag the  $\mu$ P when the conversion has ended and a valid result is available.  $\overline{INT}$  goes low when the conversion is complete and the output data is ready (Figures 4 and 5).  $\overline{INT}$  returns high on the first read cycle or if a new control byte is written.

### Selecting Clock Mode

The MAX1060/MAX1064 operate with an internal or external clock. Control bits D6 and D7 select either internal or external clock mode. The part retains the last-requested clock mode if a power-down mode is selected in the current input word. For both internal and external clock modes, internal or external acquisition can be used. At power-up, the MAX1060/MAX1064 enter the default external clock mode.

**Table 1. Control Byte Functional Description**

BIT	NAME	FUNCTION
D7, D6	PD1, PD0	<b>PD1</b> and <b>PD0</b> select the various clock and power-down modes.
		<b>0</b> <b>0</b> Full power-down mode. Clock mode is unaffected.
		<b>0</b> <b>1</b> Standby power-down mode. Clock mode is unaffected.
		<b>1</b> <b>0</b> Normal operation mode. Internal clock mode is selected.
<b>1</b> <b>1</b> Normal operation mode. External clock mode is selected.		
D5	ACQMOD	ACQMOD = 0: Internal acquisition mode ACQMOD = 1: External acquisition mode
D4	SGL/ $\overline{DIF}$	SGL/ $\overline{DIF}$ = 0: Pseudo-differential analog input mode SGL/ $\overline{DIF}$ = 1: Single-ended analog input mode In single-ended mode, input signals are referred to COM. In pseudo-differential mode, the voltage difference between two channels is measured (Tables 2 and 3).
D3	UNI/ $\overline{BIP}$	UNI/ $\overline{BIP}$ = 0: Bipolar mode UNI/ $\overline{BIP}$ = 1: Unipolar mode In unipolar mode, an analog input signal from 0 to $V_{REF}$ can be converted; in bipolar mode, the signal can range from $-V_{REF}/2$ to $+V_{REF}/2$ .
D2, D1, D0	A2, A1, A0	Address bits A2, A1, A0 select which of the 8/4 (MAX1060/MAX1064) channels are to be converted (Tables 3 and 4).

# 400kps, +5V, 8-/4-Channel, 10-Bit ADCs with +2.5V Reference and Parallel Interface

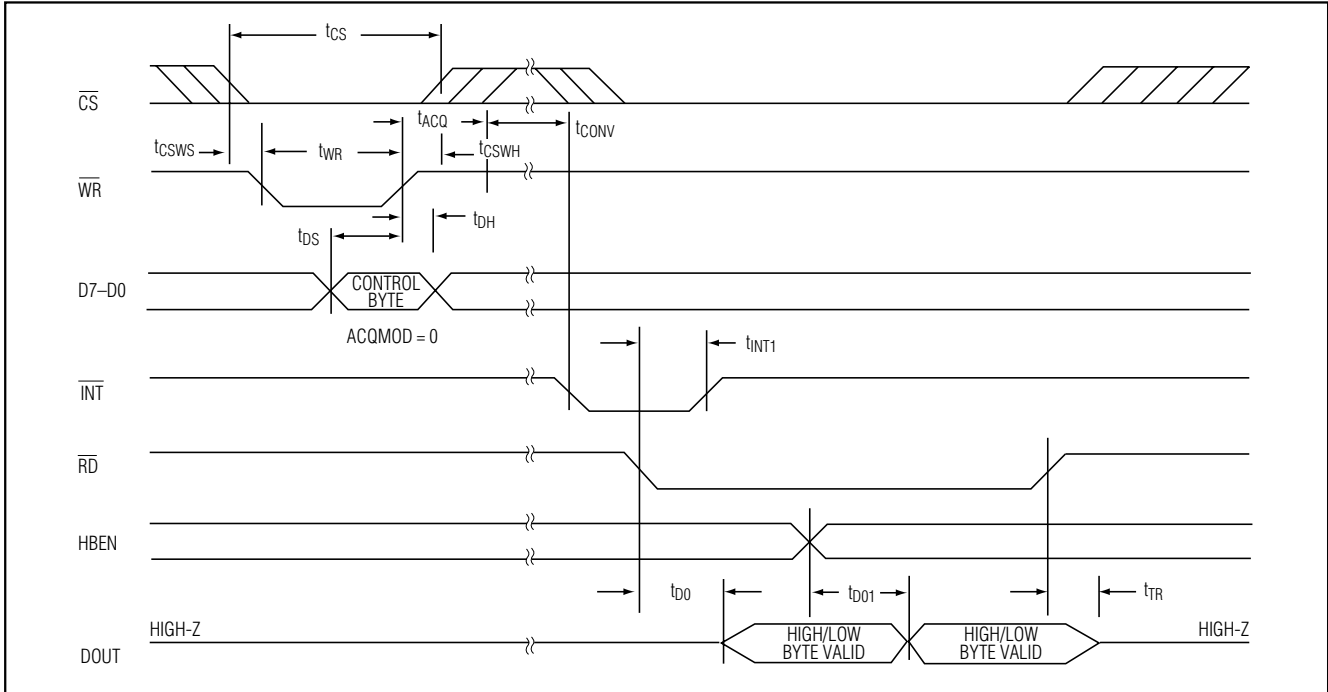


Figure 4. Conversion Timing Using Internal Acquisition Mode

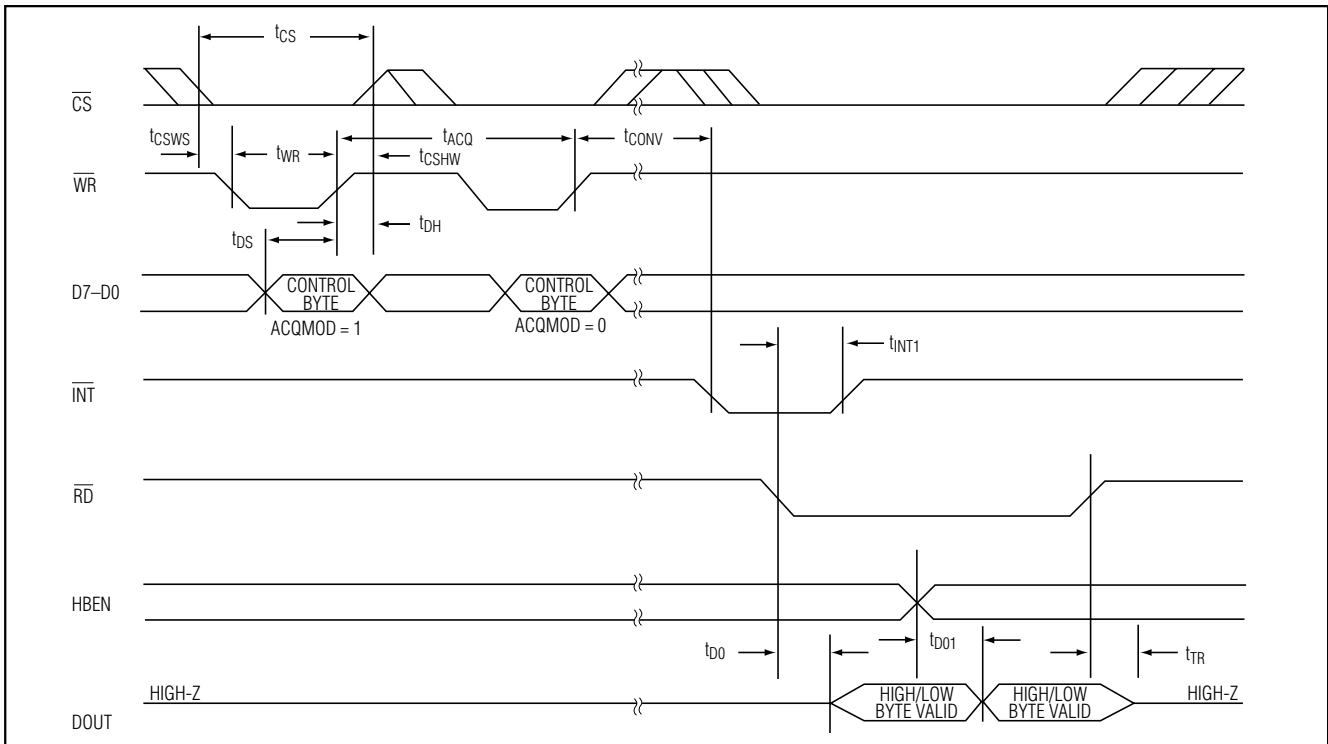


Figure 5. Conversion Timing Using External Acquisition Mode

# 400kps, +5V, 8-/4-Channel, 10-Bit ADCs with +2.5V Reference and Parallel Interface

### Internal Clock Mode

Select internal clock mode to release the  $\mu\text{P}$  from the burden of running the SAR conversion clock. To select this mode, bit D7 of the control byte must be set to 1 and bit D6 must be set to zero. The internal clock frequency is then selected, resulting in a  $3.6\mu\text{s}$  conversion time. When using the internal clock mode, connect the CLK pin either high or low to prevent the pin from floating.

### External Clock Mode

To select the external clock mode, bits D6 and D7 of the control byte must be set to 1. Figure 6 shows the clock and  $\overline{\text{WR}}$  timing relationship for internal (Figure 6a) and external (Figure 6b) acquisition modes with an external clock. Proper operation requires a 100kHz to 7.6MHz clock frequency with 30% to 70% duty cycle. Operating the MAX1060/MAX1064 with clock frequencies lower than 100kHz is not recommended, because it causes a voltage droop across the hold capacitor in the T/H stage that results in degraded performance.

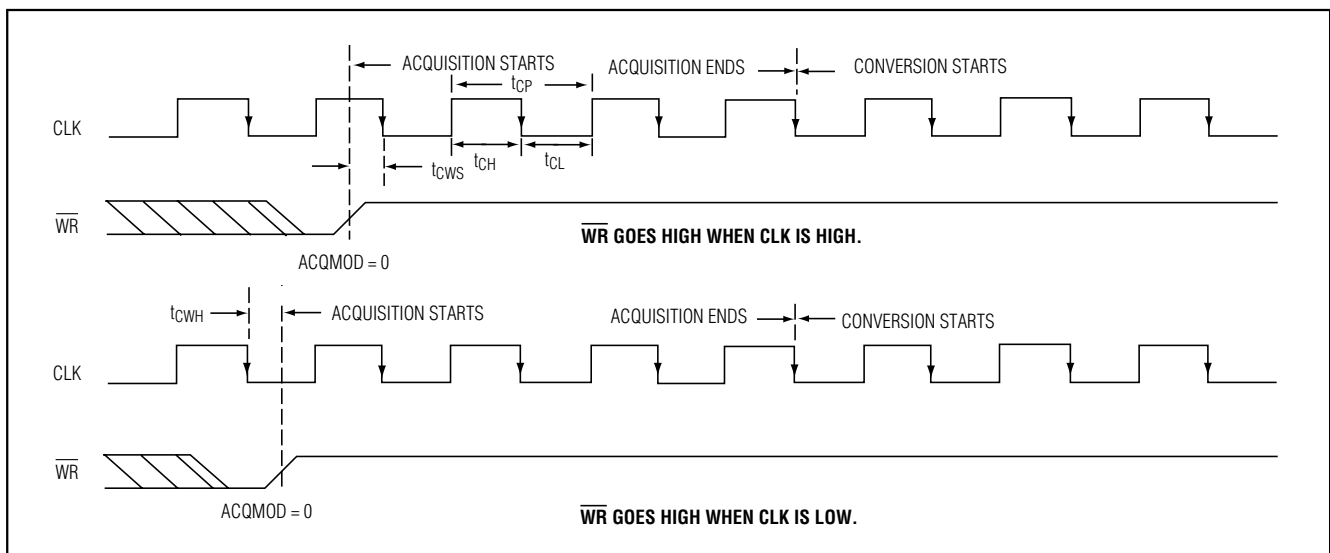


Figure 6a. External Clock and  $\overline{\text{WR}}$  Timing (Internal Acquisition Mode)

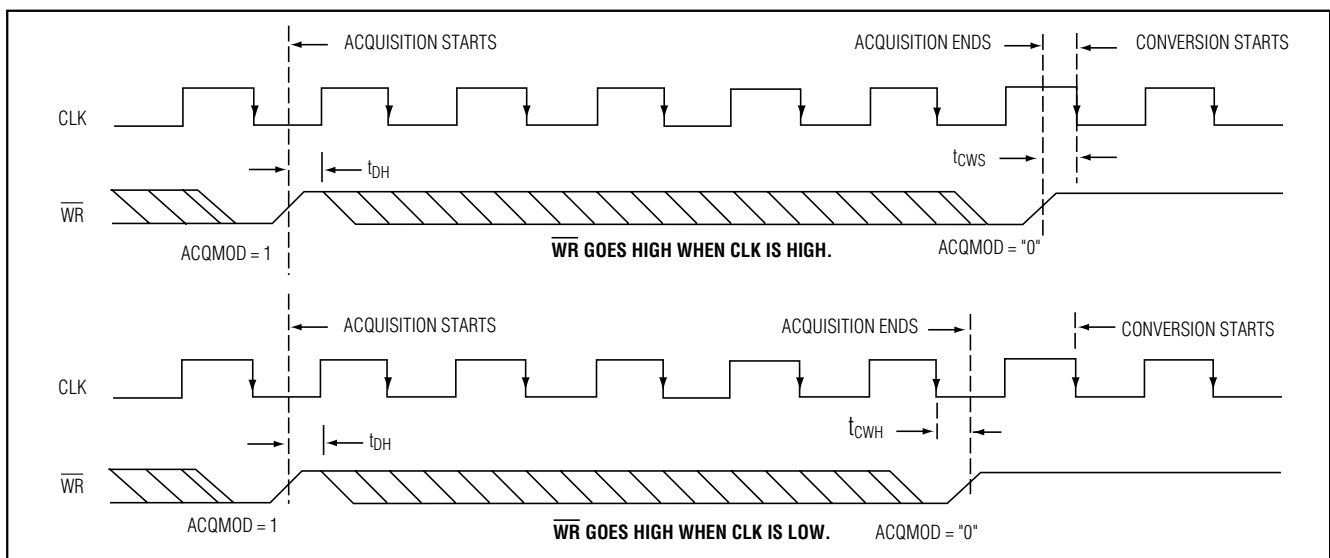


Figure 6b. External Clock and  $\overline{\text{WR}}$  Timing (External Acquisition Mode)

# 400ksp/s, +5V, 8-/4-Channel, 10-Bit ADCs with +2.5V Reference and Parallel Interface

## Digital Interface

Input (control byte) and output data are multiplexed on a tri-state parallel interface. This parallel interface (I/O) can easily be interfaced with standard  $\mu$ Ps. Signals  $\overline{CS}$ ,  $\overline{WR}$ , and  $\overline{RD}$  control the write and read operations.  $\overline{CS}$  represents the chip-select signal, which enables a  $\mu$ P to address the MAX1060/MAX1064 as an I/O port. When high,  $\overline{CS}$  disables the CLK,  $\overline{WR}$ , and  $\overline{RD}$  inputs and forces the interface into a high-impedance (high-Z) state.

## Input Format

The control byte is latched into the device on pins D7–D0 during a write command. Table 2 shows the control byte format.

## Output Format

The output format for the MAX1060/MAX1064 is binary in unipolar mode and two's complement in bipolar mode. When reading the output data,  $\overline{CS}$  and  $\overline{RD}$  must be low. When HBEN = 0, the lower 8 bits are read. With HBEN = 1, the upper 2 bits are available and the output data bits D7–D2 are set either low in unipolar mode or to the value of the MSB in bipolar mode (Table 5).

**Table 2. Control Byte Format**

D7 (MSB)	D6	D5	D4	D3	D2	D1	D0 (LSB)
PD1	PD0	ACQMOD	SGL/DIF	UNI/BIP	A2	A1	A0

**Table 3. Channel Selection for Single-Ended Operation (SGL/DIF = 1)**

A2	A1	A0	CH0	CH1	CH2	CH3	CH4*	CH5*	CH6*	CH7*	COM
0	0	0	+								-
0	0	1		+							-
0	1	0			+						-
0	1	1				+					-
1	0	0					+				-
1	0	1						+			-
1	1	0							+		-
1	1	1								+	-

\*Channels CH4–CH7 apply to MAX1060 only.

**Table 4. Channel Selection for Pseudo-Differential Operation (SGL/DIF = 0)**

A2	A1	A0	CH0	CH1	CH2	CH3	CH4*	CH5*	CH6*	CH7*
0	0	0	+	-						
0	0	1	-	+						
0	1	0			+	-				
0	1	1			-	+				
1	0	0					+	-		
1	0	1					-	+		
1	1	0							+	-
1	1	1							-	+

\*Channels CH4–CH7 apply to MAX1060 only.

# 400ksps, +5V, 8-/4-Channel, 10-Bit ADCs with +2.5V Reference and Parallel Interface

MAX1060/MAX1064

**Table 5. Data-Bus Output (8 + 2 Parallel Interface)**

PIN	HBEN = 0	HBEN = 1	
D0	Bit 0 (LSB)	Bit 8	
D1	Bit 1	Bit 9 (MSB)	
		BIPOLAR (UNI/BIP = 0)	UNIPOLAR (UNI/BIP = 1)
D2	Bit 2	Bit 9	0
D3	Bit 3	Bit 9	0
D4	Bit 4	Bit 9	0
D5	Bit 5	Bit 9	0
D6	Bit 6	Bit 9	0
D7	Bit 7	Bit 9	0

## Applications Information

### Power-On Reset

When power is first applied, internal power-on reset circuitry activates the MAX1060/MAX1064 in external clock mode and sets INT high. After the power supplies stabilize, the internal reset time is 10 $\mu$ s, and no conversions should be attempted during this phase. When using the internal reference, 500 $\mu$ s are required for VREF to stabilize.

### Internal and External Reference

The MAX1060/MAX1064 can be used with an internal or external reference voltage. An external reference can be connected directly to REF or REFADJ.

An internal buffer is designed to provide +2.5V at REF for both devices. The internally trimmed +1.22V reference is buffered with a +2.05V/V gain.

### Internal Reference

The full-scale range with the internal reference is +2.5V with unipolar inputs and  $\pm 1.25$ V with bipolar inputs. The internal reference buffer allows for small adjustments ( $\pm 100$ mV) in the reference voltage (Figure 7).

**Note:** The reference buffer must be compensated with an external capacitor (4.7 $\mu$ F min) connected between REF and GND to reduce reference noise and switching spikes from the ADC. To further minimize reference noise, connect a 0.01 $\mu$ F capacitor between REFADJ and GND.

### External Reference

With the MAX1060/MAX1064, an external reference can be placed at either the input (REFADJ) or the output (REF) of the internal reference-buffer amplifier.

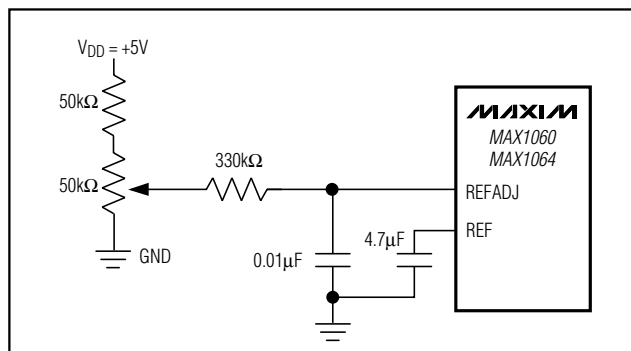


Figure 7. Reference Voltage Adjustment with External Potentiometer

Using the REFADJ input makes buffering the external reference unnecessary. The REFADJ input impedance is typically 17k $\Omega$ .

When applying an external reference to REF, disable the internal reference buffer by connecting REFADJ to VDD. The DC input resistance at REF is 25k $\Omega$ . Therefore, an external reference at REF must deliver up to 200 $\mu$ A DC load current during a conversion and have an output impedance less than 10 $\Omega$ . If the reference has higher output impedance or is noisy, bypass it close to the REF pin with a 4.7 $\mu$ F capacitor.

### Power-Down Modes

To save power, place the converter in a low-current shutdown state between conversions. Select standby mode or shutdown mode using bits D6 and D7 of the control byte (Tables 1 and 2). In both software power-down modes, the parallel interface remains active, but the ADC does not convert.

### Standby Mode

While in standby mode, the supply current is 1mA (typ). The part powers up on the next rising edge on WR and is ready to perform conversions. This quick turn-on time allows the user to realize significantly reduced power consumption for conversion rates below 400ksps.

### Shutdown Mode

Shutdown mode turns off all chip functions that draw quiescent current, reducing the typical supply current to 2 $\mu$ A immediately after the current conversion is completed. A rising edge on WR causes the MAX1060/MAX1064 to exit shutdown mode and return to normal operation. To achieve full 10-bit accuracy with a 4.7 $\mu$ F reference bypass capacitor, 500 $\mu$ s is required after power-up. Waiting 500 $\mu$ s in standby mode, instead of in full-power mode, can reduce power consumption by a factor of 3 or more. When using an external reference,

# 400ksp/s, +5V, 8-/4-Channel, 10-Bit ADCs with +2.5V Reference and Parallel Interface

only 50µs are required after power-up. Enter standby mode by performing a dummy conversion with the control byte specifying standby mode.

**Note:** Bypass capacitors larger than 4.7µF between REF and GND result in longer power-up delays.

### Transfer Function

Table 6 shows the full-scale voltage ranges for unipolar and bipolar modes.

Figure 8 depicts the nominal, unipolar input/output (I/O) transfer function, and Figure 9 shows the bipolar I/O transfer function. Code transitions occur halfway between successive-integer LSB values. Output coding is binary, with  $1 \text{ LSB} = V_{REF} / 1024$ .

### Maximum Sampling Rate/Achieving 475ksp/s

When running at the maximum clock frequency of 7.6MHz, the specified 400ksp/s throughput is achieved by completing a conversion every 19 clock cycles: 1 write cycle, 3 acquisition cycles, 13 conversion cycles, and 2 read cycles. This assumes that the results of the last conversion are read before the next control byte is written. It is possible to achieve higher throughputs (Figure 10), up to 475ksp/s, by first writing a control word to begin the acquisition cycle of the next conversion, then reading the results of the previous conversion from the bus. This technique allows a conversion to be completed every 16 clock cycles. Note that switching the data bus during acquisition or conversion can cause additional supply noise that can make it difficult to achieve true 10-bit performance.

### Layout, Grounding, and Bypassing

For best performance, use printed circuit boards. Wire-wrap configurations are not recommended since the layout should ensure proper separation of analog and digital traces. Do not run analog and digital lines parallel to each other, and do not lay out digital signal paths underneath the ADC package. Use separate analog and digital PC board ground sections with only one star point (Figure 11) connecting the two ground systems (analog and digital). For lowest noise operation, ensure the ground return to the star ground's power supply is low impedance and as short as possible. Route digital signals far away from sensitive analog and reference inputs.

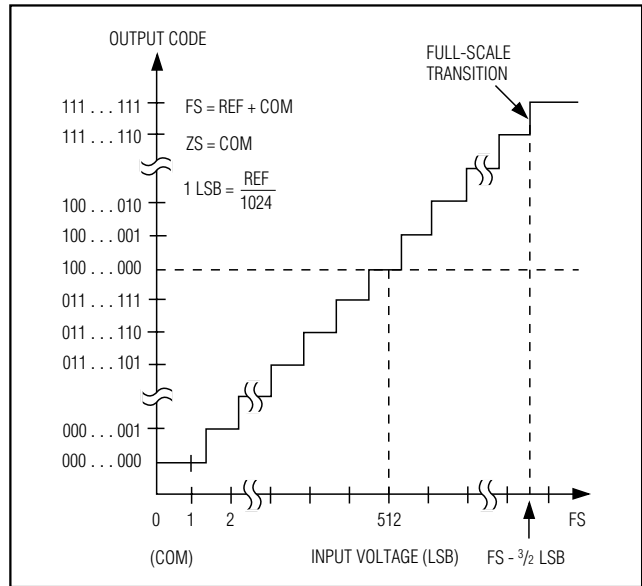


Figure 8. Unipolar Transfer Function

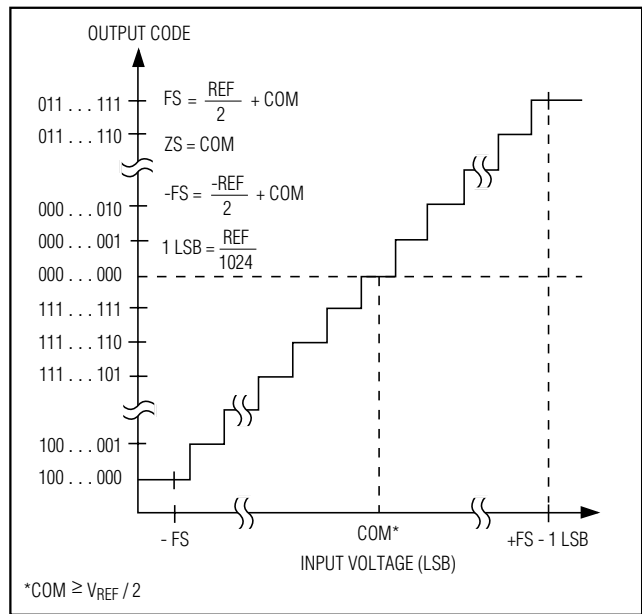


Figure 9. Bipolar Transfer Function

**Table 6. Full Scale and Zero Scale for Unipolar and Bipolar Operation**

UNIPOLAR MODE		BIPOLAR MODE	
Full scale	$V_{REF} + COM$	Positive full scale	$V_{REF}/2 + COM$
Zero scale	COM	Zero scale	COM
—	—	Negative full scale	$-V_{REF}/2 + COM$



# 400ksps, +5V, 8-/4-Channel, 10-Bit ADCs with +2.5V Reference and Parallel Interface

High-frequency noise in the power supply ( $V_{DD}$ ) could influence the proper operation of the ADC's fast comparator. Bypass  $V_{DD}$  to the star ground with a network of two parallel capacitors, 0.1 $\mu$ F and 4.7 $\mu$ F, located as close as possible to the MAX1060/MAX1064s' power-supply pin. Minimize capacitor lead length for best supply-noise rejection, and add an attenuation resistor (5 $\Omega$ ) if the power supply is extremely noisy.

## Definitions

### Integral Nonlinearity

Integral nonlinearity (INL) is the deviation of the values on an actual transfer function from a straight line. This straight line can be either a best-straight-line fit or a line drawn between the end points of the transfer function, once offset and gain errors have been nullified. The

MAX1060/MAX1064s' INL is measured using the end-point method.

### Differential Nonlinearity

Differential nonlinearity (DNL) is the difference between an actual step width and the ideal value of 1 LSB. A DNL error specification of less than 1 LSB guarantees no missing codes and a monotonic transfer function.

### Aperture Jitter

Aperture jitter ( $t_{AJ}$ ) is the sample-to-sample variation in the time between the samples.

### Aperture Delay

Aperture delay ( $t_{AD}$ ) is the time between the rising edge of the sampling clock and the instant when an actual sample is taken.

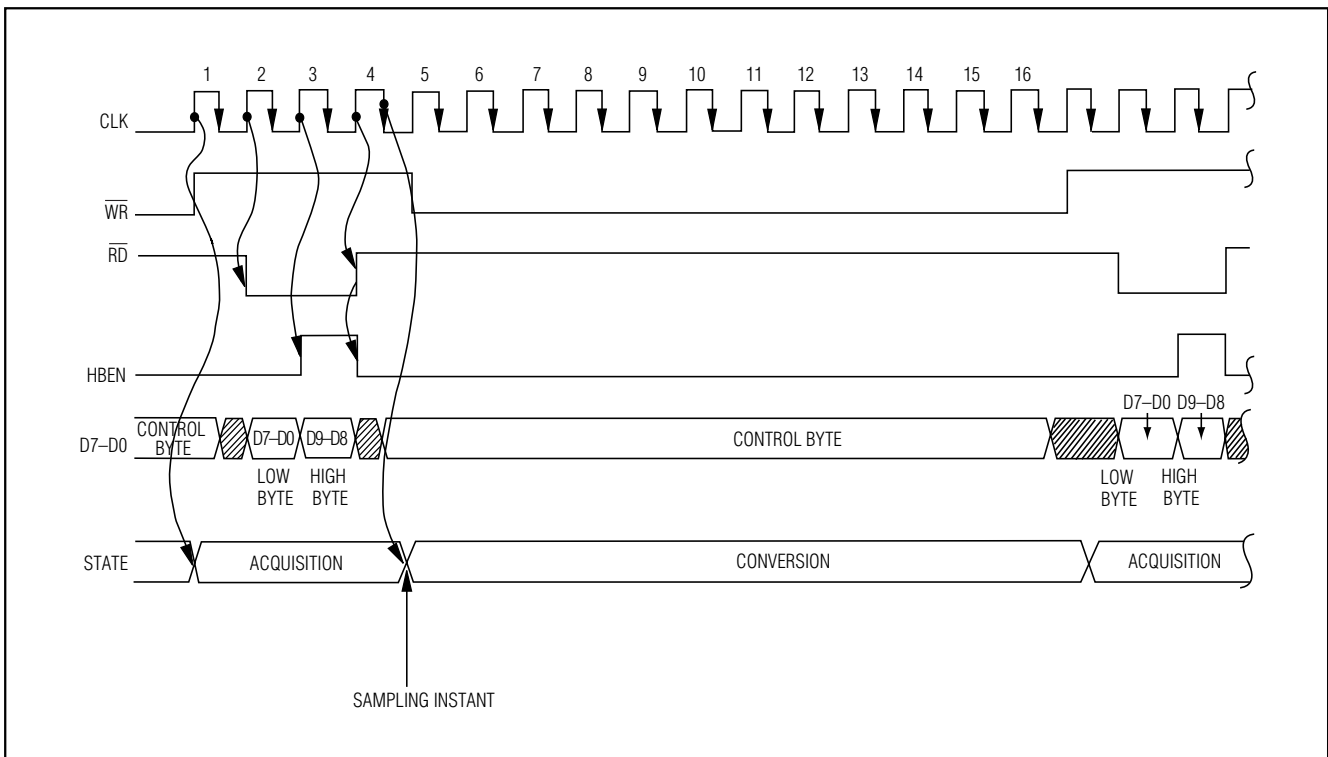


Figure 10. Timing Diagram for Fastest Conversion

# 400ksps, +5V, 8-/4-Channel, 10-Bit ADCs with +2.5V Reference and Parallel Interface

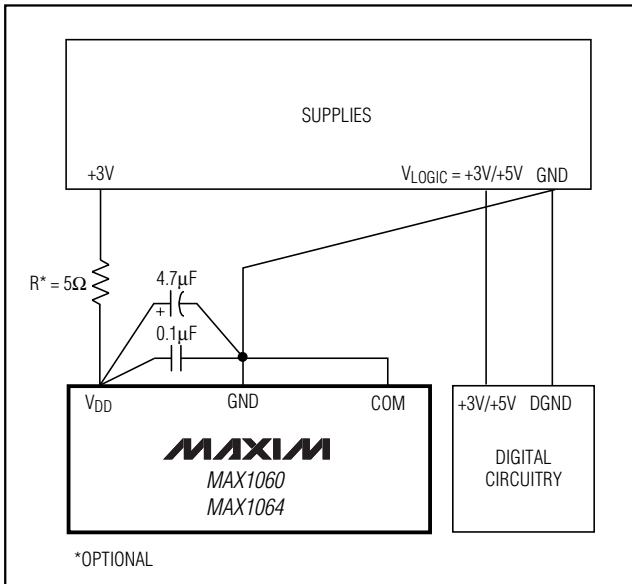


Figure 11. Power-Supply and Grounding Connections

### Signal-to-Noise Ratio

For a waveform perfectly reconstructed from digital samples, signal-to-noise ratio (SNR) is the ratio of the full-scale analog input (RMS value) to the RMS quantization error (residual error). The ideal theoretical minimum analog-to-digital noise is caused by quantization error only and results directly from the ADC's resolution (N bits):

$$\text{SNR} = (6.02 \times N + 1.76) \text{dB}$$

In reality, there are other noise sources besides quantization noise, including thermal noise, reference noise, clock jitter, etc. Therefore, SNR is computed by taking the ratio of the RMS signal to the RMS noise, which includes all spectral components minus the fundamental, the first five harmonics, and the DC offset.

### Signal-to-Noise Plus Distortion

Signal-to-noise plus distortion (SINAD) is the ratio of the fundamental input frequency's RMS amplitude to the RMS equivalent of all other ADC output signals.

$$\text{SINAD (dB)} = 20 \times \log (\text{Signal}_{\text{RMS}} / \text{Noise}_{\text{RMS}})$$

### Effective Number of Bits

Effective number of bits (ENOB) indicates the global accuracy of an ADC at a specific input frequency and sampling rate. An ideal ADC error consists of quantization noise only. With an input range equal to the ADC's full-scale range, calculate the ENOB as follows:

$$\text{ENOB} = (\text{SINAD} - 1.76) / 6.02$$

### Total Harmonic Distortion

Total harmonic distortion (THD) is the ratio of the RMS sum of the input signal's first five harmonics to the fundamental itself. This is expressed as:

$$\text{THD} = 20 \times \log \left( \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2}}{V_1} \right)$$

where  $V_1$  is the fundamental amplitude, and  $V_2$  through  $V_5$  are the amplitudes of the 2nd- through 5th-order harmonics.

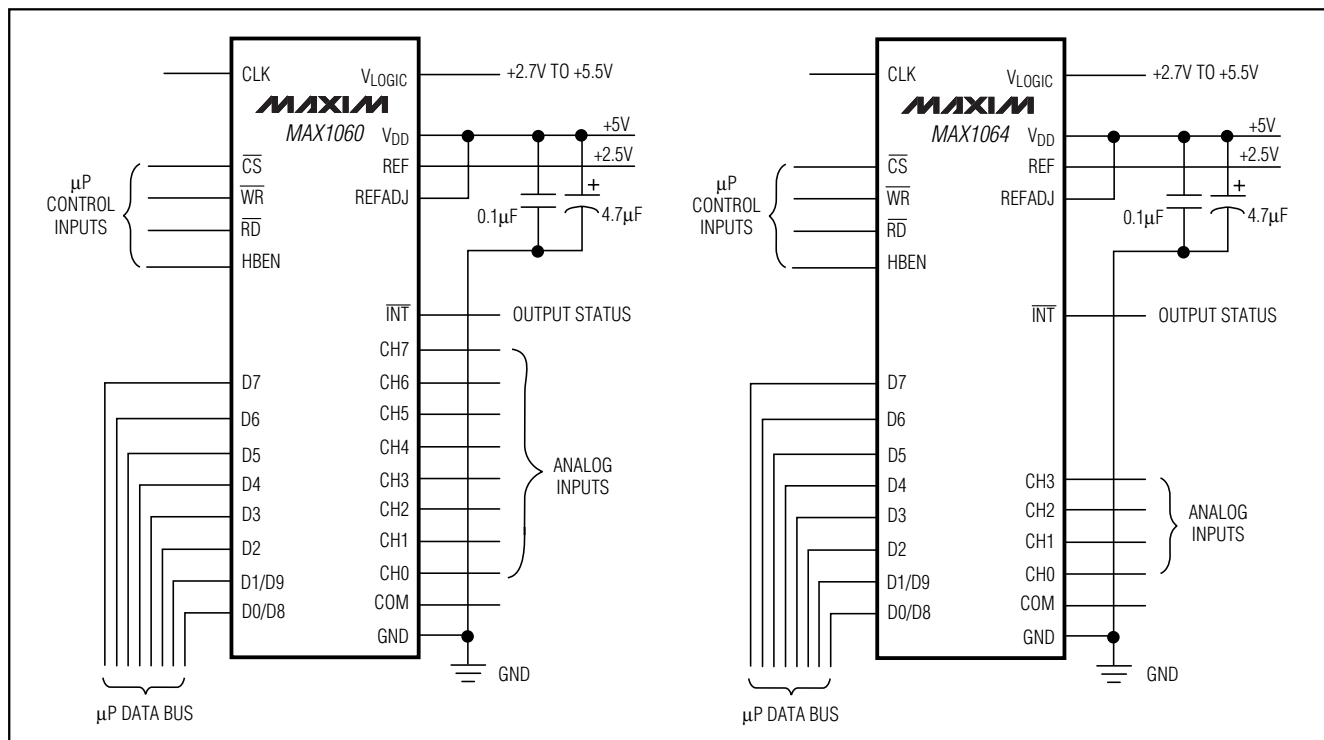
### Spurious-Free Dynamic Range

Spurious-free dynamic range (SFDR) is the ratio of the RMS amplitude of the fundamental (maximum signal component) to the RMS value of the next-largest distortion component.

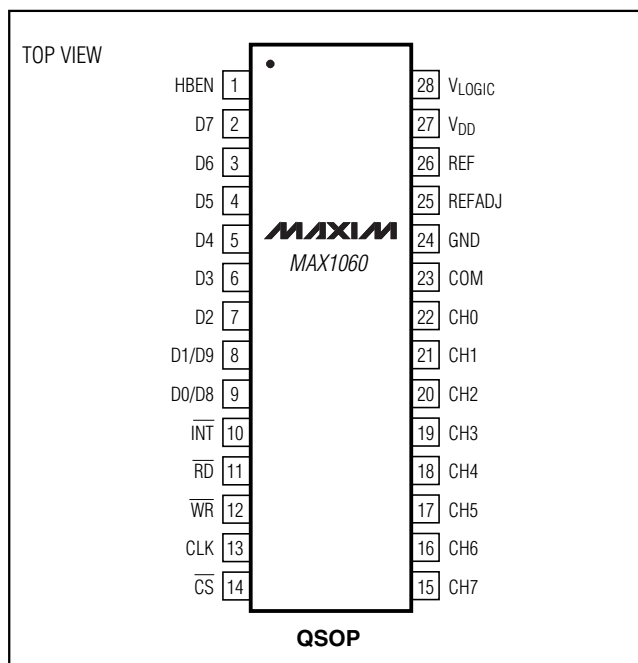
# 400kps, +5V, 8-/4-Channel, 10-Bit ADCs with +2.5V Reference and Parallel Interface

**MAX1060/MAX1064**

## Typical Operating Circuits



## Pin Configurations (continued)



## Ordering Information (continued)

PART	TEMP RANGE	PIN-PACKAGE	INL (LSB)
MAX1064ACEG	0°C to +70°C	24 QSOP	±0.5
MAX1064BCEG	0°C to +70°C	24 QSOP	±1
MAX1064AEEG	-40°C to +85°C	24 QSOP	±0.5
MAX1064BEEG	-40°C to +85°C	24 QSOP	±1

## Chip Information

TRANSISTOR COUNT: 5781

# 400ksp/s, +5V, 8-/4-Channel, 10-Bit ADCs with +2.5V Reference and Parallel Interface

## Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).)

QSOP-EPS

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.061	.068	1.55	1.73
A1	.004	.0098	0.102	0.249
A2	.055	.061	1.40	1.55
B	.008	.012	0.20	0.31
C	.0075	.0098	0.191	0.249
D	SEE VARIATIONS			
E	.150	.157	3.81	3.99
e	.025 BSC		0.635 BSC	
H	.230	.244	5.84	6.20
h	.010	.016	0.25	0.41
L	.016	.035	0.41	0.89
N	SEE VARIATIONS			
X	SEE VARIATIONS			
Y	.071	.087	1.803	2.209
α	0°	8°	0°	8°

DIM	INCHES		MILLIMETERS		N
	MIN.	MAX.	MIN.	MAX.	
D	.189	.196	4.80	4.98	16   AA
S	.0020	.0070	0.05	0.18	
X	.107	.123	2.72	3.12	
D	.337	.344	8.56	8.74	20   AB
S	.0500	.0550	1.270	1.397	
D	.337	.344	8.56	8.74	24   AC
S	.0250	.0300	0.635	0.762	
D	.386	.393	9.80	9.98	28   AD
S	.0250	.0300	0.635	0.762	
X	.271	.287	6.88	7.29	

**NOTES:**  
 1. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.  
 2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .006" PER SIDE.  
 3. HEAT SLUG DIMENSIONS X AND Y APPLY ONLY TO 16 AND 28 LEAD POWER-QSOP PACKAGES.  
 4. CONTROLLING DIMENSIONS: INCHES.  
 5. MEETS JEDEC MO137.

**MAXIM**  
PROPRIETARY INFORMATION

TITLE:  
**PACKAGE OUTLINE, QSOP, .150", .025" LEAD PITCH**

APPROVAL	DOCUMENT CONTROL NO. 21-0055	REV C	1/1
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Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

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