# SL38160-17AH
# SL38160-23AH

## Programmable Audio/Video CG with VCXO

### Key Features

- Audio + video clock generation
- Programmable on chip analog VCXO with typical pull range of +/-150ppm
- VCXO control voltage, 0V to 3V
- Uses 27MHz pullable crystal
- 3.3V +/-10% power supply range
- Available in both Commercial (0 to 70C)and Industrial (-40 to 85C) temperature grades
- Low power dissipation and low jitter
- Integrated internal voltage regulator

### Applications

- HDTV & SDTV
- Wireless HDMI
- Set Top Box
- Media Center
- DVR

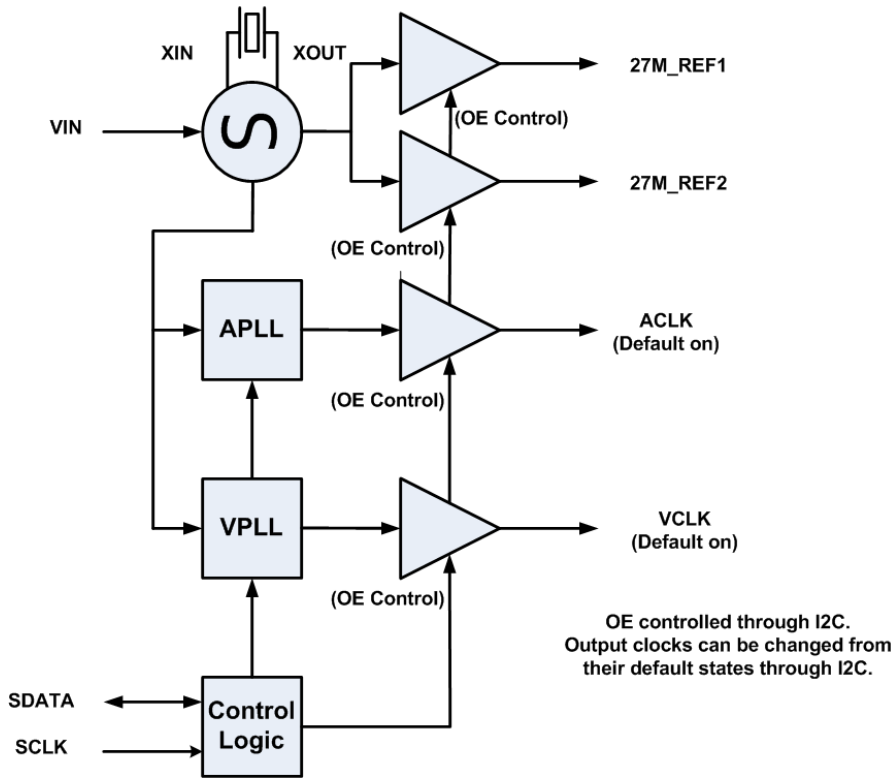
### Description

The SL38160AZC-17AH and SL38160AZC-23AH are programmable low power VCXO Clock Generators designed to enable clock recovery and to synthesize the audio and video clocks required for advanced multimedia applications. The product is designed using SpectraLinear proprietary programmable **EProClock™** technology to generate the output clocks.

The product is offered in a space saving 16-pin TSSOP package.

The two parts are identical except for IIC address, where the SL38160AZC-17AH uses D2(hex) while the SL38160AZC-23AH uses DA(hex).

### Block Diagram



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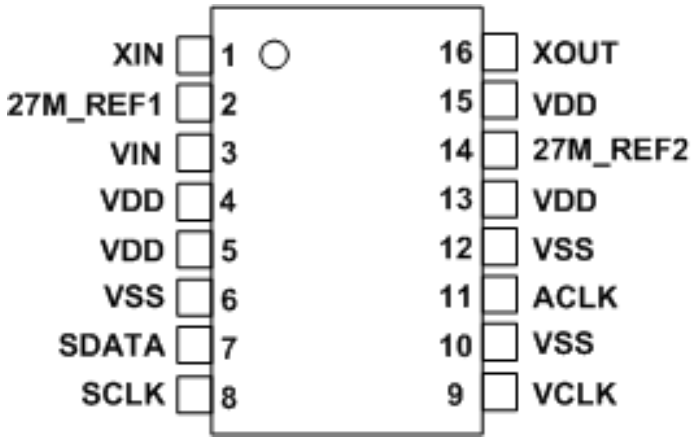
## Pin Configuration




**16-Pin TSSOP Package**

## Pin Description

| Pin Number | Pin Name | Pin Type | Pin Description |
|---|---|---|---|
| 1 | XIN | Input | Crystal oscillator input. Use fundamental parallel mode 27MHz crystal. |
| 2 | 27M_REF1 | Output | 27 MHz reference clock output 1. (Default on) (Can be changed to off/synchronous stop, pulled low to VSS, through I2C) |
| 3 | VIN | Input | VCXO frequency control voltage |
| 4, 5, 13, 15 | VDD | Power | 3.3V +/-10% Positive Power Supply. |
| 6, 10,12 | VSS | Power | Power supply ground for VDD. |
| 7 | SDATA | I/O | I2C Serial Data |
| 8 | SCLK | Input | I2C Clock |
| 9 | VCLK | Output | Video clock output. (Default on) (Can be changed to off/high impedance state through I2C) |
| 11 | ACLK | Output | Audio clock output .(Default on) (Can be changed to off/synchronous stop, pulled low to VSS, through I2C) |
| 14 | 27M_REF2 | Output | 27 MHz reference clock output 2. (Default on) (Can be changed to off/synchronous stop, pulled low to VSS, through I2C) |
| 16 | XOUT | Output | Crystal oscillator output. Use fundamental parallel mode 27MHz crystal. |

## Absolute Maximum Ratings

| Description | Condition | Min | Max | Unit |
|---|---|---|---|---|
| Supply voltage, VDD | | -0.5 | 4.2 | V |
| All Inputs and Outputs | | -0.5 | VDD+0.5 | V |
| Ambient Operating Temperature | In operation | 0 | 70 | °C |
| Ambient Operating Temperature | Industrial grade, in operation | -40 | 85 | °C |
| Storage Temperature | No power is applied | -65 | 150 | °C |
| Junction Temperature | In operation, power is applied | - | 125 | °C |
| Soldering Temperature | | - | 260 | °C |
| ESD Rating (Human Body Model) | JEDEC22-A114D | -4,000 | 4,000 | V |
| ESD Rating (Charge Device Model) | JEDEC22-C101C | -1,500 | 1,500 | V |
| ESD Rating (Machine Model) | JEDEC22-A115D | -250 | 250 | V |
| Moisture Sensitivity Level | JEDEC (J-STD-020) | 1 | | |

**Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.**

## DC Electrical Characteristics

Unless otherwise stated VDD= 3.3V+/-10%, VIN=1.65V, Output Load=15pF and Ambient Temperature range 0 to +70°C for Commercial or -40 to +85°C for Industrial temperature option.

| Description | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Operating Voltage | VDD | 3.3V +/-10% | 2.97 | 3.3 | 3.63 | V |
| Input High Voltage | VIH | | 0.7xVDD | - | - | V |
| Input Low Voltage | VIL | | - | - | 0.3xVDD | V |
| Output High Voltage | VOH | IOH=-6mA | VDD-0.5 | - | - | V |
| Output Low Voltage | VOL | IOL=6mA | - | - | 0.5 | V |
| Operating Supply Current | IDD | Output load = 0pF | - | 20 | 25 | mA |
| VIN Input Impedance | $VIN_R$ | | 1 | - | - | MΩ |
| Input Pull-Down/Up Resistor | | | - | 250 | - | KΩ |

## AC Electrical Characteristics

Unless otherwise stated VDD= 3.3V+/-10%, VIN=1.65V, Output Load=15pF for f<200MHz, 5pF for f>200MHz and Ambient Temperature range 0 to +70°C for Commercial or -40 to +85°C for Industrial temperature option.

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Input Frequency Range | FIN | Crystal input | - | 27 | - | MHz |
| Output Rise Time | Tr | VCLK and ACLK, all frequencies | - | - | 1.5 | ns |
| Output Rise Time | Tr | 27M_REF1,27M_ REF2 clocks | - | - | 2.0 | ns |
| Output Fall Time | Tf | VCLK and ACLK, all frequencies | - | - | 1.5 | ns |
| Output Fall Time | Tf | 27M_REF1,27M_ REF2 clocks | - | - | 2.0 | ns |
| Output Duty Cycle | - | All outputs ,f≤100MHz | 45 | 50 | 55 | % |
| Output Duty Cycle | - | All outputs, f>100MHz | 40 | 50 | 60 | % |
| Output Frequency Synthesis Error | FOUT | All Frequencies except 193.16MHz, which has a +15ppm error | - | - | 0 | ppm |
| Cycle to Cycle Jitter | - | 27M_REF1, 27M_REF2 outputs | - | 160 | 250 | ps |
| Cycle to Cycle Jitter | - | VCLK output | - | 175 | 350 | ps |
| Cycle to Cycle Jitter | - | ACLK output | - | 150 | 250 | ps |
| Long Term Jitter[1] | - | 27M_REF1, 27M_REF2 outputs | - | 85 | 120 | ps-rms |
| Long Term Jitter[1] | - | VCLK output | - | 250 | 700 | ps-rms |
| Long Term Jitter[1] | - | ACLK output | - | 550 | 950 | ps-rms |
| Frequency Settling Time | - | Time before valid clock output after programming frequency via IIC | - | - | 0.5 | ms |
| Power-up Time | $T_{PUP}$ | Time from VDD minimum to valid frequency output | - | - | 5.5 | ms |
| VCXO Pull Range[2] | $\Delta F_{VCXO}$ | Monotonic VCXO Crystal Pull Range | - | +/-150 | - | ppm |

## Recommended Crystal Specifications (for VCXO applications)[2]

| Symbol | Description | Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $F_{NOM}$ | Nominal frequency | Fundamental mode | - | 27 | - | MHz |
| $F_{DELTA25}$ | Frequency tolerance at 25°C | | -20 | - | 20 | ppm |
| $F_{DELTAT}$ | Temperature tolerance | 0 to 70°C (reference to 25°C ) | -20 | - | 20 | ppm |
| $CL_{NOM}$ | Nominal load capacitance | | - | 14 | - | pF |
| R1 | Equivalent series resistance | Fundamental mode (CL=series) | - | 20 | 50 | Ω |
| DL | Drive level | Nominal VDD @25°C over +/-150ppm Pull range | - | - | 500 | uW |
| C0 | Shunt capacitance | | - | 3.0 | 7.0 | pF |

[1] Measured with 1000 samples at 10us delay on oscilloscope
[2] KDS 1C727000CC1K crystal

| | | | | | | |
|---|---|---|---|---|---|---|
| C1 | Motional capacitance | | - | 11.8 | - | fF |
| C0/C1 | Ratio of shunt to motional capacitance | | | | 250 | |
| $F3_{SEPHI}$ | Third overtone separation, high side | Mechanical third (High side of 3xFNOM) | 240 | - | - | ppm |
| $F3_{SEPLO}$ | Third overtone separation, low side | Mechanical third (Low side of 3xFNOM) | - | - | -240 | ppm |

## Serial Data Interface

To enhance the flexibility and function of the device, an I2C compatible interface is provided. Through the Serial Data Interface, various device functions, such as ACLK and VCLK frequency setting and individual clock output buffers can be individually enabled or disabled. The registers associated with the Serial Data Interface initialize to their default setting at power-up. Clock device register changes can be made after the device power up initialization process has completed.

## Data Protocol

The clock driver serial protocol accepts byte write, byte read, block write, and block read operations from the controller. For block write/read operation, Access the bytes in sequential order from lowest to highest (most significant bit first) with the ability to stop after any complete byte is transferred. For byte write and byte read operations, the system controller can access individually indexed bytes. The offset of the indexed byte is encoded in the command code descried in the command code definition section.

The block write and block read protocol is outlined in the block read and block write protocol section, while The byte read and byte write protocol section outlines byte read and byte write information.

The slave receiver address is 11010010 (D2h) for the SL38160AZC-17AH.
The slave receiver address is 11011010 (DAh) for the SL38160AZC-23AH.

## Command Code Definition

| Bit | Description |
|---|---|
| 7 | 0 = Block read or block write operation, 1 = Byte read or byte write operation |
| (6:0) | Byte offset for byte read or byte write operation. For block read or block operations, these bits should be '0000000' |

## Block Read and Block Write Protocol

| Block Write Protocol | | Block Read Protocol | |
|---|---|---|---|
| **Bit** | **Description** | **Bit** | **Description** |
| 1 | Start | 1 | Start |
| 8:2 | Slave address-7bits | 8:2 | Slave address-7bits |
| 9 | Write | 9 | Write |
| 10 | Acknowledge from slave | 10 | Acknowledge from slave |
| 18:11 | Command Code-8bits | 18:11 | Command Code-8bits |
| 19 | Acknowledge from slave | 19 | Acknowledge from slave |
| 27:20 | Byte Count-8bits | 20 | Repeat start |
| 28 | Acknowledge from slave | 27:21 | Slave address-7bits |
| 36:29 | Data byte 1-8bits | 28 | Read = 1 |
| 37 | Acknowledge from slave | 29 | Acknowledge from slave |
| 45:38 | Data byte 2-8bits | 37:30 | Byte Count from slave 8bits |
| 46 | Acknowledge from slave | 38 | Acknowledge |
| … | Data Byte/Slave Acknowledges | 46:39 | Data byte 1 from slave-8bits |
| … | Data Byte N-8bits | 47 | Acknowledge |
| … | Acknowledge from slave | 55:48 | Data byte 2 from slave-8bits |
| … | Stop | 56 | Acknowledge |
| | | … | Data bytes from slave/Acknowledge |
| | | … | Data Byte N from slave-8bits |
| | | … | NOT Acknowledge |
| | | … | Stop |

## Byte Read and Byte Write Protocol

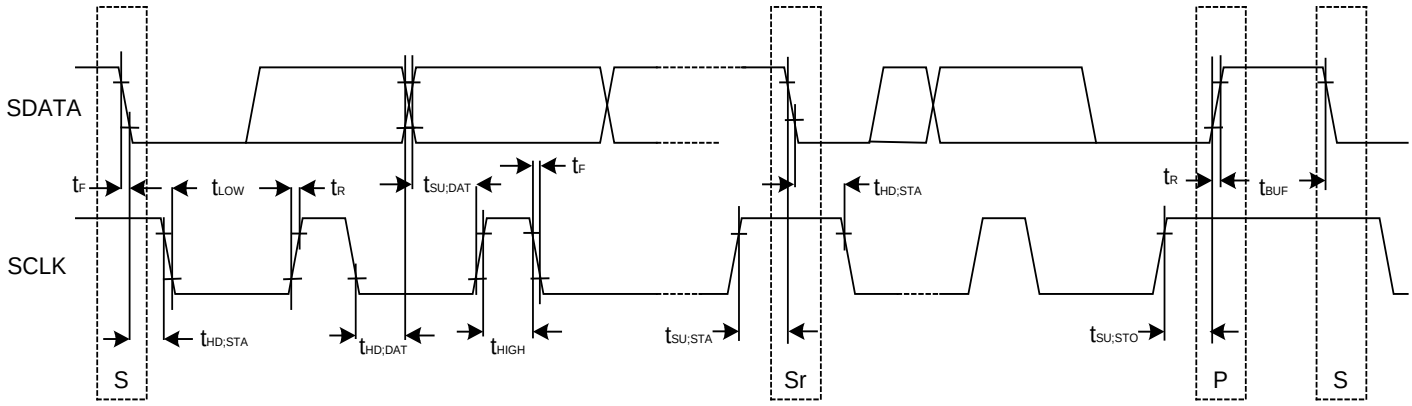
| Byte Write Protocol | | Byte Read Protocol | |
|---|---|---|---|
| **Bit** | **Description** | **Bit** | **Description** |
| 1 | Start | 1 | Start |
| 8:2 | Slave address-7bits | 8:2 | Slave address-7bits |
| 9 | Write | 9 | Write |
| 10 | Acknowledge from slave | 10 | Acknowledge from slave |
| 18:11 | Command Code-8bits | 18:11 | Command Code-8bits |
| 19 | Acknowledge from slave | 19 | Acknowledge from slave |
| 27:20 | Data byte-8bits | 20 | Repeat start |
| 28 | Acknowledge from slave | 27:21 | Slave address-7bits |
| 29 | Stop | 28 | Read |
| | | 29 | Acknowledge from slave |
| | | 37:30 | Byte Count from slave 8bits |
| | | 38 | NOT Acknowledge |
| | | 39 | Stop |

**Note:** When writing to any register bytes between 32d to 63d (20h to 40h), an additional byte outside this range must be written to immediately afterward for proper loading to the register bytes within this range.

## I2C-bus Timing Specification

| PARAMETER | SYMBOL | STANDARD-MODE | | FAST-MODE | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN. | MAX. | MIN. | MAX. | |
| SCL Clock Frequency | $f_{SCL}$ | 0 | 100 | 0 | 400 | KHz |
| START hold time | $t_{HD;STA}$ | 4.0 | - | 0.6 | - | us |
| SCLK LOW period | $t_{LOW}$ | 4.7 | - | 1.3 | - | us |
| SCLK HIGH period | $t_{HIGH}$ | 4.0 | - | 0.6 | - | us |
| START Set-up time | $t_{SU;DAT}$ | 4.7 | - | 0.6 | - | us |

| PARAMETER | SYMBOL | STANDARD-MODE | | FAST-MODE | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN. | MAX. | MIN. | MAX. | |
| SDA set-up time | $t_{SU;DAT}$ | 250 | - | 100 | - | ns |
| SDA/SCLK rise time | $t_R$ | - | 1000 | - | 300 | ns |
| SDA/SCLK fall time | $t_F$ | - | 300 | - | 300 | ns |
| STOP set-up time | $t_{SU;STO}$ | 4.0 | - | 0.6 | - | ns |
| Bus free time | $t_{BUF}$ | 4.7 | - | 1.3 | - | us |



## Table 1. Audio Clock Frequency Settings (pin 11)

| Audio Clk (MHz) | Register Byte# DEC and Bit [7:0] HEX Setting | | | | |
|---|---|---|---|---|---|
| | Byte 40 | Byte 41 | Byte 42 | Byte 43 | Byte129 |
| 8.1920 | 04 | 02 | 1F | 18 | 81 |
| 11.2896 | 0C | 45 | DE | 78 | 81 |
| 12.2880 | 04 | 01 | F6 | 38 | 81 |
| **24.5760[3]** | **04** | **01** | **F5** | **18** | **81** |
| 16.9344 | 09 | 33 | E9 | D8 | 81 |
| 18.4320 | 04 | 01 | F5 | 78 | 81 |
| 36.8640 | 04 | 01 | F4 | B8 | 81 |
| 16.3840 | 08 | 03 | 85 | D8 | 81 |
| 22.5792 | 0C | 45 | DD | 38 | 81 |
| 49.1520 | 08 | 03 | 84 | 98 | 81 |
| 33.8688 | 06 | 21 | F5 | 38 | 81 |
| 73.7280 | 04 | 01 | F4 | 58 | 81 |

## Table 2. Digital Television Video Clock Frequency Settings (pin 9)

| Video Clk (MHz) | Register Byte# (DEC) and Bit [7:0] HEX, Setting | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | Byte17 | Byte18 | Byte19 | Byte22 | Byte48 | Byte49 | Byte 50 | Byte51 | Byte128 |
| 13.50000 | 07 | 80 | AB | C6 | 04 | 00 | 7E | C7 | 34 |
| 27.00000 | 07 | 80 | AB | C6 | 04 | 00 | 5E | C7 | 34 |
| 54.00000 | 07 | 80 | AB | C6 | 04 | 00 | 4E | C7 | 34 |
| **74.17582[3]** | **05** | **80** | **AB** | **DE** | **1F** | **6D** | **86** | **C7** | **36** |
| 74.25000 | 07 | 00 | AB | C6 | 05 | 80 | 86 | C7 | 34 |
| 148.35170 | 05 | 80 | AB | DE | 1F | 6D | 82 | C7 | 36 |
| 148.50000 | 07 | 80 | AB | C6 | 05 | 80 | 82 | C7 | 34 |

[3] Default output frequency on power up

## Table 3. VGA Video Clock Settings (pin 9)[4]

| Screen Resolution | Refresh Rate (Hz) | Video Clock (MHz) | | | | Register Byte# (DEC) and Bit [7:0] HEX, Setting | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Byte 17 | Byte 18 | Byte 19 | Byte 22 | Byte 48 | Byte 49 | Byte 50 | Byte 51 | Byte 68 | Byte 69 | Byte 114 | Byte 128 |
| **640 x 350** | 85 | 31.500 | 07 | 00 | AB | C6 | 08 | C0 | D2 | C7 | 03 | 83 | 3E | 34 |
| **640 x 400** | 85 | 31.500 | 07 | 00 | AB | C6 | 08 | C0 | D2 | C7 | 03 | 83 | 3E | 34 |
| **720 x 400** | 85 | 35.500 | 07 | 00 | AB | C6 | 11 | C1 | 90 | C7 | 03 | 83 | 3E | 34 |
| | 85.04 | 35.000 | 06 | 80 | AB | C6 | 08 | C0 | D0 | C7 | 03 | 83 | 3E | 34 |
| **640 x 480** | 60 | 25.175 | 09 | 00 | 6B | 86 | FB | CF | 22 | C7 | 03 | 83 | 3E | 34 |
| | 72 | 31.500 | 07 | 00 | AB | C6 | 08 | C0 | D2 | C7 | 03 | 83 | 3E | 34 |
| | 75 | 31.500 | 07 | 00 | AB | C6 | 08 | C0 | D2 | C7 | 03 | 83 | 3E | 34 |
| | 85 | 36.000 | 07 | 80 | AB | 66 | 03 | 00 | 50 | C7 | 03 | 83 | 3E | 34 |
| **800 x 600** | 56 | 38.100 | 05 | 80 | AB | C6 | 1F | C2 | 52 | C7 | 03 | 83 | 3E | 34 |
| | 60 | 40.000 | 07 | 00 | AB | C6 | 0A | 00 | D0 | C7 | 03 | 83 | 3E | 34 |
| | 72 | 50.000 | 05 | 80 | AB | C6 | 19 | 02 | 4A | C7 | 03 | 83 | 3E | 34 |
| | 75 | 49.500 | 07 | 00 | AB | C6 | 05 | 80 | 8A | C7 | 03 | 83 | 3E | 34 |
| | 85 | 56.250 | 07 | 80 | AB | C6 | 06 | 40 | 8A | C7 | 03 | 83 | 3E | 34 |
| **1024 x 768** | 43 | 44.900 | 05 | 00 | AB | C6 | 70 | 46 | D2 | C7 | 03 | 83 | 3E | 34 |
| | 60 | 65.000 | 05 | 80 | AB | C6 | 20 | 82 | 4A | C7 | 03 | 83 | 3E | 34 |
| | 70 | 75.000 | 07 | 00 | AB | C6 | 0C | 80 | CA | C7 | 03 | 83 | 3E | 34 |
| | 75 | 78.750 | 07 | 00 | AB | C6 | 08 | C0 | C6 | C7 | 03 | 83 | 3E | 34 |
| | 85 | 94.500 | 0B | 80 | AB | C6 | 03 | 80 | 46 | C7 | 03 | 83 | 3E | 34 |
| **1152 x 864** | 75 | 108.000 | 0B | 80 | AB | C6 | 03 | 00 | 44 | C7 | 03 | 83 | 3E | 34 |
| **1280x768** | 60 | 68.250 | 06 | 80 | 6B | C6 | 16 | C1 | 8A | C7 | 03 | 83 | 3E | 34 |
| | 60 | 79.500 | 06 | 80 | 6B | C6 | 1A | 82 | 46 | C7 | 03 | 83 | 3E | 34 |
| | 75 | 102.200 | 05 | 00 | AB | C6 | 7F | CB | 44 | C7 | 03 | 83 | 3E | 34 |
| | 85 | 117.500 | 06 | 00 | 6B | C6 | 3A | C4 | 84 | C7 | 03 | 83 | 3E | 34 |
| **1360 x 768** | 60 | 85.500 | 06 | 80 | AB | C6 | 09 | 80 | C6 | C7 | 03 | 83 | 3E | 34 |
| **1280 x 960** | 60 | 108.000 | 0B | 80 | AB | C6 | 03 | 00 | 44 | C7 | 03 | 83 | 3E | 34 |
| | 85 | 148.500 | 07 | 00 | AB | C6 | 05 | 80 | 82 | C7 | 03 | 83 | 3E | 34 |
| **1280x1024** | 60 | 108.000 | 0B | 80 | AB | C6 | 03 | 00 | 44 | C7 | 03 | 83 | 3E | 34 |
| | 75 | 135.000 | 07 | 80 | AB | C6 | 03 | C0 | 44 | C7 | 03 | 83 | 3E | 34 |
| | 85 | 157.500 | 06 | 80 | AB | C6 | 08 | C0 | C2 | C7 | 03 | 83 | 3E | 34 |
| **1400x1050** | 60 | 101.000 | 06 | 80 | 6B | C6 | 19 | 42 | 44 | C7 | 03 | 83 | 3E | 34 |
| | 60 | 121.750 | 05 | 00 | 6B | C6 | 79 | C6 | C6 | C7 | 03 | 83 | 3E | 34 |
| | 75 | 156.000 | 07 | 00 | 6B | C6 | 0D | 00 | C4 | C7 | 03 | 83 | 3E | 34 |
| | 85 | 179.500 | 06 | 00 | 6B | C6 | 59 | C6 | C2 | C7 | 03 | 83 | 3E | 34 |
| **1600x1200** | 60 | 162.000 | 07 | 80 | AB | C6 | 03 | 00 | 42 | C7 | 03 | 83 | 3E | 34 |
| | 65 | 175.500 | 07 | 80 | AB | C6 | 03 | 40 | 42 | C7 | 03 | 83 | 3E | 34 |
| | 70 | 189.000 | 07 | 80 | AB | C6 | 03 | 80 | 42 | C7 | 03 | 83 | 3E | 34 |
| | 75 | 202.500 | 07 | 80 | AB | C6 | 03 | C0 | 42 | C7 | 03 | 83 | 3E | 34 |
| | 85 | 229.500 | 07 | 80 | AB | C6 | 04 | 40 | 42 | C7 | 03 | 83 | 3E | 34 |

[4] Pin 9 is the video output clock used for both the Digital Television and VGA Video frequency settings

| Screen Resolution | Refresh Rate (Hz) | Video Clock (MHz) | | | | Register Byte# (DEC) and Bit [7:0] HEX, Setting | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Byte 17 | Byte 18 | Byte 19 | Byte 22 | Byte 48 | Byte 49 | Byte 50 | Byte 51 | Byte 68 | Byte 69 | Byte 114 | Byte 128 |
| **1920x1080i** | 50 | 72.000 | 07 | 80 | AB | C6 | 04 | 00 | 4A | C7 | 03 | 83 | 3E | 34 |
| **1920x1200**[5] | 60 | 154.000 | 06 | 00 | 6B | C6 | 26 | 82 | 44 | C7 | 03 | 83 | 3E | 34 |
| | 60 | 193.160 | 05 | 80 | AB | DE | 32 | F8 | C2 | C7 | 03 | 83 | 3E | 36 |
| | 60 | 193.250 | 05 | 00 | AB | C6 | C1 | 4D | 82 | C7 | 03 | 83 | 3E | 34 |
| | 75 | 245.250 | 06 | 80 | 6B | C6 | 1B | 41 | 82 | C7 | 03 | 83 | 3E | 34 |
| | 85 | 281.250 | 06 | 80 | 6B | C6 | 1F | 43 | 00 | C7 | 0F | C3 | BE | 34 |
| **1792x 1344** | 60 | 204.750 | 31 | 00 | AB | C6 | 16 | C1 | 82 | C7 | 03 | 83 | 3E | 34 |
| | 75 | 261.000 | 07 | 00 | AB | C6 | 07 | 40 | C0 | C7 | 0F | C3 | BE | 34 |
| **1856x1392** | 60 | 218.250 | 31 | 00 | AB | C6 | 18 | 41 | 82 | C7 | 03 | 83 | 3E | 34 |
| | 75 | 288.000 | 07 | 00 | AB | C6 | 08 | 00 | C0 | C7 | 0F | C3 | BE | 34 |
| **1920x 1440** | 60 | 234.000 | 31 | 80 | AB | C6 | 0D | 00 | C2 | C7 | 03 | 83 | 3E | 34 |
| | 75 | 297.000 | 07 | 00 | AB | C6 | 05 | 80 | 80 | C7 | 0F | C3 | BE | 34 |

[5] 15ppm synthesis error

## Table 4. Output Control

| Output | Byte to change | Enable | Disable |
|---|---|---|---|
| REF-1 | 64d | **04h**[6] | 08h |
| VCLK | 117d | **00h**[6] | 04h |
| ACLK | 86d | **04h**[6] | 08h |
| REF-2 | 96d | **04h**[6] | 08h |

## Table 5. Power Down Control

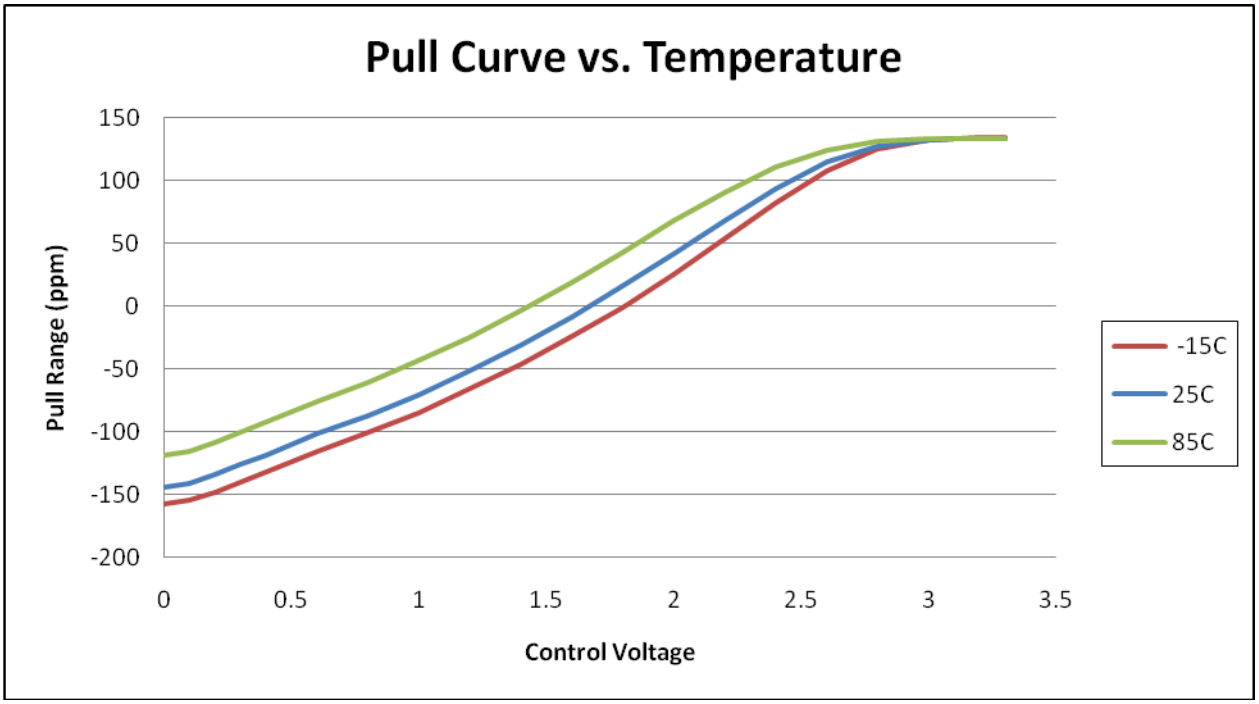
| Byte to change | Active Mode | Powerdown Mode |
|---|---|---|
| 29d | **16h**[6] | 36h |

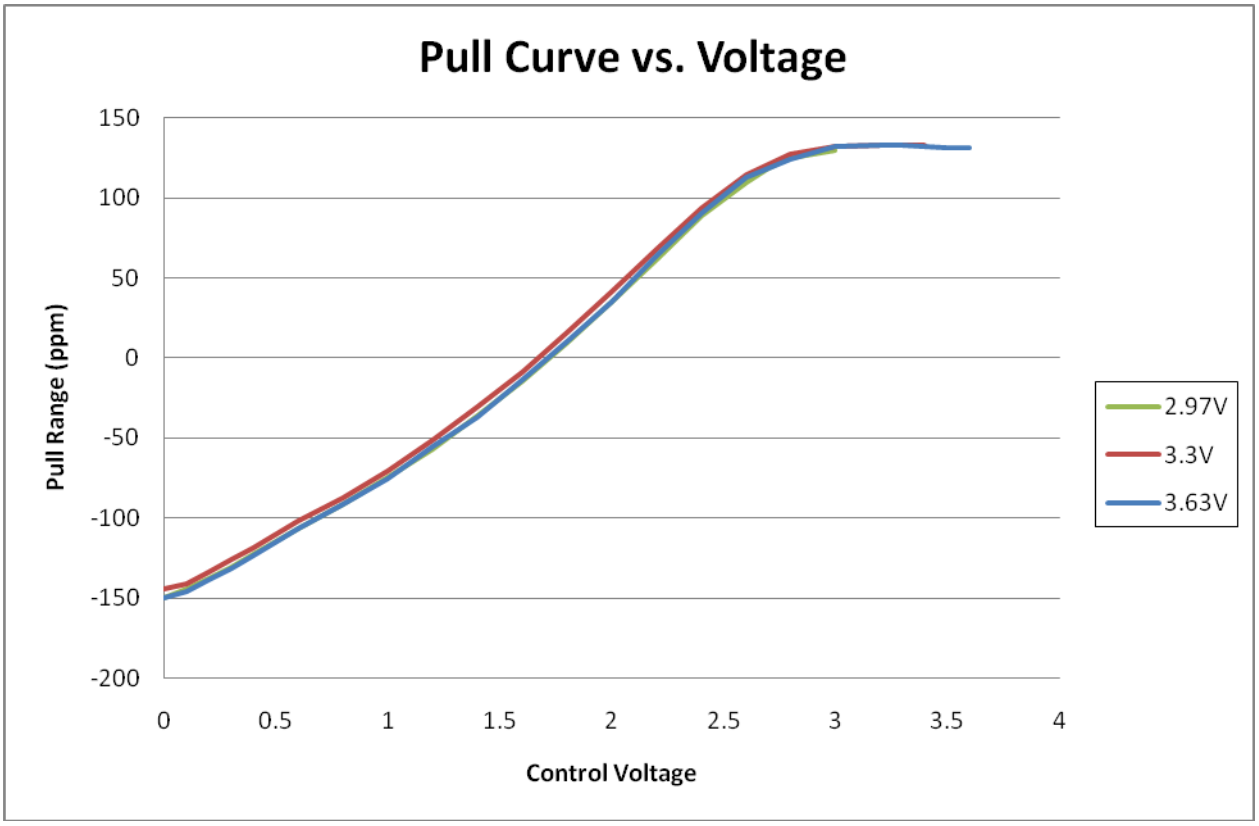
## Table 6. Additional Bytes to Program

| Byte to change | Value |
|---|---|
| 126d | 26h |
| 130d | 53h |

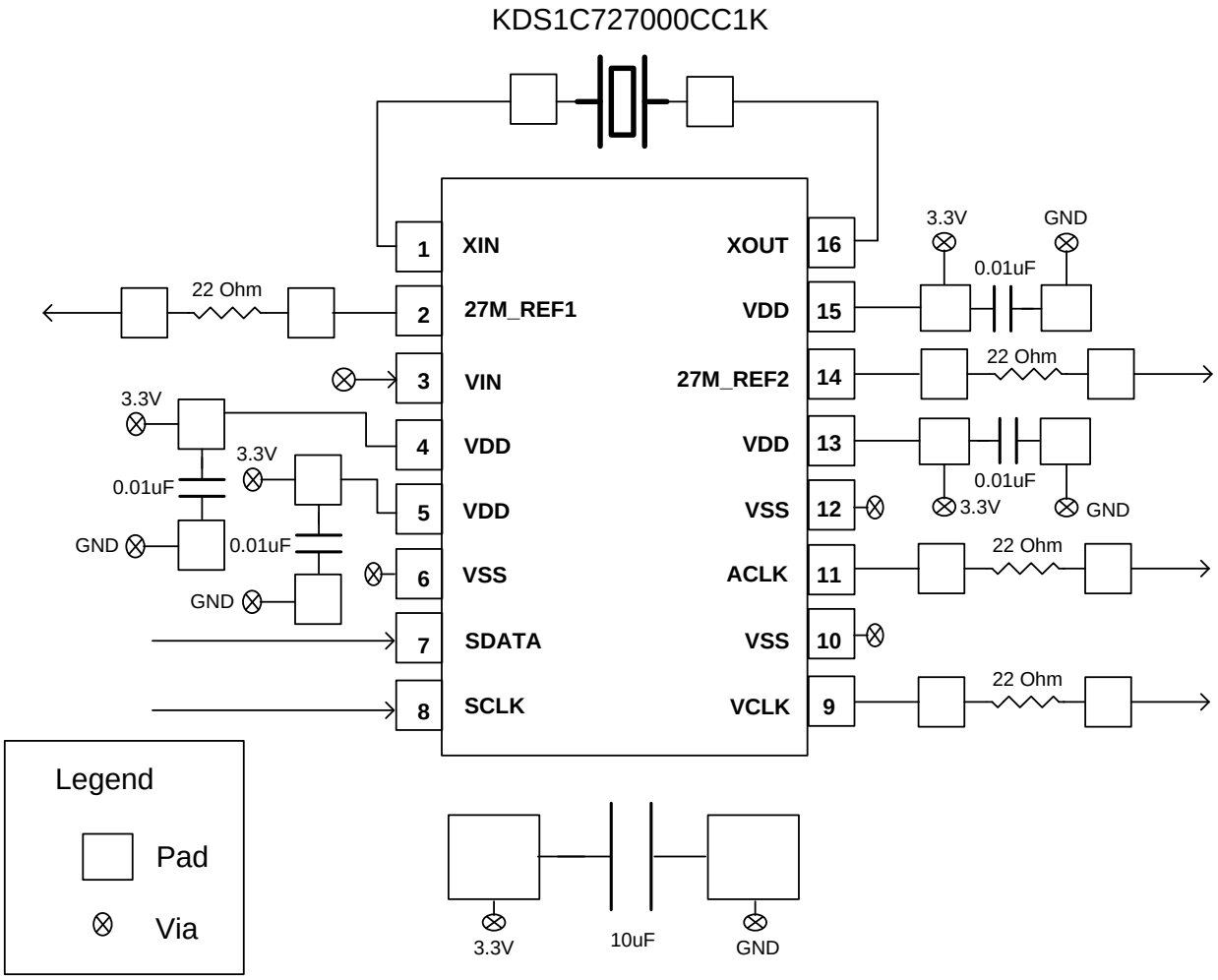
Note: these bytes should be programmed once after device power up.

[6] Default condition


Pull Curve vs. Temperature
Pull Range (ppm)
150
100
50
0
-50
-100
-150
-200
0
0.5
1
1.5
2
2.5
3
3.5
Control Voltage
-15C
25C
85C


Pull Curve vs. Voltage
Pull Range (ppm)
150
100
50
0
-50
-100
-150
-200
0
0.5
1
1.5
2
2.5
3
3.5
4
Control Voltage
2.97V
3.3V
3.63V

## Typical Application Circuit

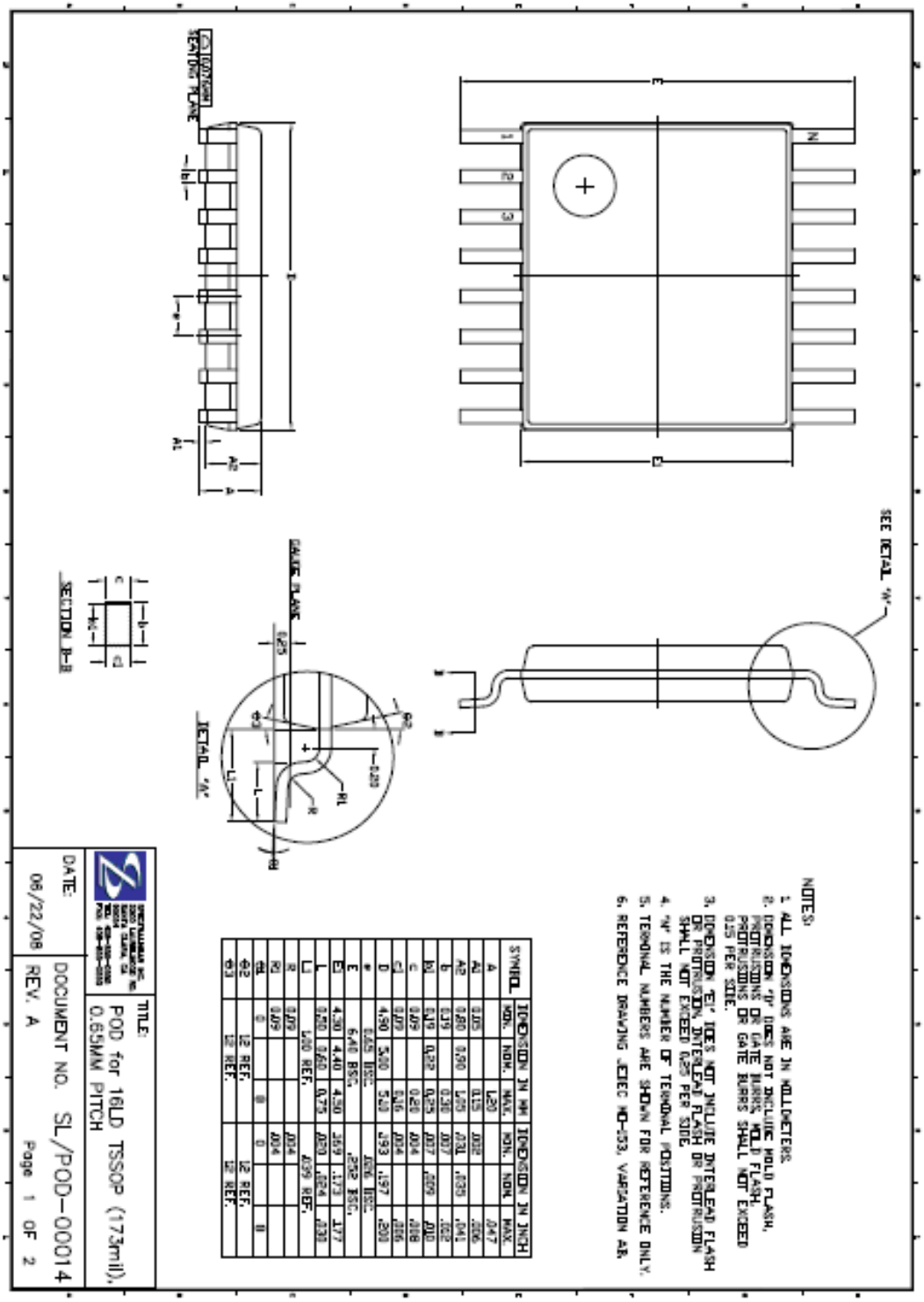



## General Guidelines:

1. Place crystal on same side of the board.
2. Place 0.01µF capacitors as close as possible to the power pin.
3. Install one bulk capacitor (10µF). Note that this filtered power should connect to the 0.01µF capacitor pads first. This is known as pin-cap-via.
4. The 22 Ohm series resistors placed on clock outputs are board dependent. This is a nominal value for 50 Ohm impedance boards. Never share ground vias.
5. It is preferable to have a ground flood directly underneath the part.
6. If PCB process takes advantage of via-in-pad technology, then it is recommended that the ground side of all bypass capacitors have the GND via placed inside the pad to lower inductance to ground.

## Package Outline and Package Dimensions

16-Pin TSSOP Package (4.4mm)



## Thermal Characteristics

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Thermal Resistance Junction to Ambient | **θ JA** | Still air | **-** | **80** | **-** | **°C/W** |
| | **θ JA** | 1m/s air flow | **-** | **70** | **-** | **°C/W** |
| | **θ JA** | 3m/s air flow | **-** | **68** | **-** | **°C/W** |
| Thermal Resistance Junction to Case | **θ JC** | Independent of air flow | **-** | **36** | **-** | **°C/W** |

## Ordering Information

| Ordering Number | Marking | Shipping Package | Package | Temperature |
|---|---|---|---|---|
| SL38160AZC-17AH | SL38160AZC-17AH | Tube | 16-pin TSSOP | 0 to 70°C |
| SL38160AZC-17AHT | SL38160AZC-17AH | Tape and Reel | 16-pin TSSOP | 0 to 70°C |
| SL38160AZC-23AH | SL38160AZC-23AH | Tube | 16-pin TSSOP | 0 to 70°C |
| SL38160AZC-23AHT | SL38160AZC-23AH | Tape and Reel | 16-pin TSSOP | 0 to 70°C |
| SL38160AZI-17AH | SL38160AZI-17AH | Tube | 16-pin TSSOP | -40 to 85°C |
| SL38160AZI-17AHT | SL38160AZI-17AH | Tape and Reel | 16-pin TSSOP | -40 to 85°C |
| SL38160AZI-23AH | SL38160AZI-23AH | Tube | 16-pin TSSOP | -40 to 85°C |
| SL38160AZI-23AHT | SL38160AZI-23AH | Tape and Reel | 16-pin TSSOP | -40 to 85°C |

Notes:

1. All SLI products are RoHS compliant.

## Document History Page

| REV. | Issue Date | Originator | Description of change |
|---|---|---|---|
| A.1.0 | 7/8/10 | D. Christenberry | Create initial datasheet as advance information. |
| B.1.0 | 9/2/10 | D. Christenberry | Final datasheet |
| B. 1.1 | 10/5/10 | D. Christenberry | New frequency support added per customer, also updated package drawing |
| B.1.2 | 10/14/10 | D. Christenberry | Updated cy-cy jitter specifications |
| AA | 10/28/10 | D. Christenberry | Release version. Added additional bytes, 5pF load condition for f>200Mz |
| AB | 1/16/11 | D. Christenberry | Added Industrial temperature operation |