

N-channel 800 V, 0.19 Ω typ., 19.5 A MDmesh™ K5 Power MOSFETs
in D²PAK, TO-220FP, TO-220 and TO-247 packages

Datasheet – production data

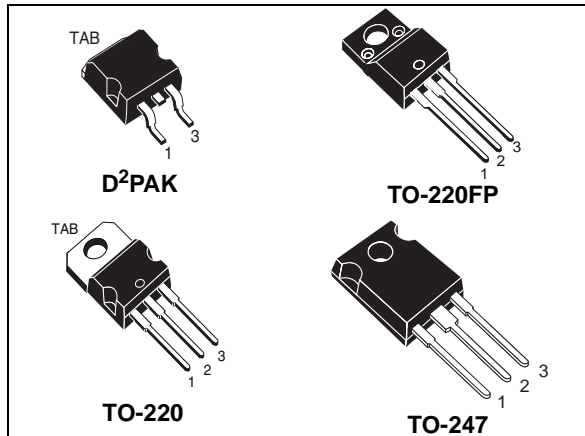
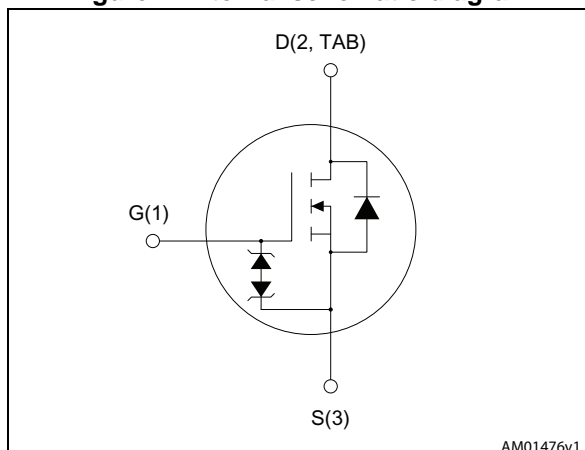


Figure 1. Internal schematic diagram



Features

Order code	V_{DS} @ T_{Jmax}	$R_{DS(on)}$ max	I_D	P_{TOT}
STB25N80K5	800 V	< 0.260 Ω	19.5 A	250 W
STF25N80K5				40 W
STP25N80K5				250 W
STW25N80K5				

- Industry's lowest $R_{DS(on)}$ x area
- Industry's best figure of merit (FoM)
- Ultra low gate charge
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

These very high voltage N-channel Power MOSFETs are designed using MDmesh™ K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

Table 1. Device summary

Order code	Marking	Package	Packaging
STB25N80K5	25N80K5	D ² PAK	Tape and reel
STF25N80K5		TO-220FP	Tube
STP25N80K5		TO-220	
STW25N80K5		TO-247	

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		D ² PAK, TO-220, TO-247	TO-220FP	
V _{GS}	Gate- source voltage	± 30		V
I _D	Drain current (continuous) at T _C = 25 °C	19.5	19.5 ⁽¹⁾	A
I _D	Drain current (continuous) at T _C = 100 °C	12.3	12.3 ⁽¹⁾	A
I _{DM} ⁽²⁾	Drain current (pulsed)	78	78 ⁽¹⁾	A
P _{TOT}	Total dissipation at T _C = 25 °C	250	40	W
I _{AR}	Max current during repetitive or single pulse avalanche (pulse width limited by T _{jmax})	6.5		A
E _{AS}	Single pulse avalanche energy (starting T _J = 25 °C, I _D =I _{AS} , V _{DD} = 50 V)	200		mJ
V _{iso}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t=1 s; T _C =25 °C)		2500	V
dv/dt ⁽³⁾	Peak diode recovery voltage slope	6		V/ns
T _j T _{stg}	Operating junction temperature Storage temperature	-55 to 150		°C

- Limited by package.
- Pulse width limited by safe operating area.
- $I_{SD} \leq 19.5$ A, $di/dt \leq 100$ A/ μ s, $V_{Peak} \leq V_{(BR)DSS}$

Table 3. Thermal data

Symbol	Parameter	Value				Unit
		TO-220	TO-247	D ² PAK	TO-220FP	
R _{thj-case}	Thermal resistance junction-case max	0.5			3.1	°C/W
R _{thj-amb}	Thermal resistance junction-amb max	62.5	50		62.5	
R _{thj-pcb} ⁽¹⁾	Thermal resistance junction-pcb max			30		

- When mounted on 1inch² FR-4 board, 2 oz Cu.

2 Electrical characteristics

($T_{CASE} = 25\text{ °C}$ unless otherwise specified).

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage ($V_{GS} = 0$)	$I_D = 1\text{ mA}$	800			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = 800\text{ V}$			1	μA
		$V_{DS} = 800\text{ V}, T_C = 125\text{ °C}$			50	μA
I_{GSS}	Gate body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20\text{ V}$			± 10	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 100\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}, I_D = 10\text{ A}$		0.19	0.260	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 100\text{ V}, f = 1\text{ MHz}, V_{GS} = 0$	-	1600	-	pF
C_{oss}	Output capacitance		-	130	-	pF
C_{rss}	Reverse transfer capacitance		-	2	-	pF
$C_{o(tr)}^{(1)}$	Equivalent capacitance time related	$V_{GS} = 0, V_{DS} = 0\text{ to }640\text{ V}$	-	185	-	pF
$C_{o(er)}^{(2)}$	Equivalent capacitance energy related		-	300	-	pF
R_G	Intrinsic gate resistance	$f = 1\text{ MHz open drain}$	-	4	-	Ω
Q_g	Total gate charge	$V_{DD} = 640\text{ V}, I_D = 19.5\text{ A}$ $V_{GS} = 10\text{ V}$ (see Figure 19)	-	40	-	nC
Q_{gs}	Gate-source charge		-	10		nC
Q_{gd}	Gate-drain charge		-	25		nC

1. Time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}
2. Energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 400\text{ V}$, $I_D = 10\text{ A}$, $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ (see Figure 21)	-	25	-	ns
t_r	Rise time		-	13	-	ns
$t_{d(off)}$	Turn-off delay time		-	60	-	ns
t_f	Fall time		-	15	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		19.5	A
I_{SDM}	Source-drain current (pulsed)		-		78	A
$V_{SD}^{(1)}$	Forward on voltage	$I_{SD} = 19.5\text{ A}$, $V_{GS} = 0$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 19.5\text{ A}$, $V_{DD} = 60\text{ V}$ $di/dt = 100\text{ A}/\mu\text{s}$, (see Figure 20)	-	515		ns
Q_{rr}	Reverse recovery charge		-	11		μC
I_{RRM}	Reverse recovery current		-	43.2		A
t_{rr}	Reverse recovery time	$I_{SD} = 19.5\text{ A}$, $V_{DD} = 60\text{ V}$ $di/dt = 100\text{ A}/\mu\text{s}$, $T_J = 150\text{ }^\circ\text{C}$ (see Figure 20)	-	615		ns
Q_{rr}	Reverse recovery charge		-	13		μC
I_{RRM}	Reverse recovery current		-	43		A

1. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

Table 8. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	$I_{GS} = \pm 1\text{ mA}$, $I_D = 0$	30	-	-	V

The built-in back-to-back Zener diodes have been specifically designed to enhance the ESD capability of the device. The Zener voltage is appropriate for efficient and cost-effective intervention to protect the device integrity. These integrated Zener diodes thus eliminate the need for external components.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for D²PAK

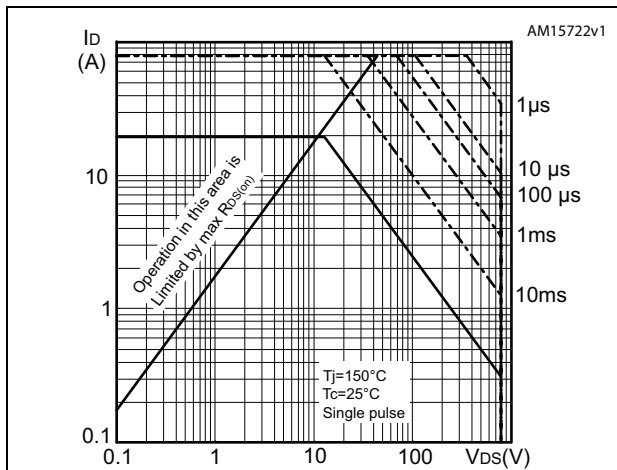


Figure 3. Thermal impedance for D²PAK and TO-220

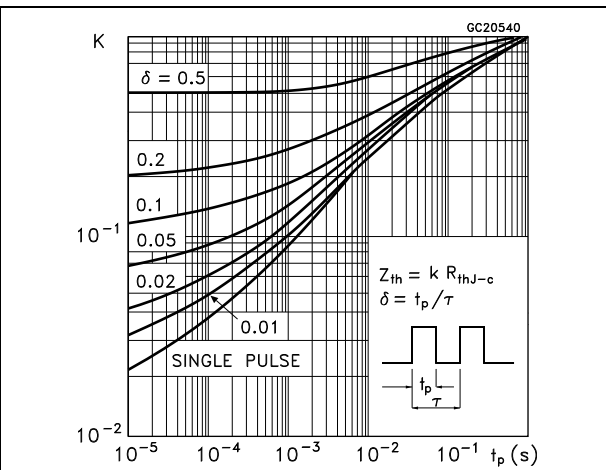


Figure 4. Safe operating area for TO-220FP

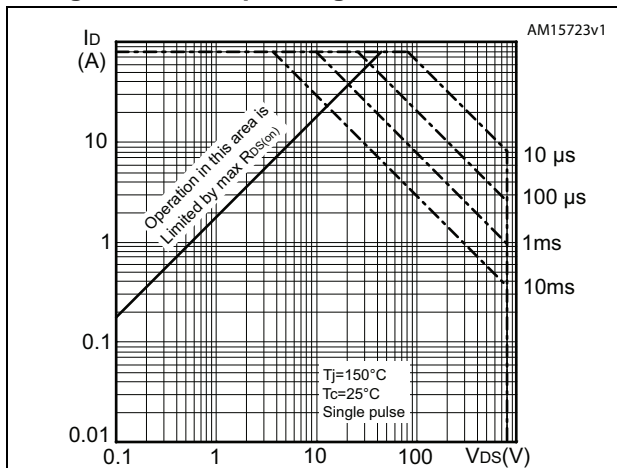


Figure 5. Thermal impedance for TO-220FP

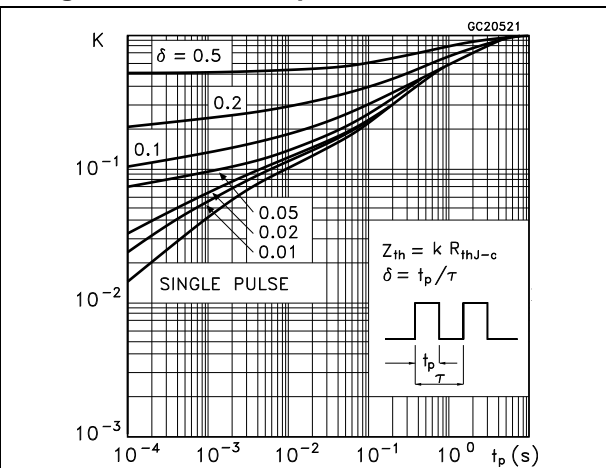


Figure 6. Safe operating area for TO-220

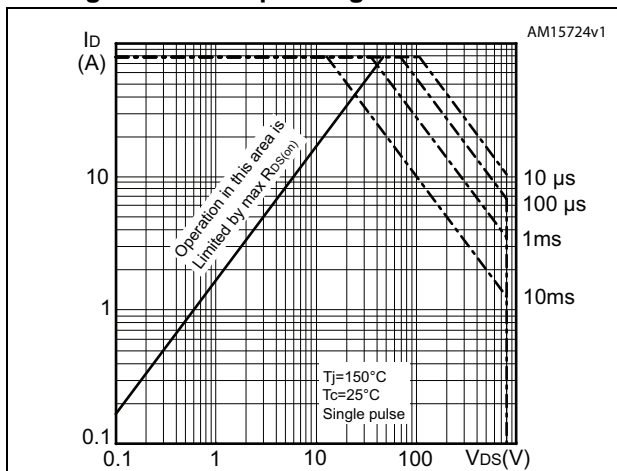


Figure 7. Normalized B_{VDSS} vs temperature

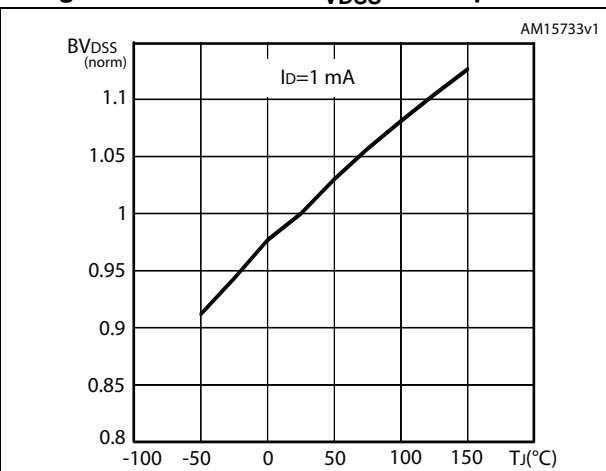


Figure 8. Safe operating area for TO-247

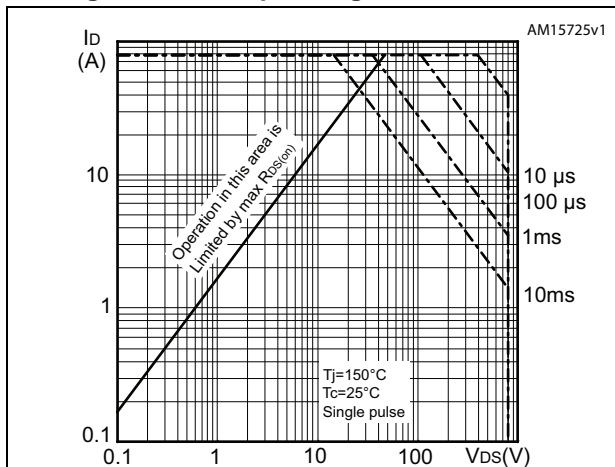


Figure 9. Thermal impedance for TO-247

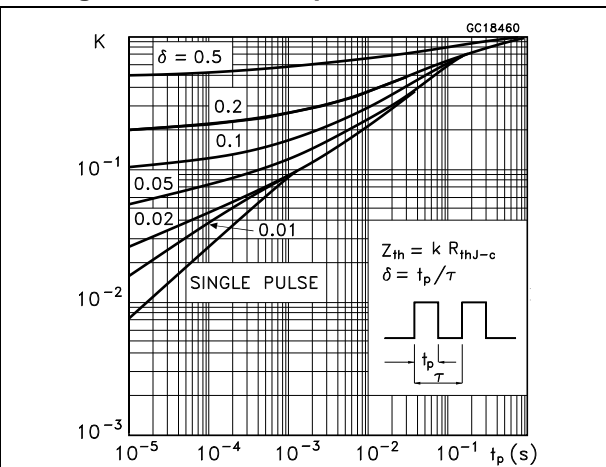


Figure 10. Output characteristics

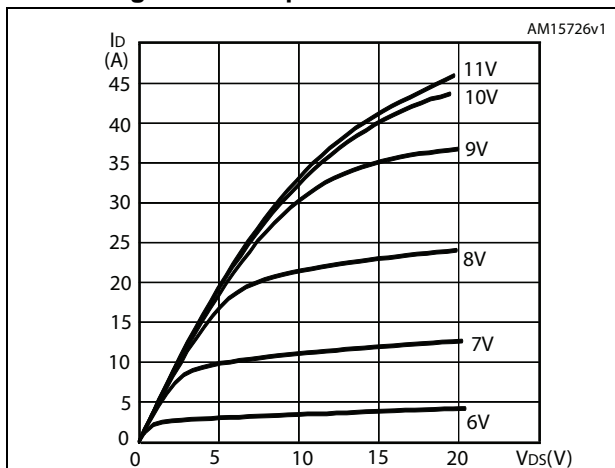


Figure 11. Transfer characteristics

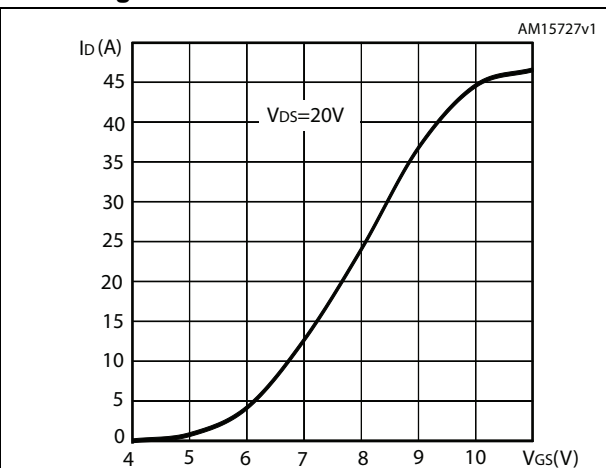


Figure 12. Static drain-source on-resistance

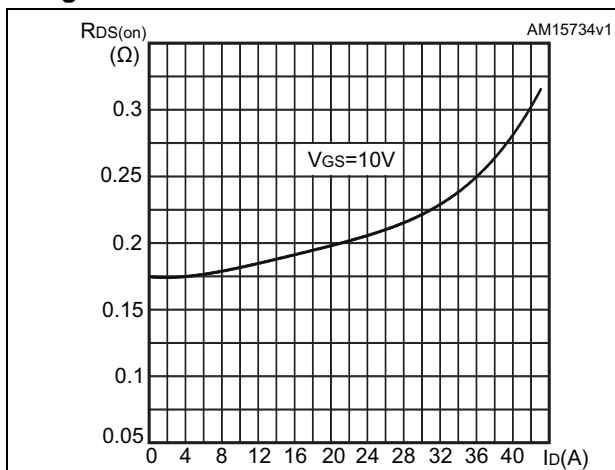


Figure 13. Gate charge vs gate-source voltage

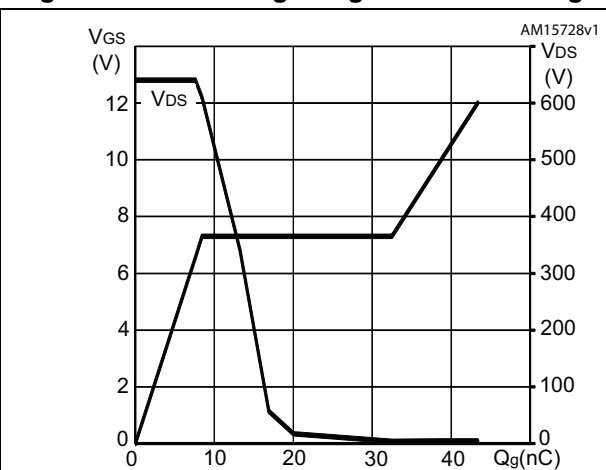


Figure 14. Capacitance variations

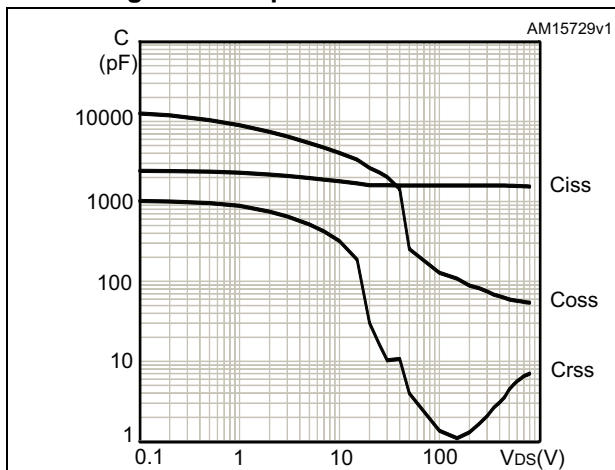


Figure 15. Output capacitance stored energy

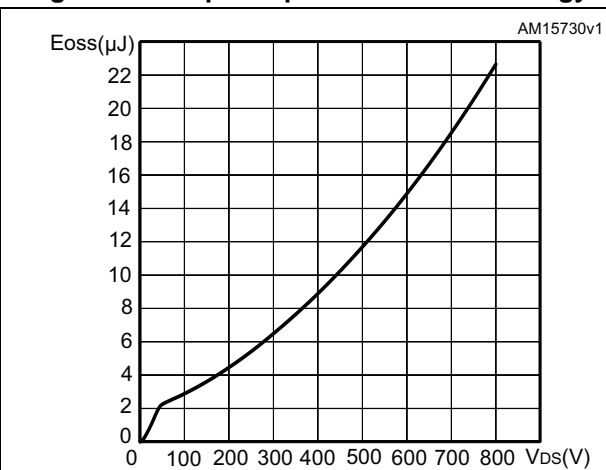


Figure 16. Normalized on-resistance vs temperature

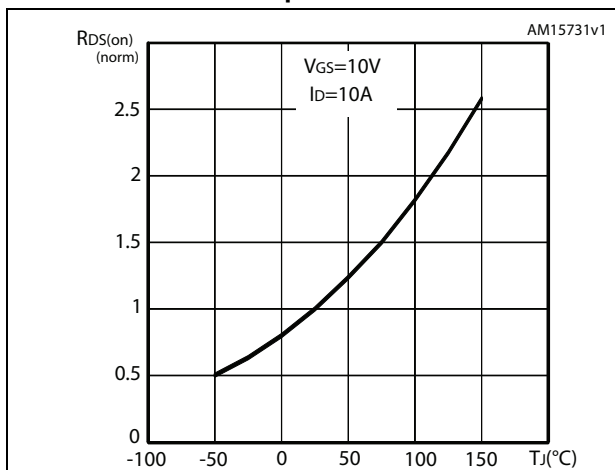
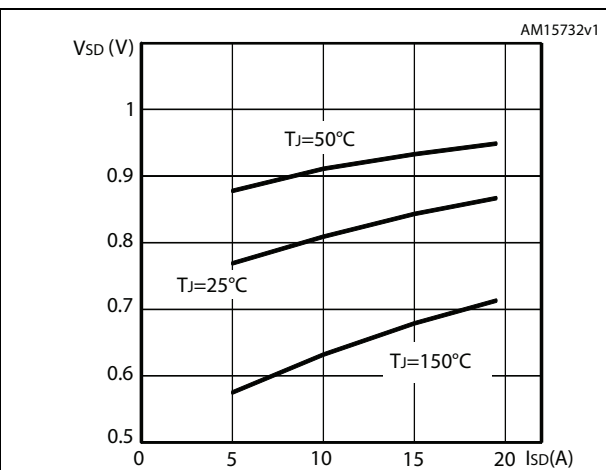
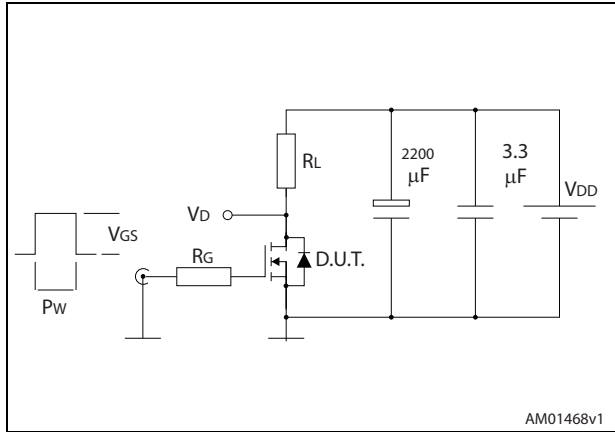


Figure 17. Source-drain diode forward characteristics



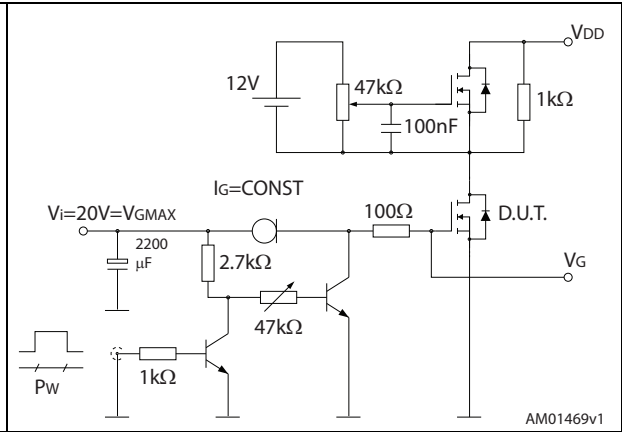
3 Test circuits

Figure 18. Switching times test circuit for resistive load



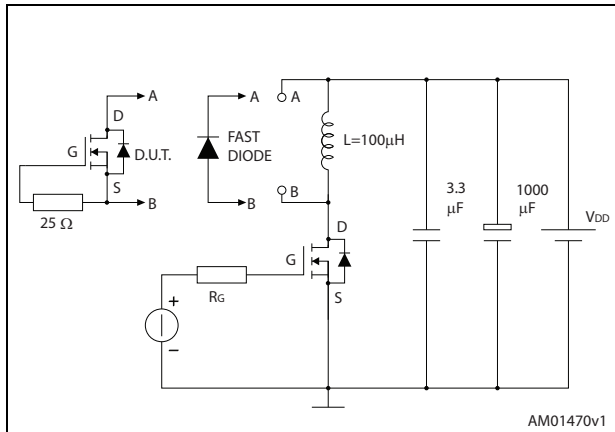
AM01468v1

Figure 19. Gate charge test circuit



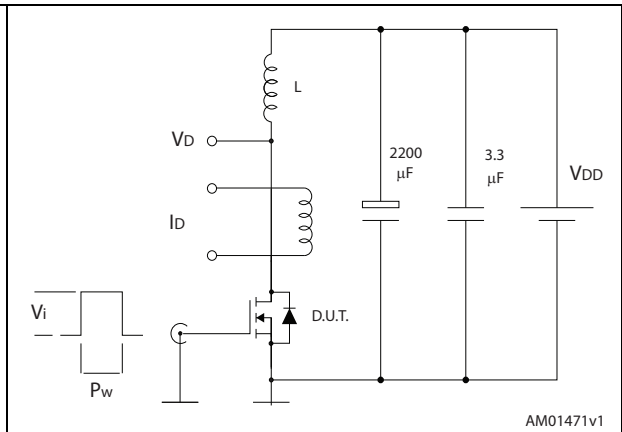
AM01469v1

Figure 20. Test circuit for inductive load switching and diode recovery times



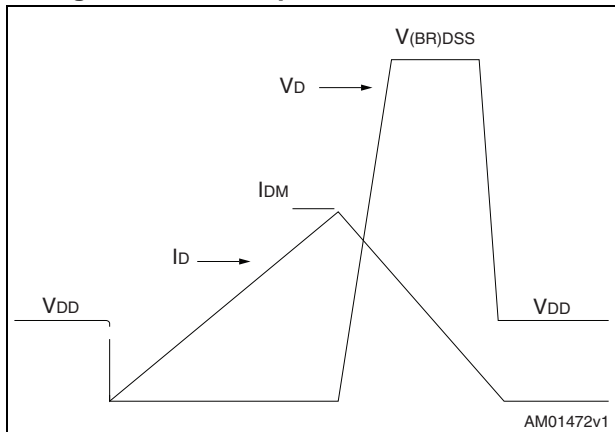
AM01470v1

Figure 21. Unclamped inductive load test circuit



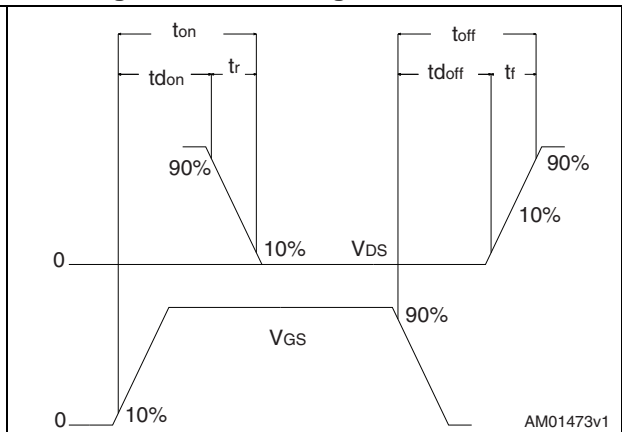
AM01471v1

Figure 22. Unclamped inductive waveform



AM01472v1

Figure 23. Switching time waveform



AM01473v1

4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

4.1 STB25N80K5, D²PAK

Figure 24. D²PAK (TO-263) drawing

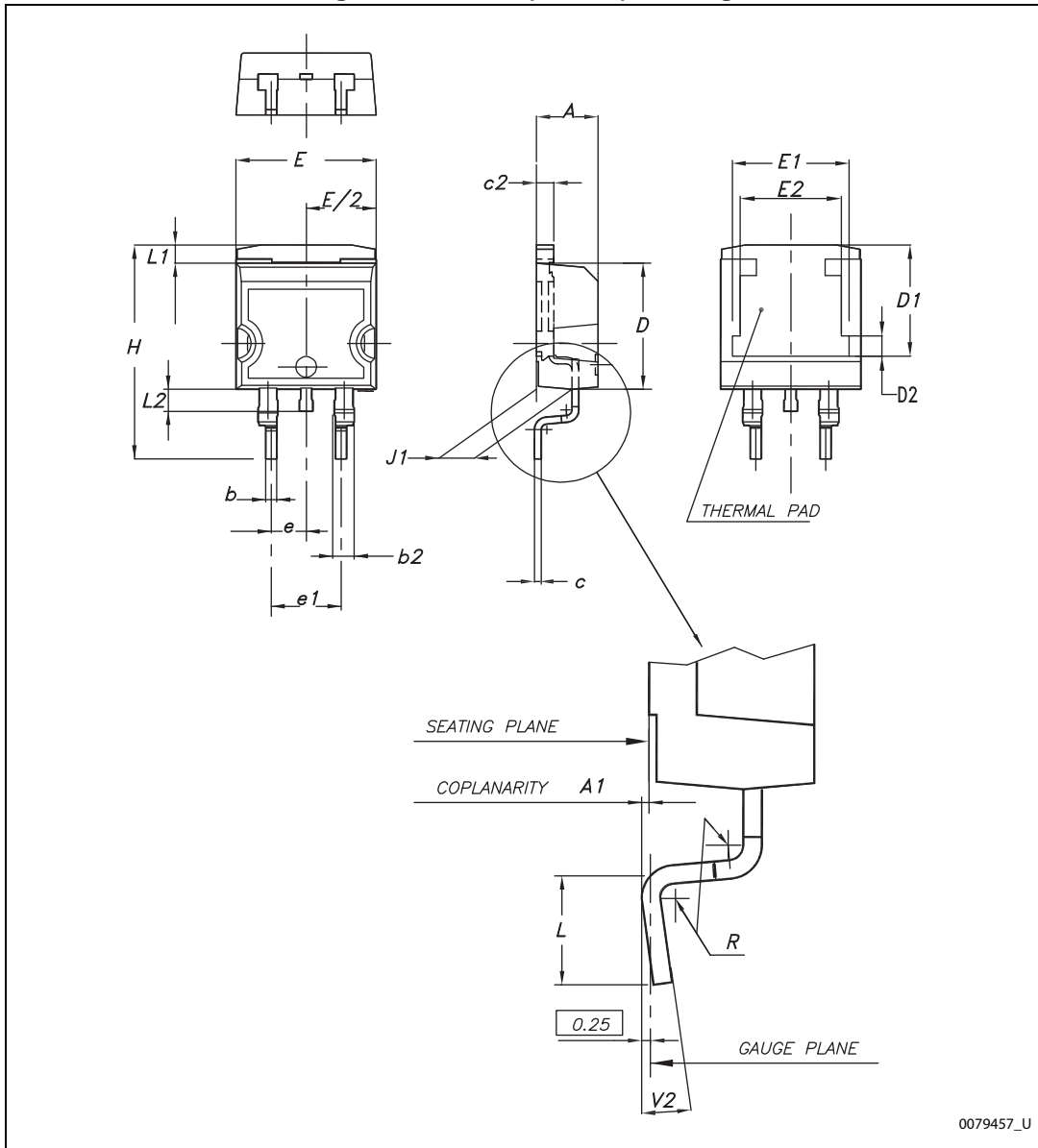
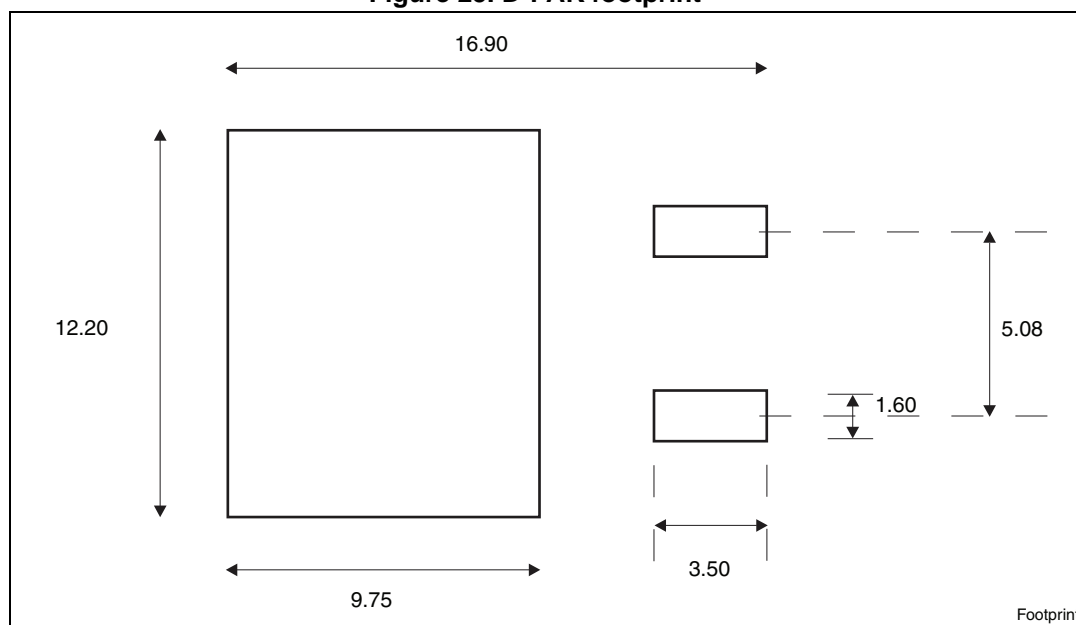


Table 9. D²PAK (TO-263) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50	7.75	8.00
D2	1.10	1.30	1.50
E	10		10.40
E1	8.50	8.70	8.90
E2	6.85	7.05	7.25
e		2.54	
e1	4.88		5.28
H	15		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.4	
V2	0°		8°

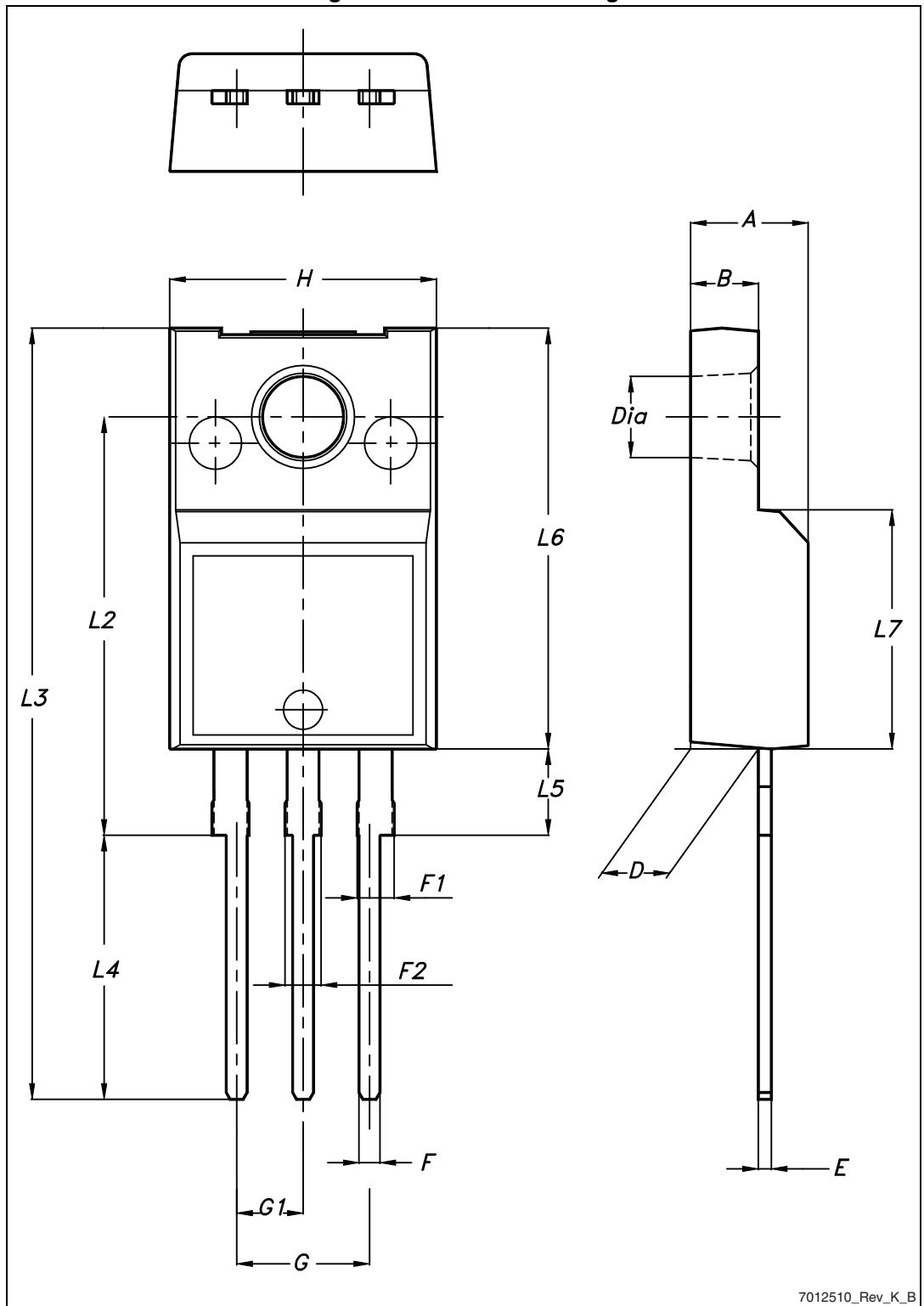
Figure 25. D²PAK footprint^(a)



a. All dimension are in millimeters

4.2 STF25N80K5, TO-220FP

Figure 26. TO-220FP drawing



7012510_Rev_K_B

Table 10. TO-220FP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

4.3 STP25N80K5, TO-220

Figure 27. TO-220 type A drawing

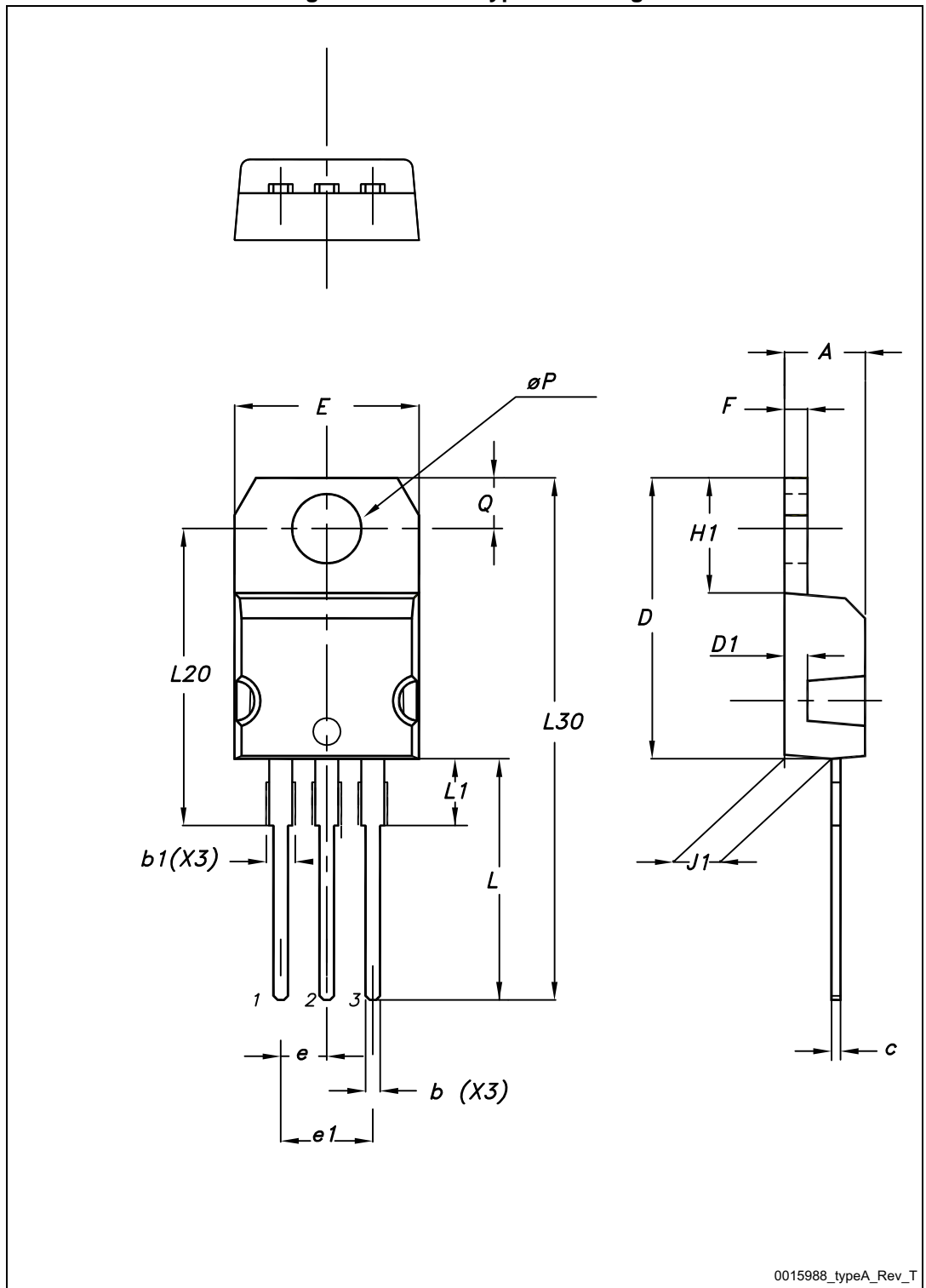


Table 11. TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
∅P	3.75		3.85
Q	2.65		2.95

4.4 STW25N80K5, TO-247

Figure 28. TO-247 drawing

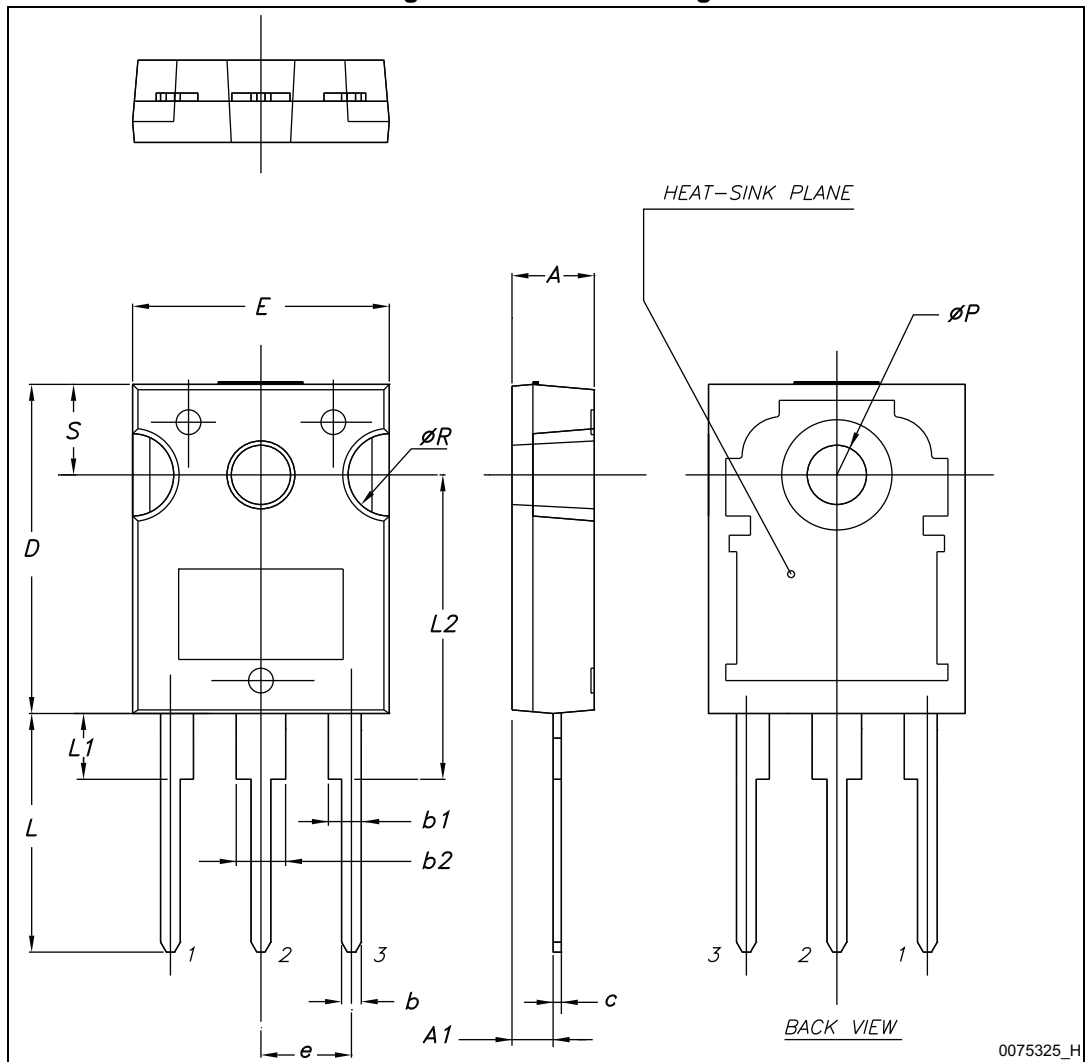


Table 12. TO-247 mechanical data

Dim.	mm.		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70

5 Packaging information

Figure 29. Tape

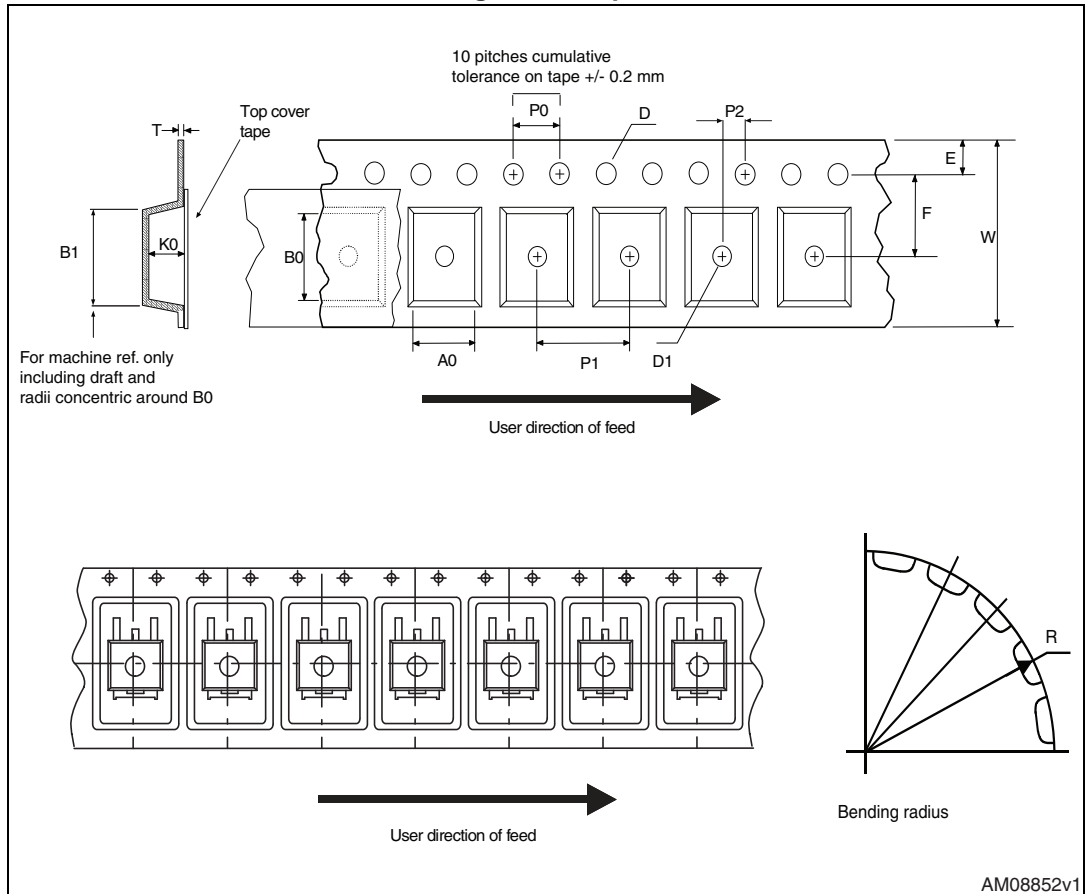


Figure 30. Reel

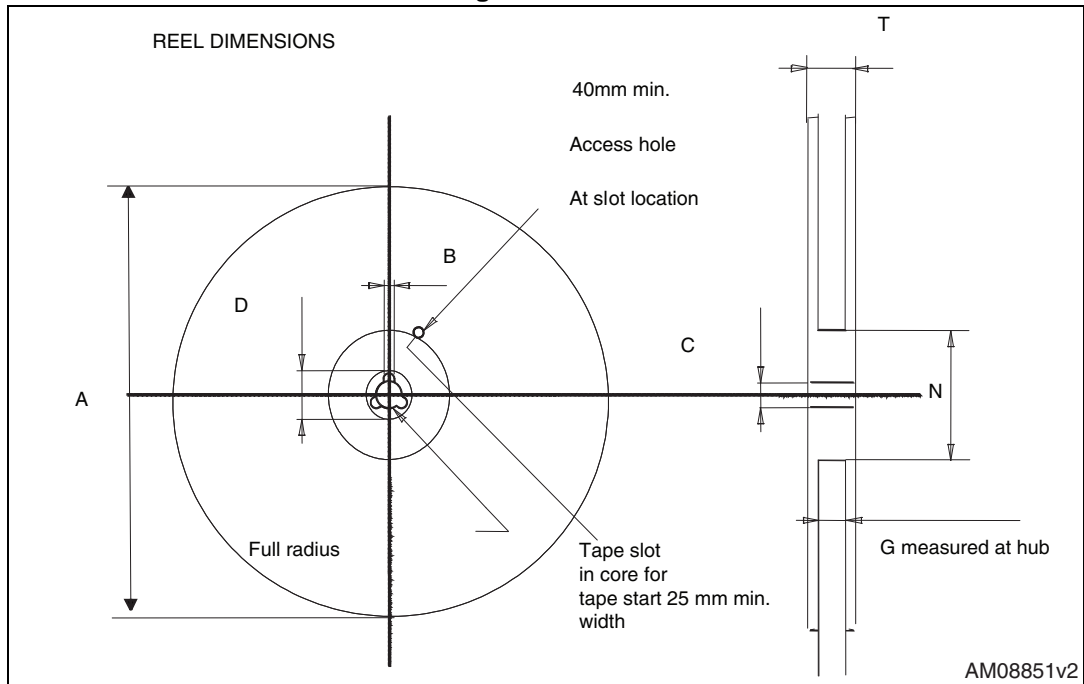


Table 13. D²PAK (TO-263) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1		Base qty	1000
P2	1.9	2.1		Bulk qty	1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

6 Revision history

Table 14. Document revision history

Date	Revision	Changes
17-Jul-2012	1	First release.
04-Jun-2013	2	<ul style="list-style-type: none">– Modified: I_{AR}, E_{AS}, dv/dt on Table 2, $R_{DS(on)}$ value on Table 4, entire values on Table 5, 6 and 7– Updated: Section 4: Package mechanical data– Minor text changes– Updated: Table 11 and Figure 27– Document status promoted from preliminary data to production data
31-Oct-2014	3	<p>Updated title, description and features in cover page. Updated Figure 12: Static drain-source on-resistance. Updated Section 4.1: STB25N80K5, D²PAK and Section 4.4: STW25N80K5, TO-247 Minor text change</p>

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