

# 93Z450/93Z451 1024 x 8-Bit Programmable Read Only Memory

Memory and High Speed Logic

### Description

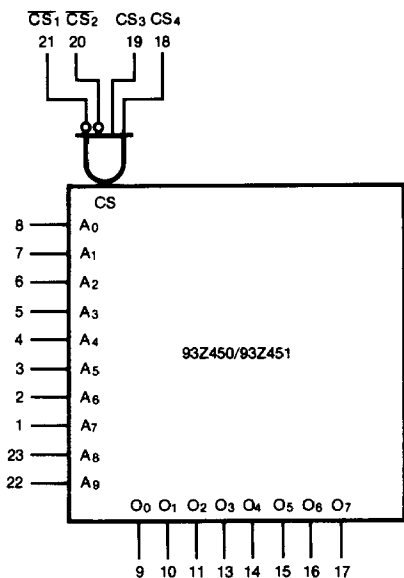
The 93Z450 and 93Z451 are fully decoded 8,192-bit Programmable Read Only Memories (PROMs), organized 1024 words by eight bits per word. The two devices are identical except the 93Z450 has open collector outputs while the 93Z451 has three state outputs. Both devices are available in two speed versions, standard speed and 'A' grade.

- **Commercial Address Access Time**  
93Z450/93Z451 — 40 ns Max  
93Z450A/93Z451A — 35 ns Max
- **Military Address Access Time**  
93Z450/93Z451 — 55 ns Max  
93Z450A/93Z451A — 45 ns Max
- **Highly Reliable Vertical Fuses Ensure High Programming Yields**
- **Available with Open Collector (93Z450) or Three State (93Z451) Outputs**
- **Low Current PNP Inputs**

### Pin Names

A <sub>0</sub> -A <sub>9</sub>	Address Inputs
$\overline{CS}_1, \overline{CS}_2$	Chip Select Inputs (Active LOW)
CS <sub>3</sub> , CS <sub>4</sub>	Chip Select Inputs (Active HIGH)
O <sub>0</sub> -O <sub>7</sub>	Data Outputs

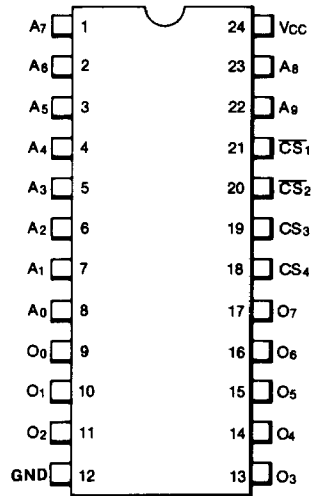
### Logic Symbol



Vcc = Pin 24  
GND = Pin 12

### Connection Diagrams

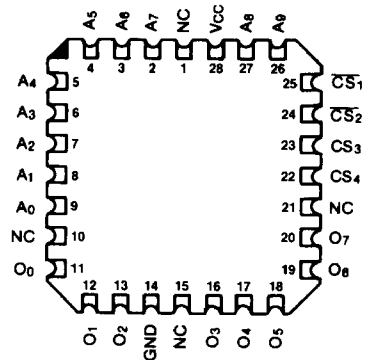
#### 24-pin DIP (Top View)



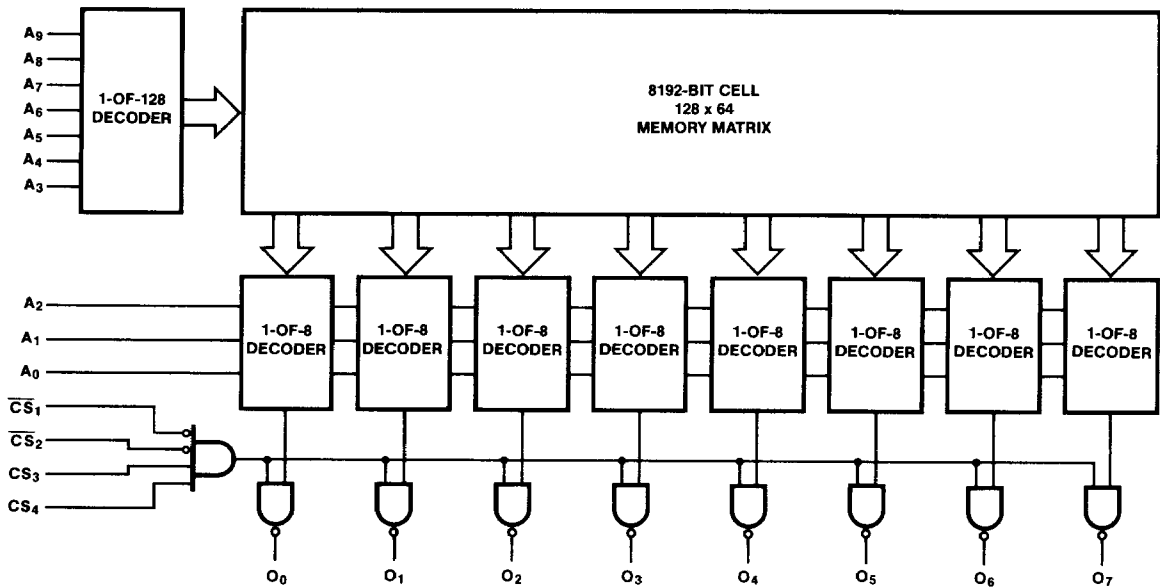
#### Note:

The 24-pin Flatpak has the same pinout (Connection Diagram) as the 24-pin DIP.

#### 28-pin Leadless Chip Carrier (Top View)



## Logic Diagram



## Functional Description

The 93Z450 and 93Z451 are TTL bipolar field Programmable Read Only Memories (PROMs) organized 1024 words by eight bits per word. Open-collector outputs are provided on the 93Z450 for use in wired-OR applications. The 93Z451 has 3-state outputs which provide active pull ups when enabled and high output impedance when disabled. This allows optimization of word expansion in bus organized systems.

Four Chip Select inputs are provided for logic flexibility and for memory array expansion of up to 128K without the need for external decoding. The fast Chip Select access time permits direct address decoding without increasing overall memory access times. Both devices are enabled only when  $\overline{CS}_1$  and  $\overline{CS}_2$  are LOW and  $CS_3$  and  $CS_4$  are HIGH.

The devices contain an internal test row and test column which are accessed and programmed during both wafer sort and final test. These test fuses are used to assure high programmability and to guarantee AC performance and DC parameters.

The 93Z450 and 93Z451 use open base vertical transistor (junction) fuse cells. Initially an unprogrammed cell is in the logic '0' state. Cells can be programmed to a logic '1' state by following the specified programming procedure which fuses aluminum through the emitter base junction of the cell transistor.

The read function is identical to that of a conventional Read Only Memory (ROM). A binary address is applied to the address pins  $A_0$  through  $A_9$  and the chip is selected. Data is then available at the outputs after  $t_{AA}$ .

**DC Performance Characteristics:** Over guaranteed operating ranges unless otherwise noted

Symbol	Characteristic	Min	Typ(1)	Max	Unit	Condition
V <sub>IL</sub>	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
V <sub>IH</sub>	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V <sub>IC</sub>	Input Clamp Diode Voltage			-1.2	V	V <sub>CC</sub> = Min, I <sub>IN</sub> = -18 mA
V <sub>OL</sub>	Output LOW Voltage		0.30	0.45	V	V <sub>CC</sub> = Min, I <sub>OL</sub> = 16 mA
V <sub>OH</sub>	Output HIGH Voltage (93Z451)	2.4			V	V <sub>CC</sub> = Min, I <sub>OH</sub> = -2.0 mA Address Any '1'
I <sub>IL</sub>	Input LOW Current		-10	-100	μA	V <sub>CC</sub> = Max, V <sub>IL</sub> = 0.45 V
I <sub>IH</sub>	Input HIGH Current	-40		40	μA	V <sub>CC</sub> = Max, V <sub>IH</sub> = 2.4 V to V <sub>CC</sub>
I <sub>OHZ</sub> I <sub>OLZ</sub>	Output Leakage Current for High Impedance State (93Z451)			40 -40	μA	V <sub>OH</sub> = 2.4 V V <sub>OL</sub> = 0.4 V
I <sub>CEX</sub>	Output Leakage Current (93Z450)			40	μA	V <sub>CEX</sub> = V <sub>CC</sub> , Chip Deselected
I <sub>OS</sub>	Output Short-Circuit Current (93Z451)	-20	-45	-90	mA	V <sub>CC</sub> = Max, V <sub>O</sub> = 0 V, Note 2 Address Any '1'
I <sub>CC</sub>	Power Supply Current		110	135	mA	V <sub>CC</sub> = Max, Inputs Grounded, Outputs Open

**Commercial**

**AC Performance Characteristics:** V<sub>CC</sub> = 5.0 V ± 5%, GND = 0 V, T<sub>C</sub> = 0°C to +75°C

Symbol	Characteristic	'A'	Std	Unit	Condition
t <sub>AA</sub>	Address to Output Access Time	35	40	ns	See AC Output Load
t <sub>ACS</sub>	Chip Select to Output Access Time	25	30	ns	See AC Output Load

**Military**

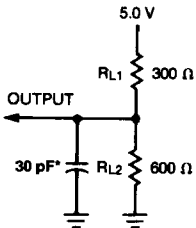
**AC Performance Characteristics:** V<sub>CC</sub> = 5.0 V ± 10%, GND = 0 V, T<sub>C</sub> = -55°C to +125°C

Symbol	Characteristic	'A'	Std	Unit	Condition
t <sub>AA</sub>	Address to Output Access Time	45	55	ns	See AC Output Load
t <sub>ACS</sub>	Chip Select to Output Access Time	30	35	ns	See AC Output Load

1. Typical values are at V<sub>CC</sub> = 5.0 V, T<sub>C</sub> = +25°C.

2. Not more than one output to be shorted at a time. Duration of the short circuit should not exceed one second.

Fig. 1 AC Test Output Load

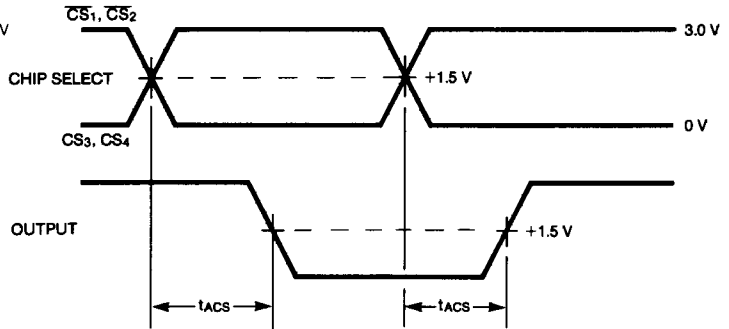
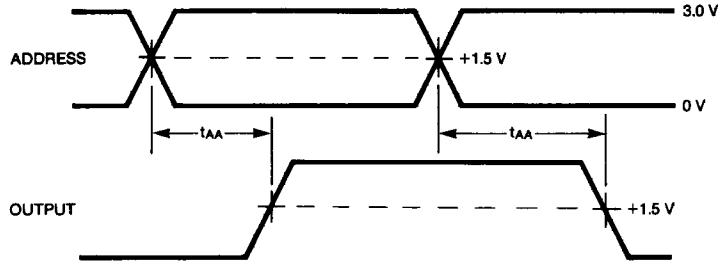


\*Includes jig and probe capacitance

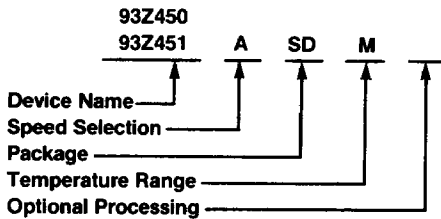
**Test Conditions**

Input pulse: 0 V to 3.0 V  
 Input pulse rise and fall times: 5 ns between 1 V and 2 V  
 Measurements made at 1.5 V level

Fig. 2 AC Waveforms



**Ordering Information**



**Speed Selection**

Blank = Standard Speed  
 A = 'A' Grade

**Packages and Outlines** (See Section 9)

D = 24-pin Ceramic DIP  
 P = 24-pin Plastic DIP (Commercial only)  
 SD = 24-pin Slim Ceramic DIP  
 F = 24-pin Flatpak  
 L = 28-pin Square Leadless Chip Carrier

**Temperature Range**

C = 0°C to +75°C  
 M = -55°C to +125°C

**Optional Processing**

QB = Mil Std 883  
 Method 5004 and 5005, Level B  
 QR = Commercial Device with  
 160 Hour Burn In or Equivalent