HARRIS SEMICONDUCTOR

HM-8808
HM-8808A

8K x 8 Asynchronous CMOS Static RAM Module

January 1992

Features

- Full CMOS Design
- 6 Transistor Memory Cell
- Low Standby Current. 250/900µA
- Low Operating Current 70mA
- Fast Address Access Time 100/120/150ns
- CMOS/TTL Compatible Inputs/Outputs
- JEDEC Approved Pinout
- Equal Cycle and Access Time
- No Clocks or Strobes Required
- Single 5 Volt Supply
- Gated Inputs - No Pull-Up or Pull-Down Resistors Required
- Temperature Range . . . . . -55°C to +125°C
- Easy Microprocessor Interfacing
- Dual Chip Enable Control (HM-8808A)

Description

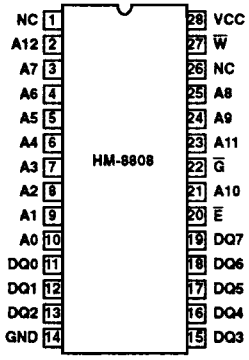
The HM-8808 and HM-8808A are 8K x 8 Asynchronous CMOS Static RAM Modules, based on multi-layered, co-fired, dual-in-line substrates. Mounted on each substrate are four HM-65162 2K x 8 CMOS SRAMs, a high speed CMOS decoder, and a ceramic decoupling capacitor, all packaged in leadless chip carriers. The capacitor is added to reduce noise and the need for external decoupling. The HM-65162 RAMs used in these modules are full CMOS devices, utilizing arrays of six transistor (6T) memory cells for the most stable and lowest possible standby supply current over the full military temperature range. In addition to this, the high stability of the 6T cell provides excellent protection against soft errors due to noise and alpha particles. This stability also improves the radiation tolerance of the RAM over that of four transistor devices. The HM-8808 and HM-8808A have gated inputs to simplify system design for optimum standby supply current. The pinouts of these modules conform to the JEDEC 28 pin 8 bit wide standard, which is compatible with a variety of industry standard memories. The HM-8808A is pin-compatible with many standard 8K x 8 RAMs, adding the advantage of high performance over the full military temperature range. Also, because of the second chip enable (E2), the HM-8808A simplifies the design of low-power battery back-up memory systems.

Ordering Information

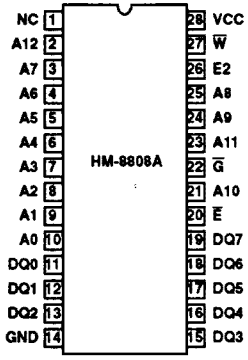
PACKAGE	TEMPERATURE RANGE	100ns	120ns	150ns
MODULE	-55°C to +125°C	HM5-8808S-8	HM5-8808B-8	HM5-8808-8
MODULE	-55°C to +125°C	HM5-8808AS-8	HM5-8808AB-8	HM5-8808A-8

Pinouts

28LEAD MODULE
TOP VIEW

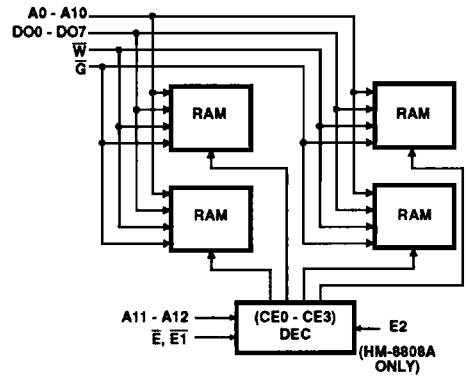


28 LEAD MODULE
TOP VIEW



PIN	DESCRIPTION
A	InputAddress Input
DQ	Data Input/Output
$\overline{E}$	Chip Enable (HM-8808)
$\overline{E1}$	Chip Enable (HM-8808A)
E2	Chip Enable (HM-8808A)
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable

Functional Diagram



6 CMOS MEMORY

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3014

Absolute Maximum Ratings

Supply Voltage . . . . . +7.0V
Input or Output Voltage. . . . . GND-0.3V to VCC+0.3V
Storage Temperature Range . . . . . -65°C to +150°C
Gate Count . . . . . 105000 Gates
Junction Temperature . . . . . +175°C
Lead Temperature (Soldering 10s) . . . . . +300°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range . . . . . +4.5V to +5.5V
Operating Temperature Range . . . . . -55°C to +125°C
Input Rise and Fall Time . . . . . 40ns Max.

DC Electrical Specifications

VCC = 5V ± 10%; T_A = -55°C to +125°C (HM-8808X-8)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS (NOTE 1)
ICCSB1	Standby Supply Current (CMOS)	-	250	µA	HM-8808S/AS-8, HM-8808B/AB-8 IO = 0, $\overline{E}$ = VCC-0.3V (Note 4), E2 = 0.3V (Note 5)
		-	900	µA	HM-8808_/A-8 IO = 0, $\overline{E}$ = VCC-0.3V (Note 4), E2 = 0.3V (Note 5)
ICCSB	Standby Supply Current (TTL)	-	35	mA	IO = 0, $\overline{E}$ = VIH (Note 4), E2 = VIL (Note 5)
ICCEN	Enabled Supply Current	-	60	mA	HM-8808S/AS-8, HM-8808B/AB-8, IO = 0, $\overline{E}$ = VIL (Note 4), E2 = VIH (Note 5)
		-	70	mA	HM-8808_/A-8, IO = 0, $\overline{E}$ = VIL (Note 4), E2 = VIH (Note 5)
ICCOP	Operating Supply Current	-	70	mA	IO = 0, f = 1MHz, $\overline{E}$ = VIL (Note 4), E2 = VIH (Notes 2, 5)
ICCDR	Data Retention Supply Current	-	125	µA	HM-8808S/AS-8, HM-8808B/AB-8, VCC = 2.0V, $\overline{E}$ = VCC-0.3V (Note 4), E2 = 0.3V (Note 5)
		-	400	µA	HM-8808_/A-8, VCC = 2.0V, $\overline{E}$ = VCC-0.3V (Note 4), E2 = 0.3V (Note 5)
II	Input Leakage Current	-1.0	+1.0	µA	VI = GND or VCC
IIOZ	Input/Output Leakage Current	-1.0	+1.0	µA	VIO = GND or VCC
VCCDR	Data Retention Supply Voltage	2.0	-	V	VCC = 2.0V, $\overline{E}$ = VCC (Note 4), E2 = GND (Note 5)
VOL	Output Low Voltage	-	0.4	V	IO = 4.0mA
VOH1	Output High Voltage	2.4	-	V	IO = -1.0mA
VOH2	Output High Voltage	VCC-0.4	-	V	IO = -100mA (Note 3)
VIL	Input Low Voltage	0	0.8	V	
VIH	Input High Voltage	2.4	VCC	V	

Capacitance

T_A = +25°C (Note 3)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
CE	Enable Input Capacitance	-	15	pF	VE = VCC or GND, f = 1MHz (Note 3)
CW	Write Enable Capacitance	-	48	pF	VW = VCC or GND, f = 1MHz (Note 3)
CI	Input Capacitance: $\overline{G}$, A	-	35	pF	VI = VCC or GND, f = 1MHz (Note 3)
CIO	Input/Output Capacitance	-	43	pF	VIO = VCC or GND, f = 1MHz (Note 3)

NOTES:

1. All devices tested at worst case temperature and supply voltage limits.
2. Typical derating = 5mA/MHz increase in ICCOP, VI = VCC or GND.
3. Guaranteed but not tested.
4. Relevant to the HM-8808-8 only.
5. Relevant to the HM-8808A-8 only.

AC Electrical Specifications VCC = 5V 10%; T_A = -55°C to +125°C

SYMBOL	PARAMETER	HM-8808S/AS-8		HM-8808B/AB-8		HM-8808_/A-8		UNITS	(NOTES 1, 2) TEST CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX		
READ CYCLE									
(1) TAVAX	Read Cycle Time	100	-	120	-	150	-	ns	
(2) TAVQV	Address Access Time	-	100	-	120	-	150	ns	
(3) TELQV	Chip Enable Access Time	-	100	-	120	-	150	ns	(Note 4)
(4) TGLQV	Output Enable Access Time	-	50	-	65	-	65	ns	
(5) TELQX	Chip Enable Output Enable Time	20	-	20	-	25	-	ns	(Notes 3, 4)
(6) TGLQX	Output Enable Output Enable Time	5	-	5	-	5	-	ns	(Note 3)
(7) TAXQX	Address Output Hold Time	5	-	5	-	5	-	ns	
(8) TEHQZ	Chip Disable Output Disable Time	0	60	0	70	0	80	ns	(Notes 3, 5)
(9) TGHQZ	Output Disable Time	0	40	0	40	0	50	ns	(Note 3)
WRITE CYCLE									
(10) TAVAX	Write Cycle Time	100	-	120	-	150	-	ns	
(11) TELWH	Chip Enable to End of Write	70	-	80	-	90	-	ns	(Note 4)
(12) TWLWH	Write Enable Pulse Width	40	-	55	-	65	-	ns	
(13) TELEH	Enable Pulse Width (Early Write)	40	-	60	-	65	-	ns	(Notes 3, 4, 5)
(14) TAVWL	Address Setup Time (Late Write)	15	-	15	-	20	-	ns	
(15) TAVEL	Address Setup Time (Early Write)	0	-	0	-	5	-	ns	(Notes 3, 4)
(16) TWHAX	Address Hold Time (Late Write)	10	-	10	-	20	-	ns	
(17) TEHAX	Address Hold Time (Early Write)	30	-	30	-	45	-	ns	(Note 3)
(18) TDVWH	Data Setup Time (Late Write)	30	-	30	-	35	-	ns	
(19) TDVEH	Data Setup Time (Early Write)	30	-	30	-	35	-	ns	(Note 5)
(20) TWHDX	Data Hold Time (Late Write)	10	-	15	-	20	-	ns	
(21) TEHDX	Data Hold Time (Early Write)	30	-	30	-	45	-	ns	(Notes 3, 5)
(22) TWLEH	Write Enable Pulse Setup Time	40	-	55	-	65	-	ns	(Note 5)
(23) TWLQZ	Write Enable Output Disable Time	-	40	-	40	-	50	ns	(Note 3)
(24) TWHQX	Write Disable Output Enable Time	0	-	0	-	0	-	ns	(Note 3)

NOTES:

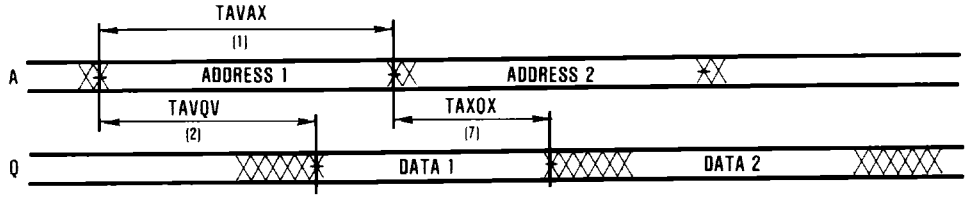
1. All devices tested at worst case temperature and supply voltage limits.
2. Input pulse levels: VIL = 0.0V, VIH = 3.0V Input rise and fall times: 5ns (max.) VCC = 4.5V and 5.5V. Input and output timing reference levels: 1.5V Output load: 1 TTL gate equivalent and 50pF (min, including scope and jig).
3. Guaranteed but not tested.
4. "EL" (enable input valid) equivalent to: EL on the HM-8808-8. EIL and E2H on the HM-8808A-8
5. "EH" (enable input invalid) equivalent to: EH on the HM-8808-8. EIH or E2L on the HM-8808A-8.

Truth Table

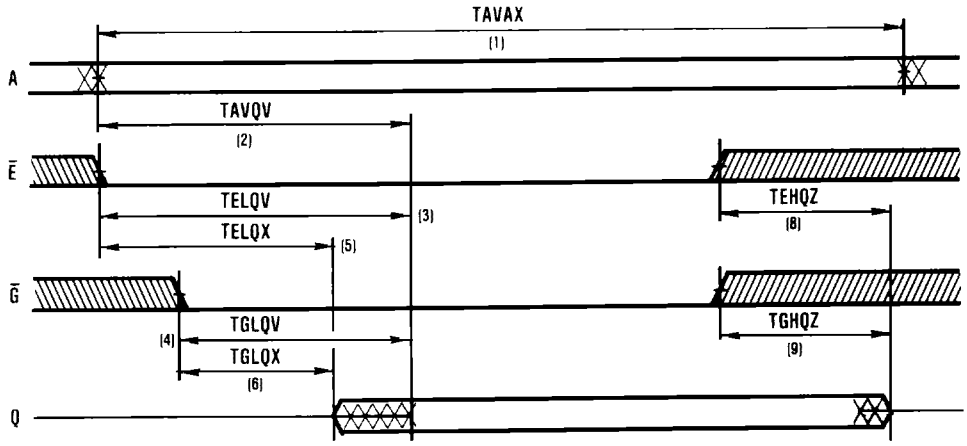
MODE	HM-8808	HM-8808A		HM-8808/8808A	
	$\overline{E}$	$\overline{E1}$	E2	$\overline{W}$	$\overline{G}$
Standby (CMOS)	VCC	X	GND	X	X
Standby (TTL)	VIH	VIH	VIL	X	X
Enabled (High Z)	VIL	VIL	VIH	VIH	VIH
Write	VIL	VIL	VIH	VIL	X
Read	VIL	VIL	VIH	VIH	VIL

HM-8808 Timing Diagrams

READ CYCLE 1 (Notes 1, 2)



READ CYCLE 2 (Note 1)

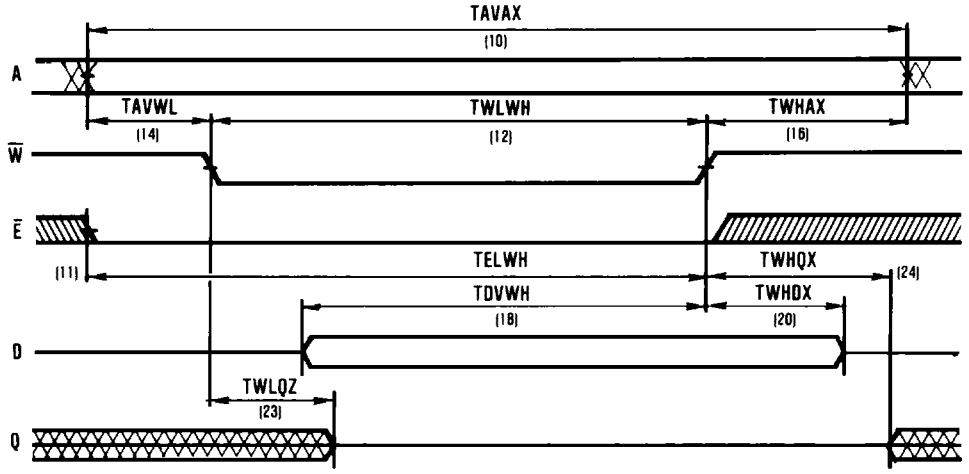


NOTES:

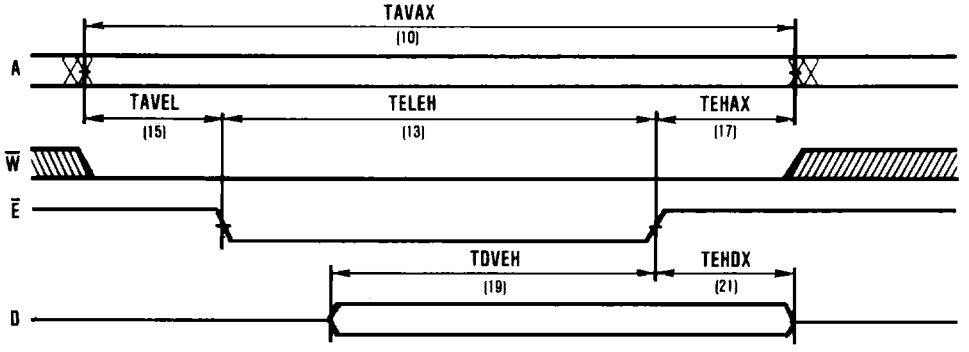
1. In a read cycle, $\overline{W}$ is held high.
2. In read cycle 1, the module is kept continuously enabled. $\overline{G}$, and $\overline{E}$ are held at VIL.

HM-8808 Timing Diagrams (Continued)

WRITE CYCLE 1 (Notes 1, 3, 4)



WRITE CYCLE 2 (Notes 2, 4)

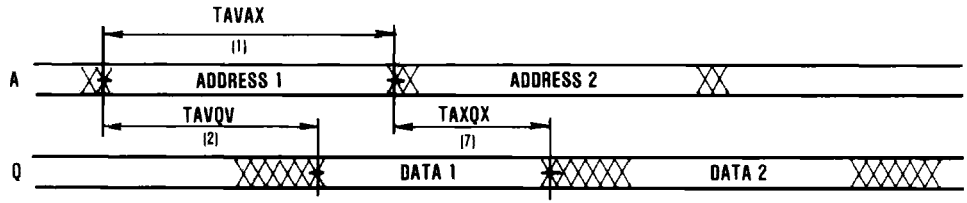


NOTES:

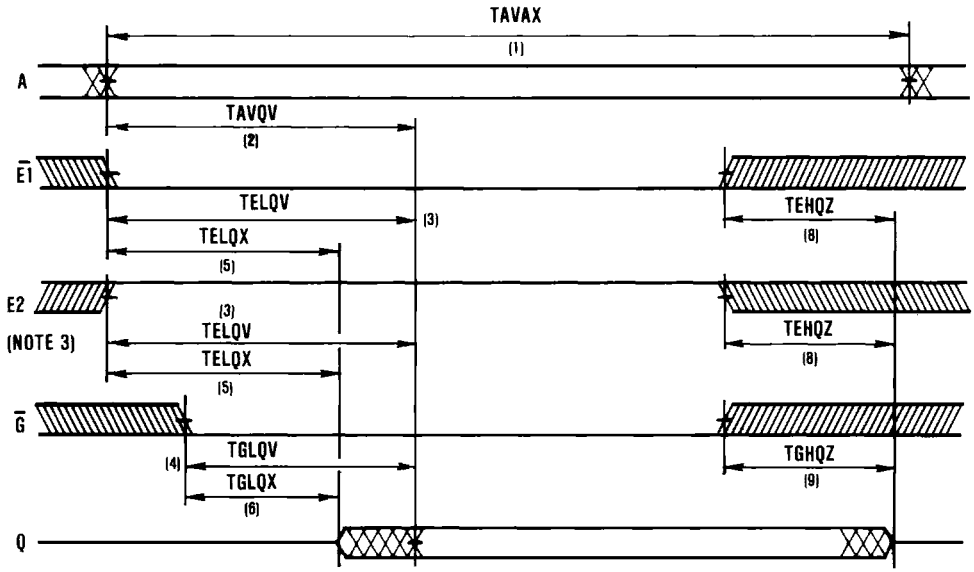
1. In Write Cycle 1, the module is first enabled and then data is strobed into the RAM with a pulse on Write Enable ($\overline{W}$). Because $\overline{W}$ becomes valid after the part is enabled, this is sometimes referred to as a "Late Write" cycle.
2. In Write Cycle 2, Address (A) and Write Enable ($\overline{W}$) are first set up, and then data is strobed into the RAM with a pulse on $\overline{E}$. Because $\overline{W}$ is valid before the module is enabled, this is sometimes referred to as an "Early Write" cycle.
3. Output Enable ($\overline{G}$) is normally held stable throughout the entire cycle. If $\overline{G}$ is held high, then the outputs (Q) remain in the high impedance state. If $\overline{G}$ is held low, then it may be necessary to lengthen the cycle to prevent bus contention. This would occur if TWLQZ and TDVWH overlapped.
4. Data Inputs (D) and Data Outputs (Q) are connected internally at the DQ pins.

HM-8808A Timing Diagrams

READ CYCLE 1 (Note 1, 2)



READ CYCLE 2 (Note 1)

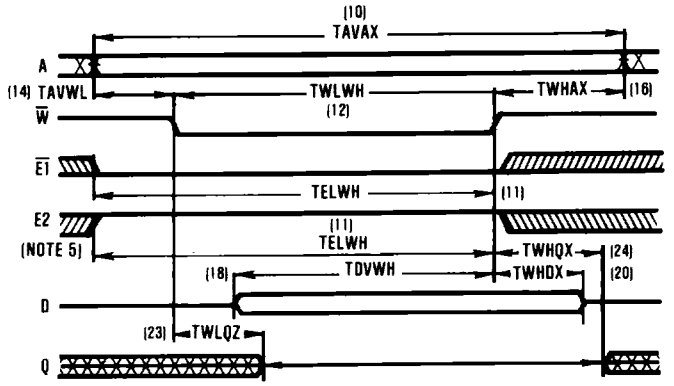


NOTES:

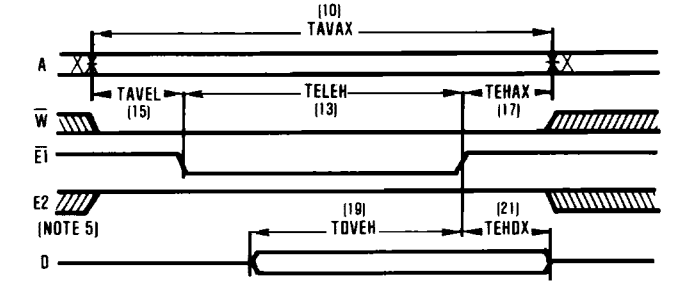
1. In a read cycle, $\overline{W}$ is held high.
2. In read cycle 2, the module is kept continuously enabled: $\overline{G}$ and $\overline{E1}$ are held at VIL. E2 is held at VIH.
3. The AC timing of E2 is the same as that of $\overline{E1}$. Only the polarity is reversed. While $\overline{E1}$ is active low, E2 is active high. Therefore AC parameters that refer to the falling edge of enable, such as TELQV, can be applied to the rising edge of E2, and parameters that refer to the rising edge of enable, such as TEHQZ, can be applied to the falling edge of E2.

HM-8808A Timing Diagrams (Continued)

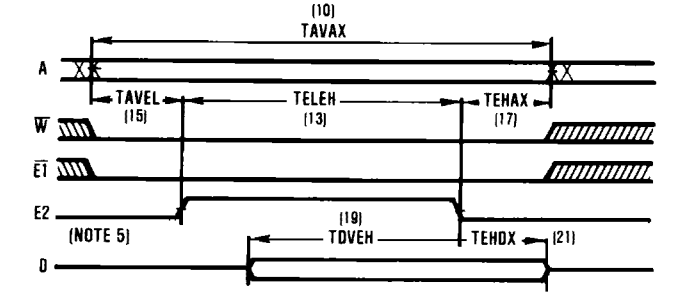
WRITE CYCLE 1: Controlled by $\overline{W}$ (Notes 1, 3, 4)



WRITE CYCLE 2: Controlled by $\overline{E1}$ (Notes 2, 4)



WRITE CYCLE 3: Controlled by E2 (Notes 2, 4)



NOTES:

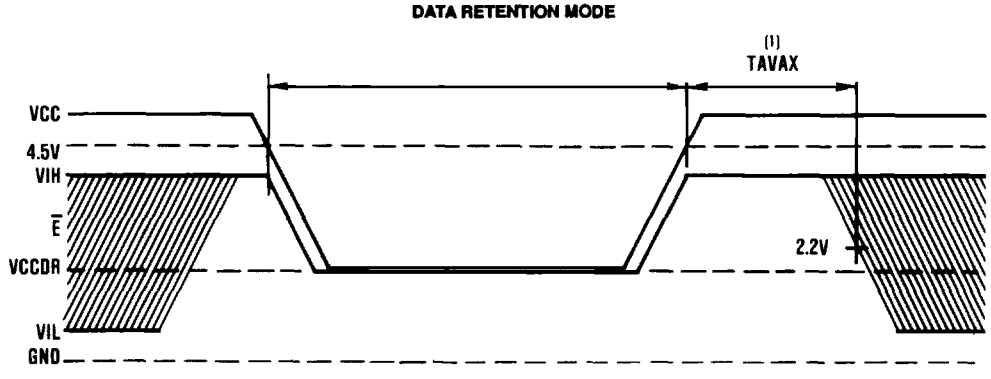
1. In Write Cycle 1, the module is first enabled and then data is strobed into the RAM with a pulse on Write Enable ($\overline{W}$). Because $\overline{W}$ becomes valid after the part is enabled, this is sometimes referred to as a "Late Write" cycle.
2. In Write Cycle 2 and 3, Address (A) and Write Enable ($\overline{W}$) are first set up, and then data is strobed into the RAM with a pulse on $\overline{E1}$ or E2. Because $\overline{W}$ is valid before the module is enabled, this is sometimes referred to as an "Early Write" cycle.
3. Output Enable ($\overline{G}$) is normally held stable throughout the entire cycle. If $\overline{G}$ is held high, then the outputs (Q) remain in the high impedance state. If $\overline{G}$ is held low, then it may be necessary to lengthen the cycle to prevent bus contention. This would occur if TWLQZ and TDVWH overlapped.
4. Data Inputs (D) and Data Outputs (Q) are connected internally at the DQ pins.
5. The AC timing of E2 is the same as that of $\overline{E1}$. Only the polarity is reversed. While $\overline{E1}$ is active low, E2 is active high. Therefore AC parameters that refer to the falling edge of enable, such as TELQV, can be applied to the rising edge of E2, and parameters that refer to the rising edge of enable, such as TEHQZ, can be applied to the falling edge of E2.

Low Voltage Data Retention

Harris CMOS RAMs are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retention:

1. The module must be kept disabled during data retention. The Chip Enable ($\overline{E}$) on the HM-8808 must be held between VCC-0.3V and VCC+0.3V. Chip Enable 2 (E2) on the HM-8808A must be held between -0.3V and GND +0.3V.
2. During power-up and power-down transitions, $\overline{E}$ (HM-8808) must be held between 90% of VCC and VCC +0.3V; E2 (HM-8808A) must be held above -0.3V and below 10% of VCC.
3. The RAM module can begin operation one TAVAX after VCC reaches the minimum operating voltage (4.5V).

HM-8808 Data Retention Timing



HM-8808A Data Retention Timing