

74FR74 • 74FR1074 Dual D-Type Flip-Flop

General Description

The 74FR74 and 74FR1074 are dual D-type flip-flops with true and complement (Q/\bar{Q}) outputs. On the 74FR74, data at the D inputs is transferred to the outputs on the rising edge of the clock input (CP_n). The 74FR1074 is the negative edge triggered version of this device. Both parts feature asynchronous clear (C_{Dn}) and set (S_{Dn}) inputs which are low level enabled.

Features

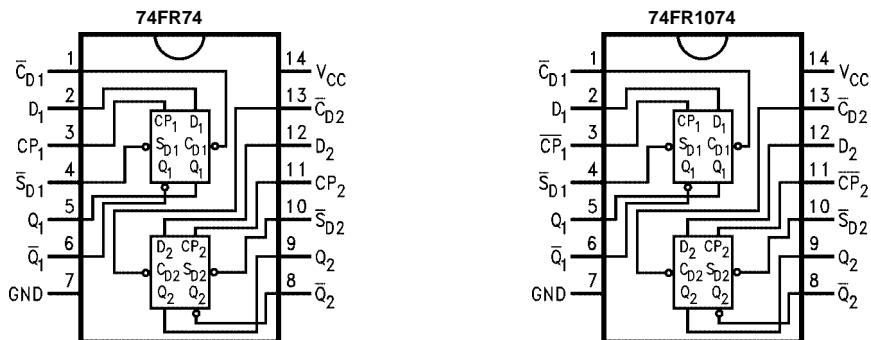
- 74FR74 is pin-for-pin compatible with the 74F74
- True 150 MHz f_{MAX} capability on 74FR74
- Outputs sink 24 mA and source 24 mA
- Guaranteed pin-to-pin skew specifications

Ordering Code:

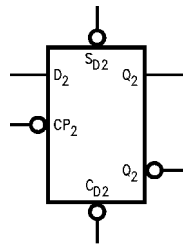
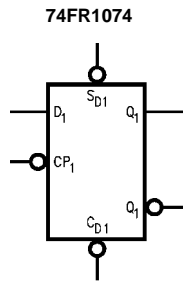
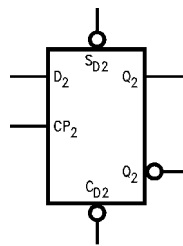
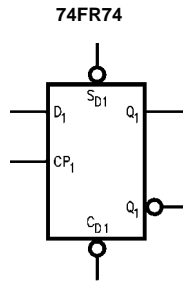
| Order Number | Package Number | Package Description |
|--------------|----------------|--|
| 74FR74SC | M14A | 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow |
| 74FR74PC | N14A | 14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide |
| 74FR1074SC | M14A | 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow |
| 74FR1074PC | N14A | 14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide |

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagrams



Logic Symbols



Pin Descriptions

| Pin Names | Description |
|------------------|---------------------------|
| D_n | Data Inputs |
| CP_n | Clock Inputs |
| S_{Dn} | Asynchronous Set Inputs |
| C_{Dn} | Asynchronous Clear Inputs |
| Q_n | True Output |
| \overline{Q}_n | Complementary Output |

Truth Tables

74FR74

| Inputs | | | | Outputs | |
|-----------------|-----------------|------|-----|---------|------------------|
| \overline{SD} | \overline{CD} | CP | D | Q | \overline{Q} |
| L | H | X | X | H | L |
| H | L | X | X | L | H |
| L | L | X | X | H | H |
| H | H | ↗ | H | H | L |
| H | H | ↘ | L | L | H |
| H | H | L | X | Q_0 | \overline{Q}_0 |

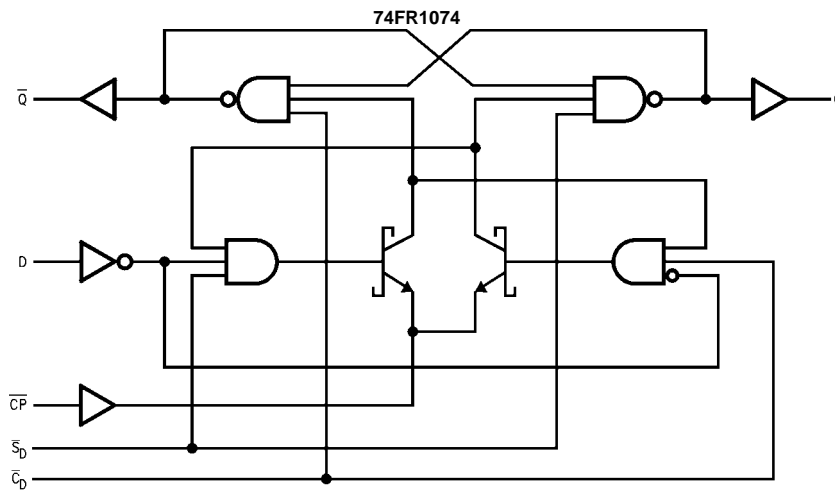
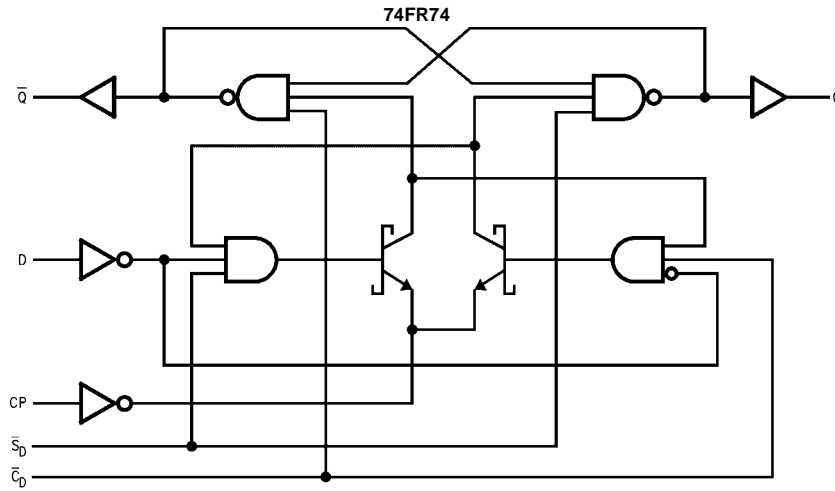
H = HIGH Voltage Level
 L = LOW Voltage Level
 Z = High Impedance
 X = Immaterial
 ↗ = Rising Edge
 ↘ = Falling Edge
 Q_0 = Previous $Q(\overline{Q})$ before LOW-to-HIGH Clock Transition

74FR1074

| Inputs | | | | Outputs | |
|-----------------|-----------------|-----------------|-----|---------|------------------|
| \overline{SD} | \overline{CD} | \overline{CP} | D | Q | \overline{Q} |
| L | H | X | X | H | L |
| H | L | X | X | L | H |
| L | L | X | X | H | H |
| H | H | ↘ | H | H | L |
| H | H | ↗ | L | L | H |
| H | H | L | X | Q_0 | \overline{Q}_0 |

H = HIGH Voltage Level
 L = LOW Voltage Level
 Z = High Impedance
 X = Immaterial
 ↘ = Falling Edge
 ↗ = Rising Edge
 Q_0 = Previous $Q(\overline{Q})$ before HIGH-to-LOW Clock Transition

Logic Diagrams



Please note that these diagrams are provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

| | |
|--|--------------------------------------|
| Storage Temperature | -65°C to +150°C |
| Ambient Temperature under Bias | -55°C to +125°C |
| Junction Temperature under Bias | -55°C to +150°C |
| V _{CC} Pin Potential to Ground Pin | -0.5V to +7.0V |
| Input Voltage (Note 2) | -0.5V to +7.0V |
| Input Current (Note 2) | -30 mA to +5.0 mA |
| Voltage Applied to Output in HIGH State (with V _{CC} = 0V) | |
| Standard Output | -0.5V to V _{CC} |
| Current Applied to Output in LOW State (Max) | twice the rated I _{OL} (mA) |
| ESD Last Passing Voltage (Min) | 2000V |

Recommended Operating Conditions

| | |
|------------------------------|----------------|
| Free Air Ambient Temperature | 0°C to +70°C |
| Supply Voltage | +4.5V to +5.5V |

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

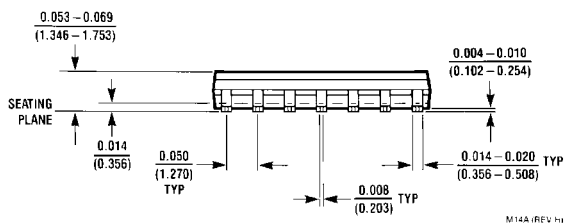
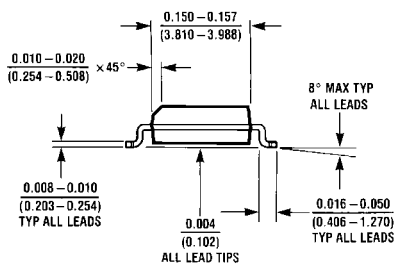
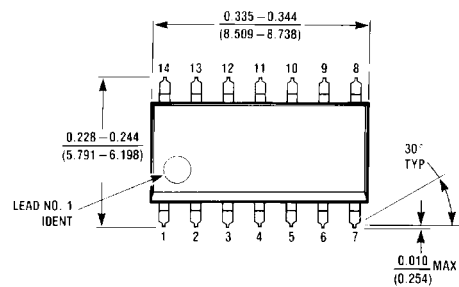
DC Electrical Characteristics

| Symbol | Parameter | Min | Typ | Max | Units | V _{CC} | Conditions |
|------------------|-----------------------------------|------|-----|------|-------|-----------------|---|
| V _{IH} | Input HIGH Voltage | 2.0 | | | V | | Recognized HIGH Signal |
| V _{IL} | Input LOW Voltage | | | 0.8 | V | | Recognized LOW Signal |
| V _{CD} | Input Clamp Diode Voltage | | | -1.2 | V | Min | I _{IN} = -18 mA |
| V _{OH} | Output HIGH Voltage | 2.5 | | | V | Min | I _{OH} = -1 mA |
| | | 2.4 | | | V | Min | I _{OH} = -3 mA |
| | | 2.0 | | | V | Min | I _{OH} = -24 mA |
| V _{OL} | Output LOW Voltage | | | 0.5 | V | Min | I _{OL} = 24 mA |
| I _{IH} | Input HIGH Current | | | 5 | μA | Max | V _{IN} = 2.7V |
| I _{BVI} | Input HIGH Current Breakdown Test | | | 7 | μA | Max | V _{IN} = 7.0V |
| I _{IL} | Input LOW Current | | | -150 | μA | Max | V _{IN} = 0.5V (D _n , CP _n) |
| | | | | -1.8 | mA | Max | V _{IN} = 0.5V (CD _n , SD _n) |
| V _{ID} | Input Leakage Test | 4.75 | | | V | 0.0 | I _{ID} = 1.9 μA, All Other Pins Grounded |
| I _{OD} | Output Circuit Leakage Test | | | 3.75 | V | 0.0 | V _{ID} = 150 mV, All Other Pins Grounded |
| I _{OS} | Output Short-Circuit Current | -100 | | -275 | mA | Max | V _{OUT} = 0.0V |
| I _{CEX} | Output HIGH Leakage Current | | | 50 | μA | Max | V _{OUT} = V _{CC} |
| I _{CC} | Power Supply Current | | | 24 | mA | Max | |

| AC Electrical Characteristics 74FR74 | | | | | | | |
|---|--|---|-----|--|--|-------|-------|
| Symbol | Parameter | T _A = +25°C V _{CC} = +5.0V C _L = 50 pF | | | T _A = 0°C to +70°C V _{CC} = +5.0V C _L = 50 pF | | Units |
| | | Min | Typ | Max | Min | Max | |
| f _{MAX} | Maximum Clock Frequency | 150 | 190 | | 150 | | MHz |
| t _{PLH} | Propagation Delay | 2.5 | 3.5 | 5.0 | 2.5 | 5.0 | ns |
| t _{PHL} | CP _n to Q _n or \overline{Q}_n | 2.5 | 4.5 | 6.0 | 2.5 | 6.0 | |
| t _{PLH} | Propagation Delay | 1.5 | 3.5 | 5.5 | 1.5 | 5.5 | ns |
| t _{PHL} | \overline{C}_{Dn} or \overline{S}_{Dn} to Q _n or \overline{Q}_n | 2.0 | 5.5 | 7.0 | 2.0 | 7.0 | |
| t _{OSSL} (Note 3) | Pin to Pin Skew for HL Transitions | | | | | 1.0 | ns |
| t _{OSLH} (Note 3) | Pin to Pin Skew for LH Transitions | | | | | 1.0 | ns |
| t _{OSt} (Note 3) | Pin to Pin Skew for HL/LH Transitions | | | | | 3.0 | ns |
| t _{OQ} (Note 3) | True/Complement Output Skew | | | | | 1.8 | ns |
| t _{ps} (Note 3) | Pin (Signal) Transition Variation | | | | | 1.8 | ns |
| <p>Note 3: Pin-to-Pin Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH-to-LOW (t_{OSSL}) or LOW-to-HIGH (t_{OSLH}) or in opposite directions both HL and LH (t_{OSt}). t_{OSt} is guaranteed by design.</p> | | | | | | | |
| AC Operating Requirements 74FR74 | | | | | | | |
| Symbol | Parameter | T _A = +25°C V _{CC} = +5.0V C _L = 50 pF | | T _A = 0°C to +70°C V _{CC} = +5.0V C _L = 50 pF | | Units | |
| | | Min | Max | Min | Max | | |
| t _S (H) | Setup Time, HIGH or LOW | 2.5 | | 2.5 | | ns | |
| t _S (L) | D _n to CP _n | 2.5 | | 2.5 | | | |
| t _H (H) | Hold Time, HIGH or LOW | 0 | | 0 | | ns | |
| t _H (L) | D _n to CP _n | 0 | | 0 | | | |
| t _W (H) | CP _n Pulse Width | 3.3 | | 3.3 | | ns | |
| t _W (L) (Note 4) | HIGH or LOW | 3.3 | | 3.3 | | | |
| t _W (L) | \overline{S}_{Dn} or \overline{C}_{Dn} Pulse Width | 4.0 | | 4.0 | | ns | |
| t _{REC} | Recovery Time \overline{S}_{Dn} or \overline{C}_{Dn} to CP _n | 2.0 | | 2.0 | | ns | |
| <p>Note 4: This specification is guaranteed by design.</p> | | | | | | | |

| AC Electrical Characteristics 74FR1074 | | | | | | | |
|---|---|---|-----|---|--|-------|-------|
| Symbol | Parameter | T _A = +25°C V _{CC} = +5.0V C _L = 50 pF | | | T _A = 0°C to +70°C V _{CC} = +5.0V C _L = 50 pF | | Units |
| | | Min | Typ | Max | Min | Max | |
| t _{MAX} | Maximum Clock Frequency | 120 | 160 | | 120 | | MHz |
| t _{PLH} | Propagation Delay CP _n to Q _n or \overline{Q}_n | 2.5 | 4.0 | 5.5 | 2.5 | 5.5 | ns |
| t _{PHL} | Propagation Delay \overline{C}_{Dn} or \overline{S}_{Dn} to Q _n or \overline{Q}_n | 3.0 | 5.0 | 6.5 | 3.0 | 6.5 | ns |
| t _{OSHL} (Note 5) | Pin to Pin Skew for HL Transitions | | | | | 1.5 | ns |
| t _{OSLH} (Note 5) | Pin to Pin Skew for LH Transitions | | | | | 1.5 | ns |
| t _{OST} (Note 5) | Pin to Pin Skew for HL/LH Transitions | | | | | 3.5 | ns |
| t _{O\overline{Q}} (Note 5) | True/Complement Output Skew | | | | | 2.0 | ns |
| t _{ps} (Note 5) | Pin (Signal) Transition Variation | | | | | 2.0 | ns |
| <p>Note 5: Pin-to-Pin Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}) or in opposite directions both HL and LH (t_{OST}). t_{OST} is guaranteed by design.</p> | | | | | | | |
| AC Operating Requirements 74FR1074 | | | | | | | |
| Symbol | Parameter | T _A = +25°C V _{CC} = +5.0V C _L = 50 pF | | T _A = 0°C = +70°C V _{CC} = +5.0V C _L = 50 pF | | Units | |
| | | Min | Max | Min | Max | | |
| t _{S(H)} | Setup Time, HIGH or LOW | 2.0 | | 2.0 | | ns | |
| t _{S(L)} | D _n to CP _n | 2.0 | | 2.0 | | | |
| t _{H(H)} | Hold Time, HIGH or LOW | 0 | | 0 | | ns | |
| t _{H(L)} | D _n to CP _n | 0 | | 0 | | | |
| t _{W(H)} | CP _n Pulse Width | 3.3 | | 3.3 | | ns | |
| t _{W(L)} (Note 6) | HIGH or LOW | 3.3 | | 3.3 | | | |
| t _{W(L)} | \overline{S}_{Dn} or \overline{C}_{Dn} Pulse Width | 4.0 | | 4.0 | | ns | |
| t _{REC} | Recovery Time \overline{S}_{Dn} or \overline{C}_{Dn} to CP _n | 2.0 | | 2.0 | | ns | |
| <p>Note 6: This specification is guaranteed by design.</p> | | | | | | | |

Physical Dimensions inches (millimeters) unless otherwise noted



**14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M14A**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



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