FAIRCHILD SEMICONDUCTOR®

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DM74AS286
9-Bit Parity Generator/Checker with Bus-Driver Parity I/O Port

Features

- PNP inputs to reduce bus loading
- Generates either odd or even parity for nine data lines
- Inputs are buffered to lower the drive requirements
- Can be used to upgrade existing systems using MSI parity circuits
- Cascadable for n-bits
- Switching specifications at 50pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- A parity I/O portable to drive bus

General Description

These universal, 9-bit parity generators/checkers utilize advanced Schottky high performance circuitry and feature odd/even outputs to facilitate operation of either odd or even parity applications. The word length capability is easily expanded by cascading.

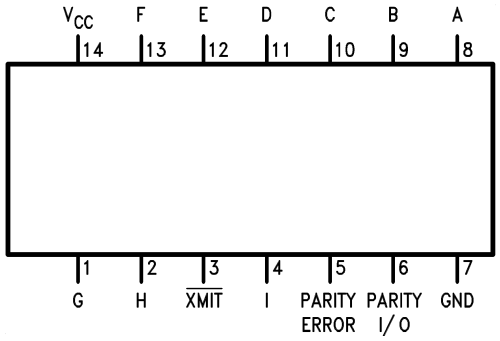
The DM74AS286 can be used to upgrade the performance of most systems utilizing the DM74AS280 parity generator/checker. Although the DM74AS286 is implemented without expander inputs, the corresponding function is provided by the availability of an input pin $\overline{XMIT}$. $\overline{XMIT}$ is a control line which makes parity error output active and parity an input port when HIGH; when LOW, parity error output is inactive and parity becomes an output port. In addition, parity I/O control circuitry contains a feature to keep the I/O port in the 3-STATE during power UP or DOWN to prevent bus glitches.

Ordering Information

Order Number	Package Number	Package Description
DM74AS286M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow

Devices also available in Tape and Reel. Specify by appending the suffix letter “X” to the ordering number.

Connection Diagram



Function Table

Number of Inputs (A thru I) that are HIGH	Parity I/O		$\overline{XMIT}$	Parity Error	Mode of Operation
	Input	Output			
0, 2, 4, 6, 8	N/A	H	L	H	Parity Generator
1, 3, 5, 7, 9	N/A	L	L	H	
0, 2, 4, 6, 8	H	N/A	H	H	Parity Checker
0, 2, 4, 6, 8	L	N/A	H	L	
1, 3, 5, 7, 9	H	N/A	H	L	Parity Checker
1, 3, 5, 7, 9	L	N/A	H	H	

L = LOW Logic Level

H = HIGH Logic Level

N/A = Not Applicable

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	7V
V_I	Input Voltage	7V
T_A	Operating Free Air Temperature Range	0°C to +70°C
T_{STG}	Storage Temperature Range	–65°C to +150°C
θ_{JA}	Typical Thermal Resistance	108.0°C/W

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter		Min.	Typ.	Max.	Units
V_{CC}	Supply Voltage		4.5	5	5.5	V
V_{IH}	HIGH Level Input Voltage		2			V
V_{IL}	LOW Level Input Voltage				0.8	V
I_{OH}	HIGH Level Output Current	Parity I/O			–15	mA
		Parity Error			–2	mA
I_{OL}	LOW Level Output Current	Parity I/O			48	mA
		Parity Error			20	mA
T_A	Operating Free-Air Temperature		0		70	°C

Electrical Characteristics

Over recommended free-air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_{IN} = –18 mA				–1.2	V
V_{OH}	HIGH Level Output Voltage	I_{OH} = Max, V_{CC} = 4.5V		2.4	3.2		V
		V_{CC} = 4.5V to 5.5V, I_{OH} = –2 mA		V_{CC} – 2			V
V_{OL}	LOW Level Output Voltage	V_{CC} = 4.5V, I_{OL} = Max			0.35	0.5	V
I_I	Input Current at Maximum Input Voltage	V_{CC} = 5.5V, V_{IH} = 7V, (V_I = 5.5V for Parity I/O)				0.1	mA
I_{IH}	HIGH Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V[1]	Others			20	µA
			Parity I/O			50	
I_{IL}	LOW Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V[1]				–0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_{OUT} = 2.25V		–30		–112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V, Transmit Mode, $\overline{XMIT}$ = LOW				43	mA
		Receive Mode, $\overline{XMIT}$ = HIGH				50	mA

Note:

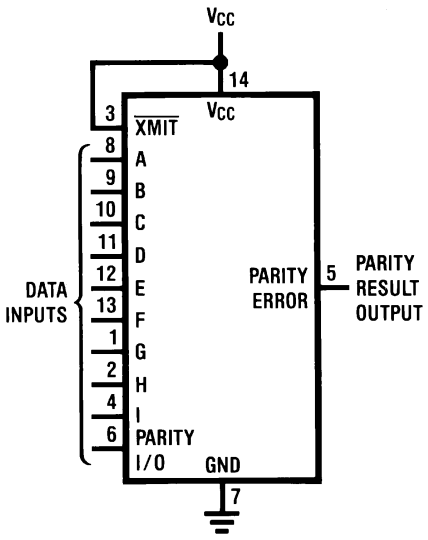
1. For I/O ports, the parameters I_{IH} and I_{IL} include the OFF-state current, I_{OZH} and I_{OZL}.

Switching Characteristics

Over recommended supply and temperature range.

Symbol	Parameter	From	To	Min.	Max.	Units
t_{PLH}	Propagation Delay Time from LOW-to-HIGH Level Output	Any Data Input	Parity I/O	3	15	ns
t_{PHL}	Propagation Delay Time from HIGH-to-LOW Level Output	Any Data Input	Parity I/O	3	14	ns
t_{PLH}	Propagation Delay Time from LOW-to-HIGH Level Output	Any Data Input	Parity Error	3	16.5	ns
t_{PHL}	Propagation Delay Time from HIGH-to-LOW Level Output	Any Data Input	Parity Error	3	16.5	ns
t_{PLH}	Propagation Delay Time from LOW-to-HIGH Level Output	Parity I/O	Parity Error	3	9	ns
t_{PHL}	Propagation Delay Time from HIGH-to-LOW Level Output	Parity I/O	Parity Error	3	9	ns
t_{PZL}	Output Enable Time to LOW Level	$\overline{XMIT}$	Parity I/O	3	16	ns
t_{PLZ}	Output Disable Time from LOW Level	$\overline{XMIT}$	Parity I/O	3	10	ns
t_{PZH}	Output Disable Time from HIGH Level	$\overline{XMIT}$	Parity I/O	3	13	ns
t_{PHZ}	Output Enable Time to HIGH Level	$\overline{XMIT}$	Parity I/O	3	11.5	ns

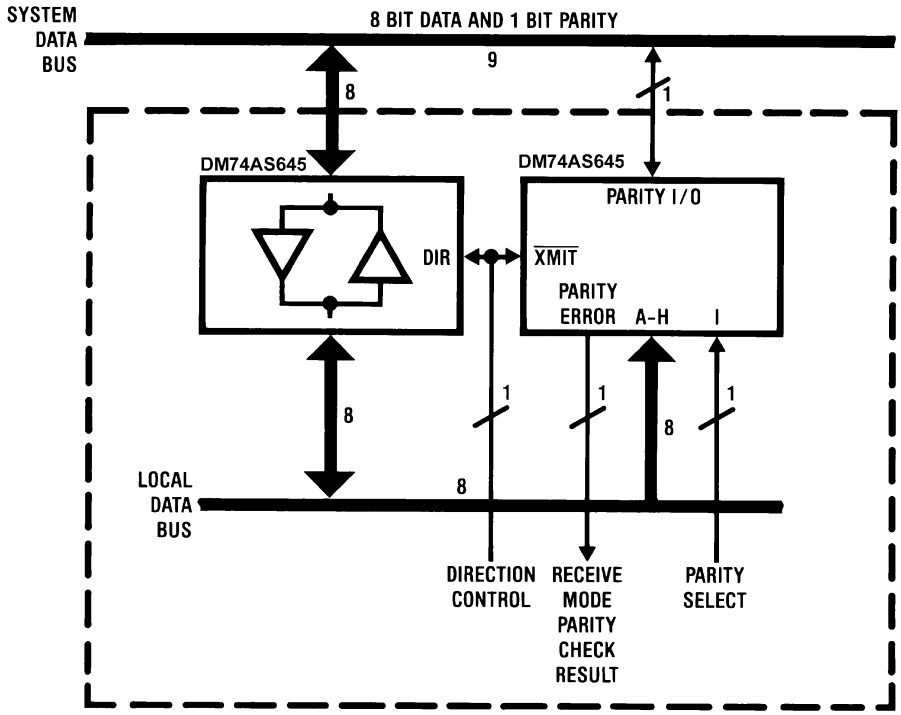
Typical Applications



Number of Inputs that are Logic "1"		Parity Result Output
0, 2, 4, 6, 8, 10	Even	L
1, 3, 5, 7, 9	Odd	H

Figure 1. Dedicated 10-Bit Parity Sensing Configuration

Typical Applications (Continued)



Direction Control (XMIT)	I/O Direction (Parity I/O)	Parity Check Result (Parity Error)	
		Level	$\sum$ Result
H	Input (Receive)	H	True
		L	False
L	Output (Transmit)	H	N/A

Parity Select (Input I)	
Level	Format
H	Even
L	Odd

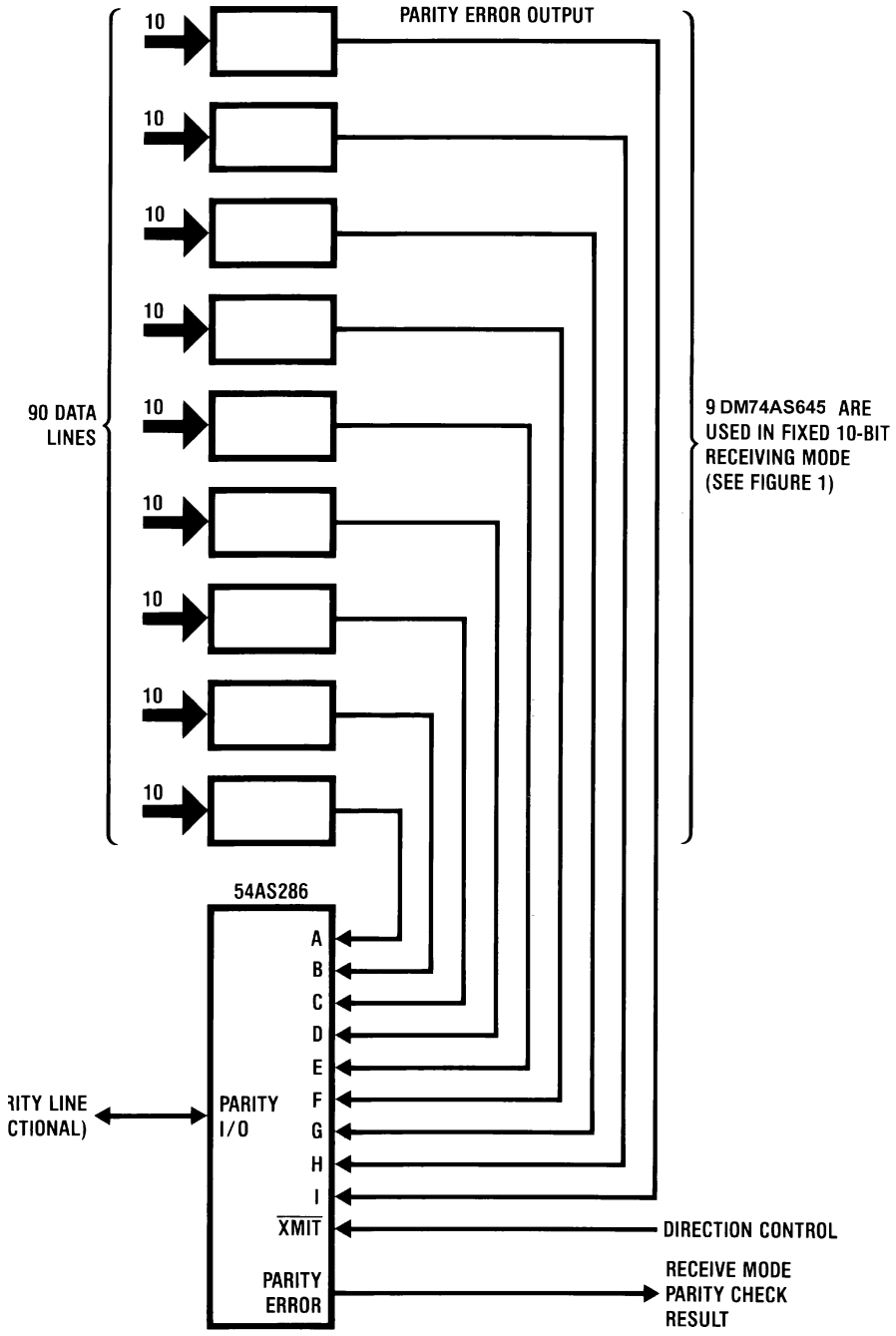
L = LOW Logic Level

H = HIGH Logic Level

N/A = Not Applicable

Figure 2. Bus I/O Parity Implementation

Typical Applications (Continued)



Note:

2. Parity format in this configuration is “odd parity”

Figure 3. 90-Bit Parity Generator/Checker Implementation Using Device Expansion Techniques

Physical Dimensions

Dimensions are in millimeters unless otherwise noted.

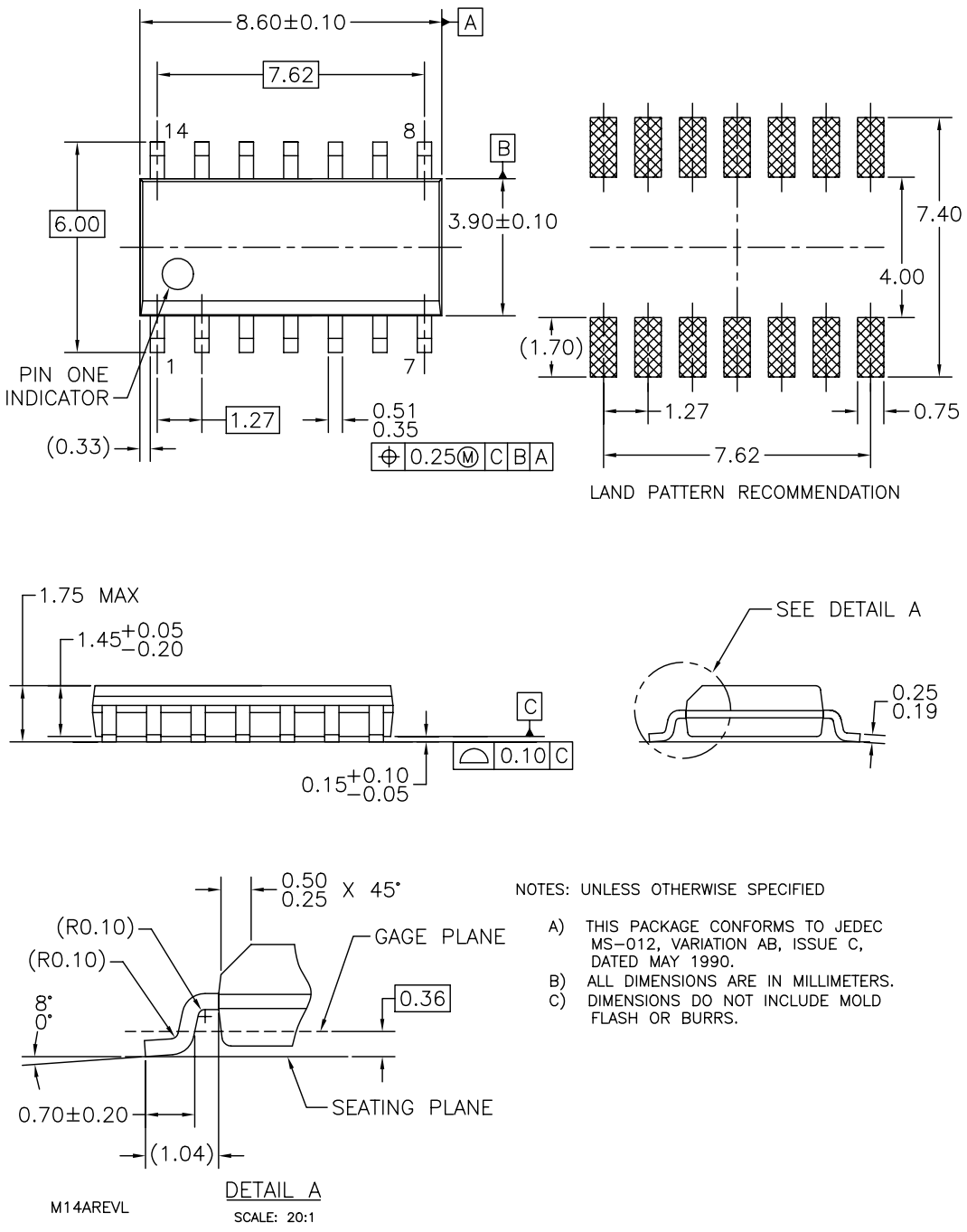


Figure 4. 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M14A

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