

NM24C08/09 – 8K-Bit Standard 2-Wire Bus Interface Serial EEPROM

General Description

The NM24C08/09 devices are 8192 bits of CMOS non-volatile electrically erasable memory. These devices conform to all specifications in the Standard IIC 2-wire protocol and are designed to minimize device pin count, and simplify PC board layout requirements.

The upper half of the memory of the 24C09 can be disabled (Write Protected) by connecting the WP pin to V_{CC} . This section of memory then becomes unalterable unless WP is switched to V_{SS} .

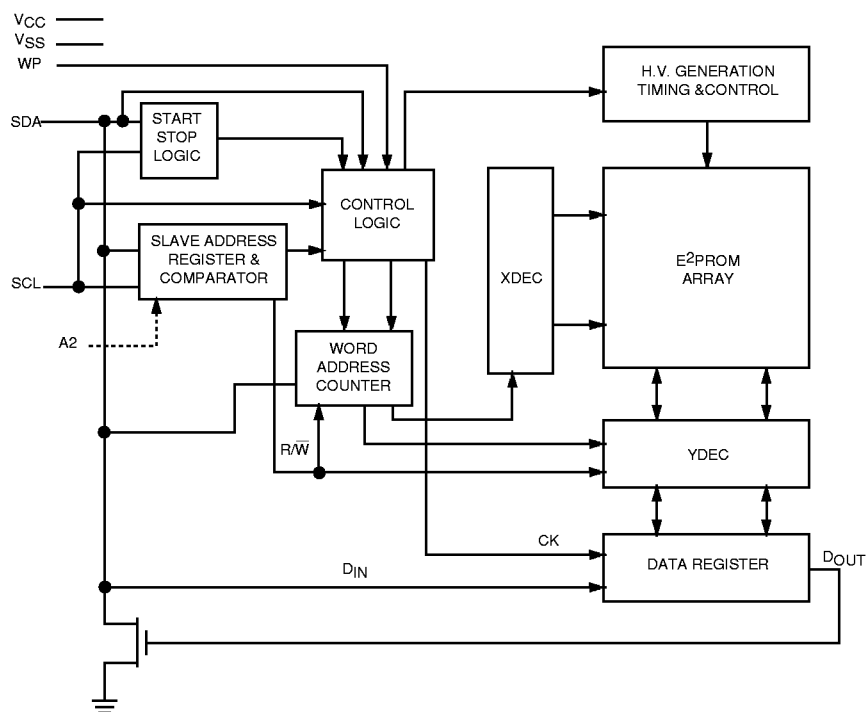
This communications protocol uses CLOCK (SCL) and DATA I/O (SDA) lines to synchronously clock data between the master (for example a microprocessor) and the slave EEPROM device(s). The Standard IIC protocol allows for a maximum of 16K of EEPROM memory which is supported by the Fairchild family in 2K, 4K, 8K, and 16K devices, allowing the user to configure the memory as the application requires with any combination of EEPROMs (not to exceed 16K). In order to implement higher EEPROM memory densities on the IIC bus, the Extended IIC protocol must be used. (Refer to the NM24C32 or NM24C65 datasheets for more information.)

Fairchild EEPROMs are designed and tested for applications requiring high endurance, high reliability and low power consumption.

Features

- Extended operating voltage 2.7V – 5.5V
- 400 KHz clock frequency (F) at 2.7V - 5.5V
- 200 μ A active current typical
10 μ A standby current typical
1 μ A standby typical (L)
0.1 μ A standby typical (LZ)
- IIC compatible interface
 - Provides bidirectional data transfer protocol
- Sixteen byte page write mode
 - Minimizes total write time per byte
- Self timed write cycle
Typical write cycle time of 6ms
- Hardwire Write Protect for upper block (NM24C09 only)
- Endurance: 1,000,000 data changes
- Data retention greater than 40 years
- Packages available: 8-pin DIP, 8-pin SO, and 8-pin TSSOP
- Available in three temperature ranges
 - Commercial: 0° to +70°C
 - Extended (E): -40° to +85°C
 - Automotive (V): -40° to +125°C

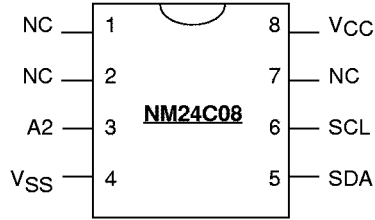
Block Diagram



DS500071-1

Connection Diagrams

Dual-In-Line Package (N), SO Package (M8), and TSSOP Package (MT8)



DS500071-2

Top View

See Package Number N08E, M08A, and MTC08

Pin Names

A2	Device Address Input
V _{SS}	Ground
SDA	Serial Data I/O
SCL	Serial Clock Input
NC	No Connection
V _{CC}	Power Supply

Dual-In-Line Package (N), SO Package (M8), and TSSOP Package (MT8)



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Top View

See Package Number N08E, M08A, and MTC08

Pin Names

NC	No Connection
A2	Device Address Input
V _{SS}	Ground
SDA	Serial Data I/O
SCL	Serial Clock input
WP	Write Protect
V _{CC}	Power Supply

Ordering Information

NM	24	C	XX	F	LZ	E	XX	Letter	Description
								Package	N 8-pin DIP M8 8-pin SOIC MT8 8-pin TSSOP
								Temp. Range	None 0 to 70°C V -40 to +125°C E -40 to +85°C
								Voltage Operating Range	Blank 4.5V to 5.5V L 2.7V to 4.5V LZ 2.7V to 4.5V and <1µA Standby Current
								SCL Clock Frequency	Blank 100KHz F 400KHz
								Density	08 8K 09 8K with Write Protect
									C CMOS Technology W Total Array Write Protect
								Interface	24 IIC
								NM	Fairchild Non-Volatile Memory

Product Specifications

Absolute Maximum Ratings

Ambient Storage Temperature	-65°C to +150°C
All Input or Output Voltages with Respect to Ground	6.5V to -0.3V
Lead Temperature (Soldering, 10 seconds)	+300°C
ESD Rating	2000V min.

Operating Conditions

Ambient Operating Temperature	0°C to +70°C
NM24C08/09	-40°C to +85°C
NM24C08E/09E	-40°C to +125°C
NM24C08V/09V	
Positive Power Supply	4.5V to 5.5V
NM24C08/09	2.7V to 5.5V
NM24C08L/09L	2.7V to 5.5V
NM24C08LZ/09LZ	2.7V to 5.5V

Standard V_{CC} (4.5V to 5.5V) DC Electrical Characteristics

Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ (Note 1)	Max	
I_{CCA}	Active Power Supply Current	$f_{SCL} = 100 \text{ kHz}$		0.2	1.0	mA
I_{SB}	Standby Current	$V_{IN} = \text{GND or } V_{CC}$		10	50	μA
I_{LI}	Input Leakage Current	$V_{IN} = \text{GND to } V_{CC}$		0.1	1	μA
I_{LO}	Output Leakage Current	$V_{OUT} = \text{GND to } V_{CC}$		0.1	1	μA
V_{IL}	Input Low Voltage		-0.3		$V_{CC} \times 0.3$	V
V_{IH}	Input High Voltage		$V_{CC} \times 0.7$		$V_{CC} + 0.5$	V
V_{OL}	Output Low Voltage	$I_{OL} = 3 \text{ mA}$			0.4	V

Low V_{CC} (2.7V to 5.5V) DC Electrical Characteristics

Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ (Note 1)	Max	
I_{CCA}	Active Power Supply Current	$f_{SCL} = 100 \text{ kHz}$		0.2	1.0	mA
I_{SB}	Standby Current for L Standby Current for LZ	$V_{IN} = \text{GND or } V_{CC}$ $V_{IN} = \text{GND or } V_{CC}$		1 0.1	10 1	μA μA
I_{LI}	Input Leakage Current	$V_{IN} = \text{GND to } V_{CC}$		0.1	1	μA
I_{LO}	Output Leakage Current	$V_{OUT} = \text{GND to } V_{CC}$		0.1	1	μA
V_{IL}	Input Low Voltage		-0.3		$V_{CC} \times 0.3$	V
V_{IH}	Input High Voltage		$V_{CC} \times 0.7$		$V_{CC} + 0.5$	V
V_{OL}	Output Low Voltage	$I_{OL} = 3 \text{ mA}$			0.4	V

Capacitance $T_A = +25^\circ\text{C}$, $f = 100/400 \text{ KHz}$, $V_{CC} = 5\text{V}$ (Note 2)

Symbol	Test	Conditions	Max	Units
$C_{I/O}$	Input/Output Capacitance (SDA)	$V_{I/O} = 0\text{V}$	8	pF
C_{IN}	Input Capacitance (A0, A1, A2, SCL)	$V_{IN} = 0\text{V}$	6	pF

Note 1: Typical values are $T_A = 25^\circ\text{C}$ and nominal supply voltage (5V).

Note 2: This parameter periodically sampled and not 100% tested.

AC Conditions of Test

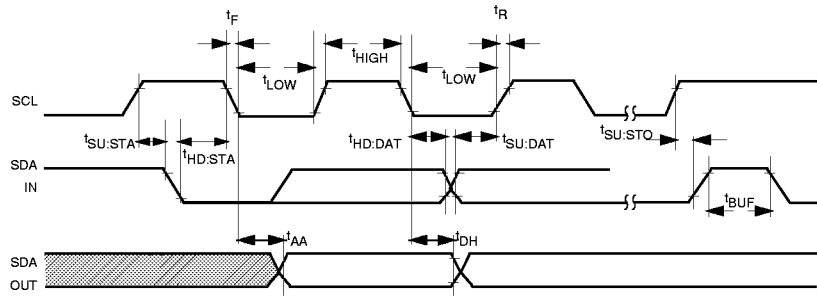
Input Pulse Levels	$V_{CC} \times 0.1$ to $V_{CC} \times 0.9$
Input Rise and Fall Times	10 ns
Input & Output Timing Levels	$V_{CC} \times 0.5$
Output Load	1 TTL Gate and $C_L = 100$ pF

Read and Write Cycle Limits (Standard and Low V_{CC} Range 2.7V - 4.5V)

Symbol	Parameter	100 KHz		400 KHz		Units
		Min	Max	Min	Max	
f_{SCL}	SCL Clock Frequency		100		400	KHz
T_I	Noise Suppression Time Constant at SCL, SDA Inputs (Minimum V_{IN} Pulse width)		100		50	ns
t_{AA}	SCL Low to SDA Data Out Valid	0.3	3.5	0.1	0.9	μ s
t_{BUF}	Time the Bus Must Be Free before a New Transmission Can Start	4.7		1.3		μ s
$t_{HD:STA}$	Start Condition Hold Time	4.0		0.6		μ s
t_{LOW}	Clock Low Period	4.7		1.5		μ s
t_{HIGH}	Clock High Period	4.0		0.6		μ s
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	4.7		0.6		μ s
$t_{HD:DAT}$	Data in Hold Time	0		0		ns
$t_{SU:DAT}$	Data in Setup Time	250		100		ns
t_R	SDA and SCL Rise Time		1		0.3	μ s
t_F	SDA and SCL Fall Time		300		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	4.7		0.6		μ s
t_{DH}	Data Out Hold Time	300		50		ns
t_{WR} (Note 3)	Write Cycle Time - NM24C08/09 - NM24C08/09L, NM24C08/09LZ		10 15		10 15	ms

Note 3: The write cycle time (t_{WR}) is the time from a valid stop condition of a write sequence to the end of the internal erase/program cycle. During the write cycle, the NM24C08/09 bus interface circuits are disabled, SDA is allowed to remain high per the bus-level pull-up resistor, and the device does not respond to its slave address.

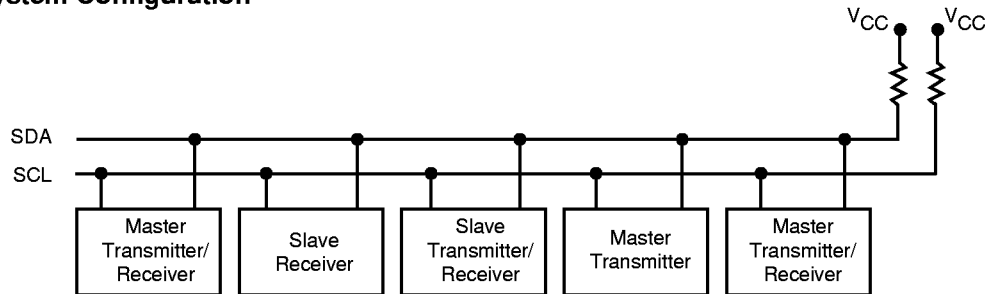
Bus Timing



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System Layout

Typical System Configuration

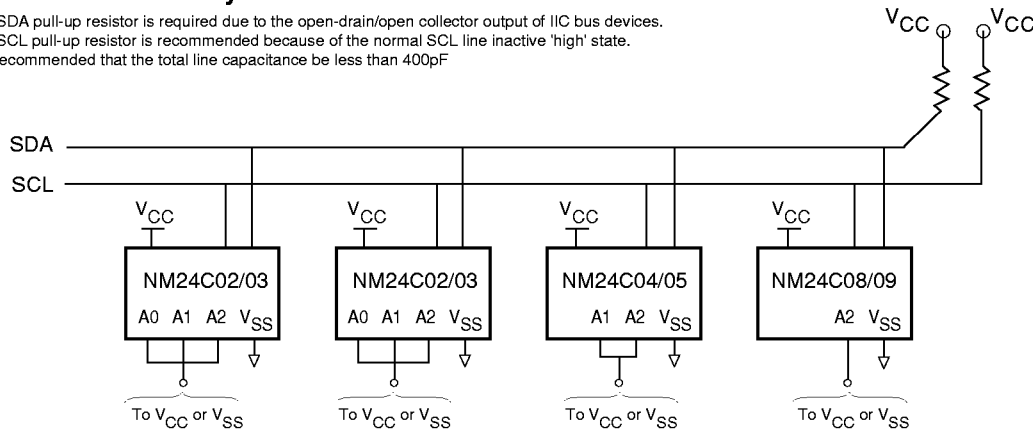


Note: Due to open drain configuration of SDA, a bus-level pull-up resistor is called for, (typical value = 4.7kΩ)

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Example of 16K of Memory on 2-Wire Bus

Note: The SDA pull-up resistor is required due to the open-drain/open collector output of IIC bus devices. The SCL pull-up resistor is recommended because of the normal SCL line inactive 'high' state. It is recommended that the total line capacitance be less than 400pF



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Device	Address Pins			Memory Size	# of Page Blocks
	A0	A1	A2		
NM24C08/09	No Connect	No Connect	ADR	8192 Bits	4

Device Operation Input (A2)

Device address pin A2 is connected to V_{CC} or V_{SS} to configure the EEPROM chip address. Table 1 shows the active pin.

Table 1.

Device	A0	A1	A2	Effects of Addresses
NM24C08/09	x	x	ADR	$2^1 = 2; 2 \times (4 \times 2k) = 16K$

Background Information (IIC Bus)

As mentioned, the IIC bus allows synchronous bidirectional communication between Transmitter/Receiver using the SCL (clock) and SDA (Data I/O) lines. All communication must be started with a valid START condition, concluded with a STOP condition and acknowledged by the Receiver with an ACKNOWLEDGE condition.

As shown below, the EEPROMs on the IIC bus may be configured in any manner required, the total memory addressed can not exceed 16K (16,384 bits). EEPROM memory address programming is controlled by 2 methods:

- Hardware configuring the A2 pin (Device Address pin) with pull-up or pull-down to V_{CC} or V_{SS} . **All unused pins must be grounded** (tied to V_{SS}).
- Software addressing the required PAGE BLOCK within the device memory array (as sent in the Slave Address string).

For devices with densities greater than 16K, a different protocol, the Extended IIC protocol, is used. Refer to NM24C32 datasheet (for example) for additional details.

Addressing an EEPROM memory location involves sending a command string with the following information: [DEVICE TYPE]–[DEVICE ADDRESS]–[PAGE BLOCK ADDRESS]–[BYTE ADDRESS]

DEFINITIONS	
BYTE	8 bits (byte) of data
PAGE	16 sequential addresses (one byte each) that may be programmed during a 'Page Write' programming cycle
PAGE BLOCK	2048 (2K) bits organized into 16 pages of addressable memory. (8 bits) x (16 bytes) x (16 pages) = 2048 bits
MASTER	Any IIC device CONTROLLING the transfer of data (such as a microprocessor)
SLAVE	Device being controlled (EEPROMs are always considered Slaves)
TRANSMITTER	Device currently SENDING data on the bus (may be either a Master or Slave).
RECEIVER	Device currently receiving data on the bus (Master or Slave)

Pin Descriptions

Serial Clock (SCL)

The SCL input is used to clock all data into and out of the device.

Serial Data (SDA)

SDA is a bidirectional pin used to transfer data into and out of the device. It is an open drain output and may be wire-ORed with any number of open drain or open collector outputs.

WP Write Protection (NM24C09 Only)

If tied to V_{CC} , PROGRAM operations onto the upper half of the memory will not be executed. READ operations are possible. If tied to V_{SS} , normal operation is enabled, READ/WRITE over the entire memory is possible.

This feature allows the user to assign the upper half of the memory as ROM which can be protected against accidental programming. When write is disabled, slave address and word address will be acknowledged but data will not be acknowledged.

Device Operation

The NM24C08/09 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is the master and the device that is controlled is the slave. The master will always initiate data transfers and provide the clock for both transmit and receive operations. Therefore, the NM24C08/09 will be considered a slave in all applications.

Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions. Refer to *Figure 2* and *Figure 3* on next page.

Start Condition

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The NM24C08/09 continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

Stop Condition

All communications are terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used by the NM24C08/09 to place the device in the standby power mode.

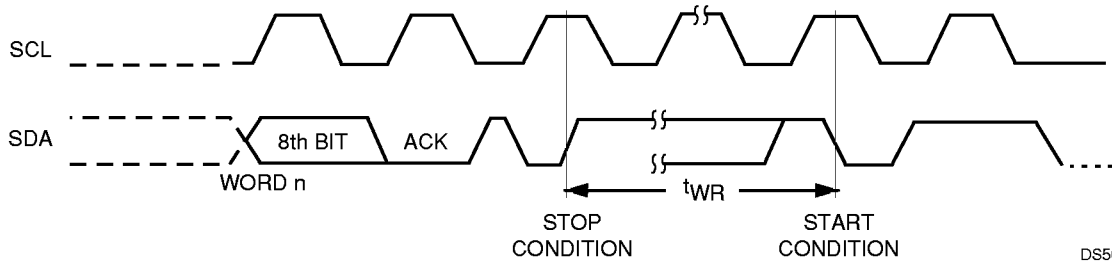
Write Cycle Timing

Acknowledge

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits.

During the ninth clock cycle the receiver will pull the SDA line to LOW to acknowledge that it received the eight bits of data. Refer to *Figure 4*.

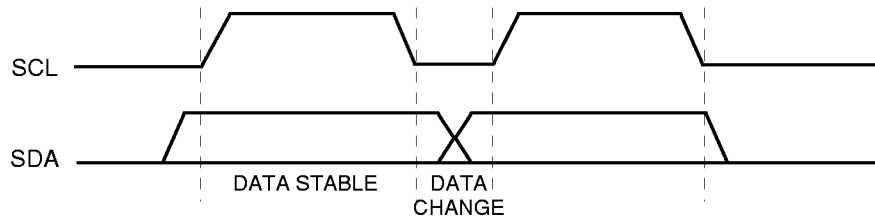
Write Cycle Timing



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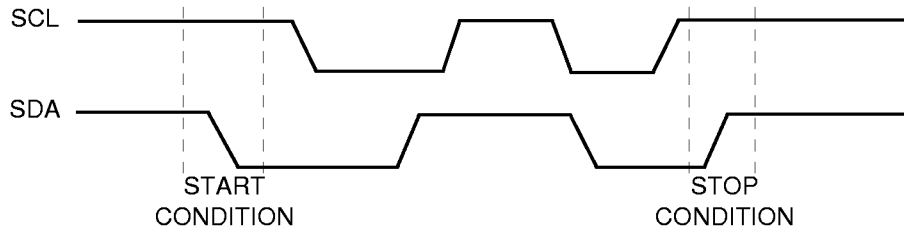
Note: The write cycle time (t_{WR}) is the time from a valid stop condition of a write sequence to the end of the internal erase/program cycle.

Data Validity (Figure 2)



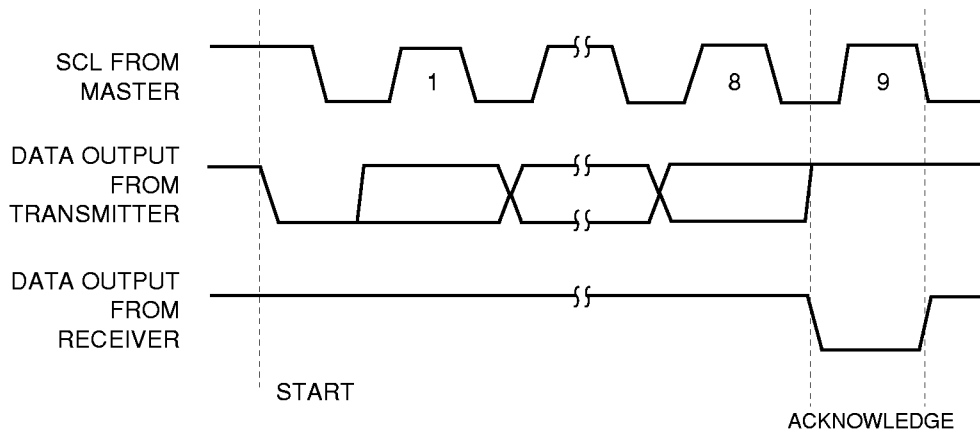
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Start and Stop Definition (Figure 3)



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Acknowledge Response from Receiver (Figure 4)



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Write Cycle Timing (Continued)

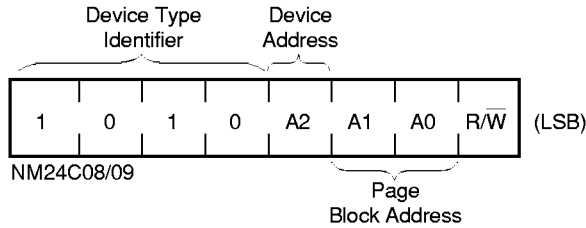
The NM24C08/09 device will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a write operation have been selected, the NM24C08/09 will respond with an acknowledge after the receipt of each subsequent eight bit byte.

In the read mode the NM24C08/09 slave will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the slave will continue to transmit data. If an acknowledge is not detected, the slave will terminate further data transmissions and await the stop condition to return to the standby power mode.

Device Addressing

Following a start condition the master must output the address of the slave it is accessing. The most significant four bits of the slave address are those of the device type identifier (see Figure 5). This is fixed as 1010 for all EEPROM devices.

Slave Addresses (Figure 5)



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Refer to the following table for Slave Addresses string details:

Device	A0	A1	A2	Page Blocks	Page Block Addresses
NM24C08/09	P	P	A	4	00 01 10 11

A: Refers to a hardware configured Device Address pin
P: Refers to an internal PAGE BLOCK memory segment.

All IIC EEPROMs use an internal protocol that defines a PAGE BLOCK size of 2K bits (for Word addresses 0000 through 1111). Therefore, address bits A0, A1, or A2 (if designated 'P') are used to access a PAGE BLOCK in conjunction with the Word address used to access any individual data byte (Word).

The last bit of the slave address defines whether a write or read condition is requested by the master. A '1' indicates that a read operation is to be executed, and a '0' initiates the write mode.

A simple review: After the NM24C08/09 recognizes the start condition, the devices interfaced to the IIC bus wait for a slave address to be transmitted over the SDA line. If the transmitted slave address matches an address of one of the devices, the designated slave pulls the line LOW with an acknowledge signal and awaits further transmissions.

Read Operations

Read operations are initiated in the same manner as write operations, with the exception that the R/W bit of the slave address is set to a one. There are three basic read operations: current address read, random read, and sequential read.

Current Address Read

Internally the NM24C08/09 contains an address counter that maintains the address of the last byte accessed, incremented by one. Therefore, if the last access (either a read or write) was to address n , the next read operation would access data from address $n + 1$. Upon receipt of the slave address with R/W set to one, the NM24C08/09 issues an acknowledge and transmits the eight bit byte. The master will not acknowledge the transfer but does generate a stop condition, and therefore the NM24C08/09 discontinues transmission. Refer to *Figure 8* for the sequence of address, acknowledge and data transfer.

Random Read

Random read operations allow the master to access any memory location in a random manner. Prior to issuing the slave address with the R/W bit set to one, the master must first perform a "dummy" write operation. The master issues the start condition, slave address and then the byte address it is to read. After the byte address acknowledge, the master immediately reissues the

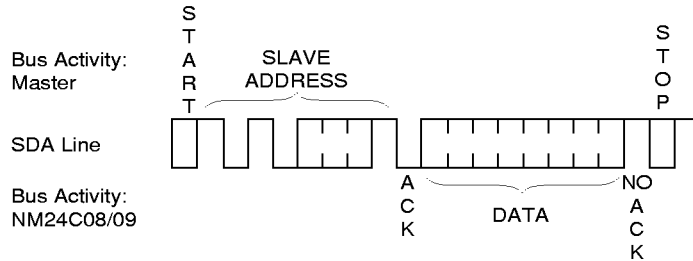
start condition and the slave address with the R/W bit set to one. This will be followed by an acknowledge from the NM24C08/09 and then by the eight bit byte. The master will not acknowledge the transfer but does generate the stop condition, and therefore the NM24C08/09 discontinues transmission. Refer to *Figure 9* for the address, acknowledge and data transfer sequence.

Sequential Read

Sequential reads can be initiated as either a current address read or random access read. The first word is transmitted in the same manner as the other read modes; however, the master now responds with an acknowledge, indicating it requires additional data. The NM24C08/09 continues to output data for each acknowledge received. The read operation is terminated by the master not responding with an acknowledge or by generating a stop condition.

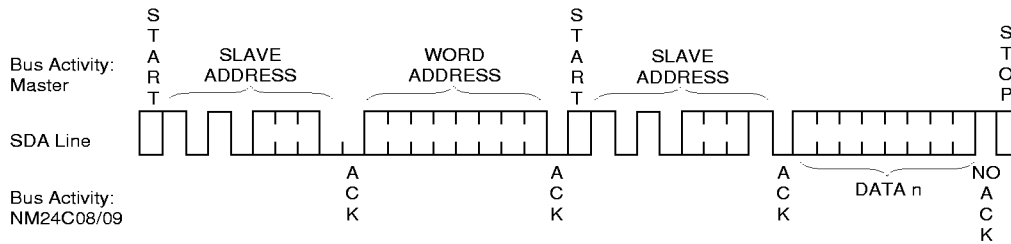
The data output is sequential, with the data from address n followed by the data from $n + 1$. The address counter for read operations increments all word address bits, allowing the entire memory contents to be serially read during one operation. After the entire memory has been read, the counter "rolls over" and the NM24C08/09 continues to output data for each acknowledge received. Refer to *Figure 10* for the address, acknowledge, and data transfer sequence.

Current Address Read (Figure 8)



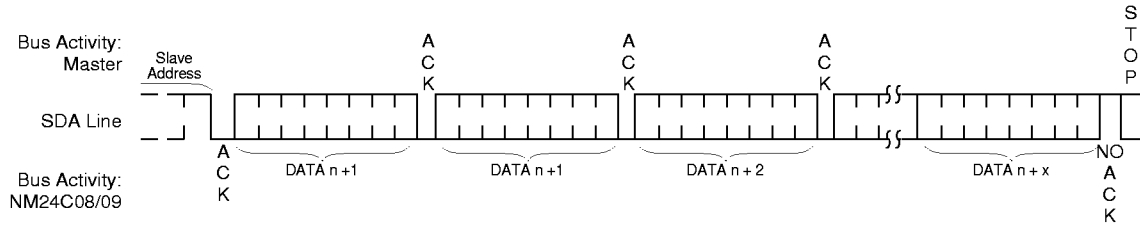
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Random Read (Figure 9)



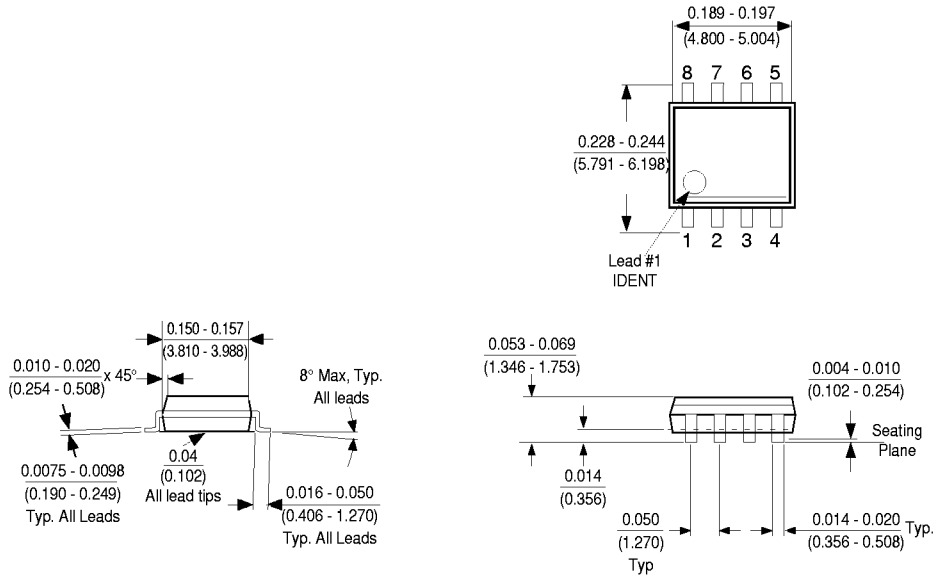
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Sequential Read (Figure 10)

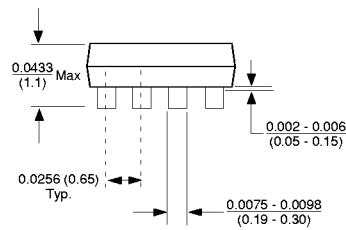
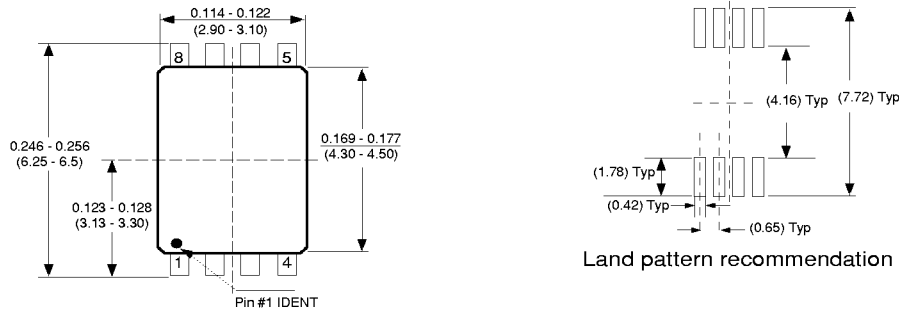


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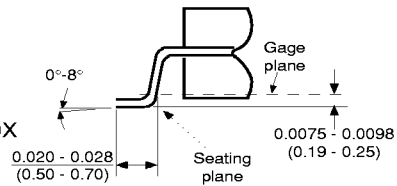
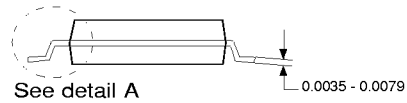
Physical Dimensions inches (millimeters) unless otherwise noted



**8-Pin Molded Small Outline Package (M8)
Package Number M08A**



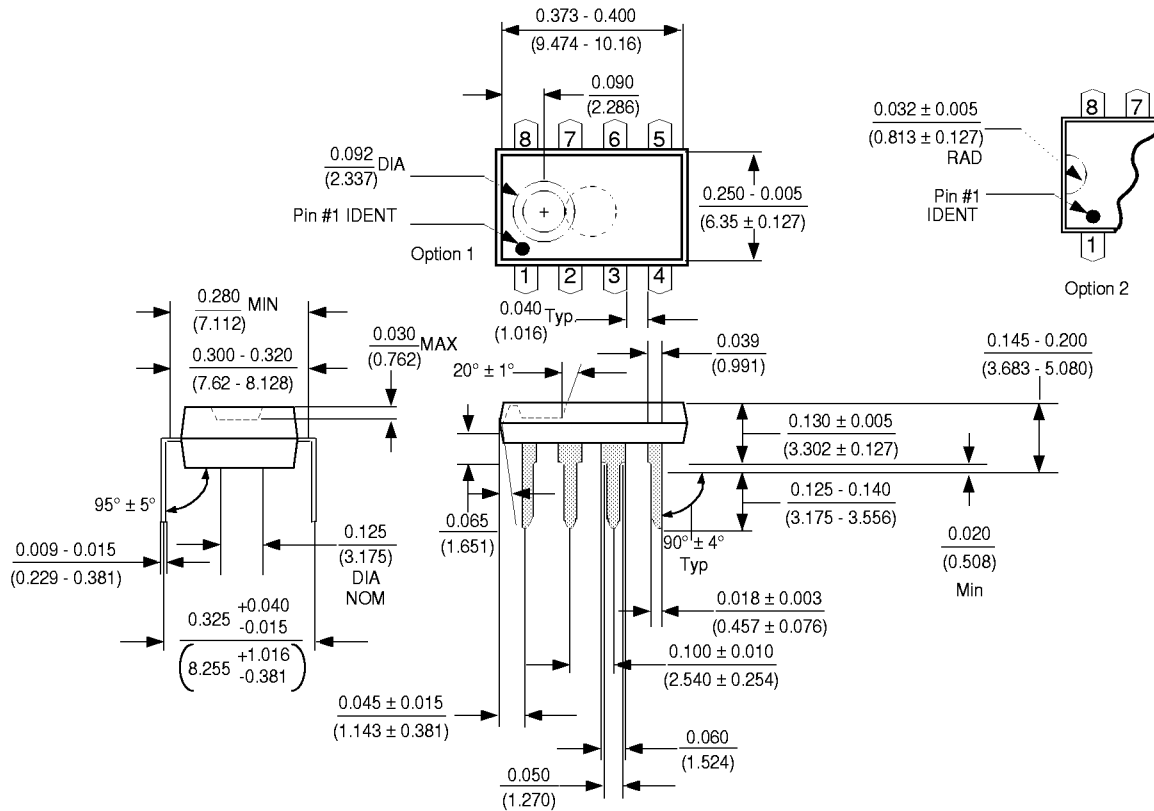
DETAIL A
Typ. Scale: 40X



Notes: Unless otherwise specified
1. Reference JEDEC registration MO153. Variation AA. Dated 7/93

Package Number MTC08

Physical Dimensions inches (millimeters) unless otherwise noted



**Molded Dual-In-Line Package (N)
Package Number N08E**

Life Support Policy

Fairchild's products are not authorized for use as critical components in life support devices or systems without the express written approval of the President of Fairchild Semiconductor Corporation. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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