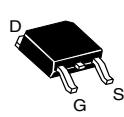
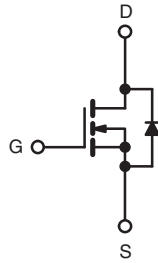
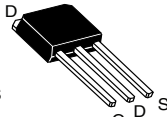


## Power MOSFET



RoHS  
COMPLIANT  
HALOGEN  
FREE  
Available

PRODUCT SUMMARY	
$V_{DS}$ (V)	100
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = 5.0$ V   0.27
$Q_g$ (Max.) (nC)	12
$Q_{gs}$ (nC)	3.0
$Q_{gd}$ (nC)	7.1
Configuration	Single

 DPAK  
(TO-252)

 IPAK  
(TO-251)


N-Channel MOSFET

### FEATURES

- Dynamic  $dV/dt$  Rating
- Repetitive Avalanche Rated
- Surface Mount (IRLR120, SiHLR120)
- Straight Lead (IRLU120, SiHLU120)
- Available in Tape and Reel
- Logic-Level Gate Drive
- $R_{DS(on)}$  Specified at  $V_{GS} = 4$  V and 5 V
- Material categorization: For definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)

### DESCRIPTION

Third generation power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The DPAK is designed for surface mounting using vapor phase, infrared, or wave soldering techniques. The straight lead version (IRLU, SiHLU series) is for through-hole mounting applications. Power dissipation levels up to 1.5 W are possible in typical surface mount applications.

ORDERING INFORMATION					
Package	DPAK (TO-252)	DPAK (TO-252)	DPAK (TO-252)	DPAK (TO-252)	IPAK (TO-251)
Lead (Pb)-free and Halogen-free	SiHLR120-GE3	SiHLR120TRL-GE3	SiHLR120TR-GE3	SiHLR120TRR-GE3	SiHLU120-GE3
Lead (Pb)-free	IRLR120PbF	IRLR120TRLPbF <sup>a</sup>	IRLR120TRPbF <sup>a</sup>	IRLR120TRRPbF <sup>a</sup>	IRLU120PbF
	SiHLR120-E3	SiHLR120TL-E3 <sup>a</sup>	SiHLR120T-E3 <sup>a</sup>	SiHLR120TR-E3 <sup>a</sup>	SiHLU120-E3

#### Note

- a. See device orientation.

ABSOLUTE MAXIMUM RATINGS ( $T_C = 25$ °C, unless otherwise noted)				
PARAMETER	SYMBOL		LIMIT	UNIT
Drain-Source Voltage	$V_{DS}$		100	V
Gate-Source Voltage	$V_{GS}$		$\pm 10$	
Continuous Drain Current	$V_{GS}$ at 5.0 V	$T_C = 25$ °C	7.7	A
		$T_C = 100$ °C	4.9	
Pulsed Drain Current <sup>a</sup>	$I_{DM}$		31	W/°C
Linear Derating Factor			0.33	
Linear Derating Factor (PCB Mount) <sup>e</sup>			0.020	
Single Pulse Avalanche Energy <sup>b</sup>	$E_{AS}$		210	mJ
Repetitive Avalanche Current <sup>a</sup>	$I_{AR}$		7.7	A
Repetitive Avalanche Energy <sup>a</sup>	$E_{AR}$		4.2	mJ
Maximum Power Dissipation	$T_C = 25$ °C		42	W
	$T_A = 25$ °C		2.5	
Peak Diode Recovery $dV/dt$ <sup>c</sup>	$dV/dt$		5.5	V/ns
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$		- 55 to + 150	°C
Soldering Recommendations (Peak Temperature) <sup>d</sup>	for 10 s		260	

#### Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = 25$  V, starting  $T_J = 25$  °C,  $L = 5.3$  mH,  $R_g = 25$   $\Omega$ ,  $I_{AS} = 7.7$  A (see fig. 12).
- $I_{SD} \leq 9.2$  A,  $dI/dt \leq 110$  A/ $\mu$ s,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 150$  °C.
- 1.6 mm from case.
- When mounted on 1" square PCB (FR-4 or G-10 material).



THERMAL RESISTANCE RATINGS						
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	
Maximum Junction-to-Ambient	$R_{thJA}$	-	-	110	°C/W	
Maximum Junction-to-Ambient (PCB Mount) <sup>a</sup>	$R_{thJA}$	-	-	50		
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	-	3.0		

**Note**

a. When mounted on 1" square PCB (FR-4 or G-10 material).

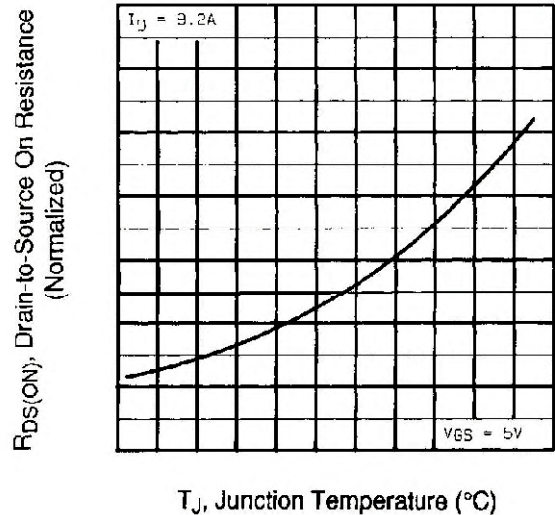
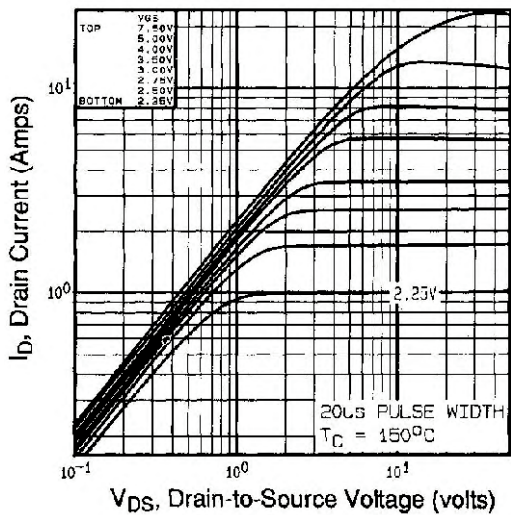
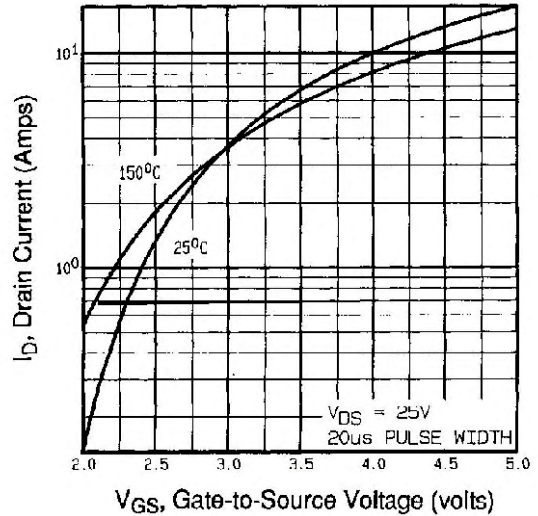
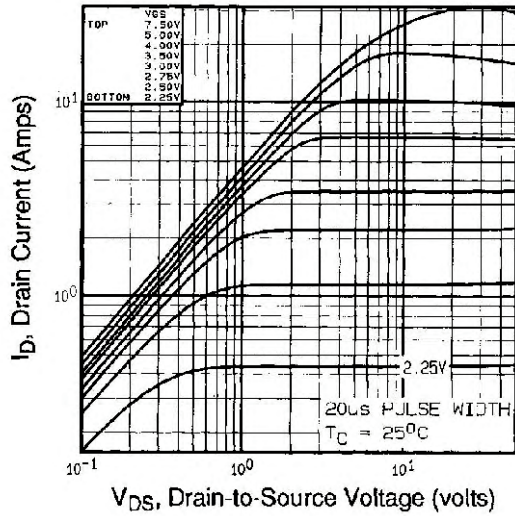
SPECIFICATIONS ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
<b>Static</b>							
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$		100	-	-	V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}, I_D = 1\text{ mA}$		-	0.13	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$		1.0	-	2.0	V
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 10\text{ V}$		-	-	$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}$		-	-	25	$\mu\text{A}$
		$V_{DS} = 80\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$		-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 5.0\text{ V}$	$I_D = 4.6\text{ A}^b$	-	-	0.27	$\Omega$
		$V_{GS} = 4.0\text{ V}$	$I_D = 3.9\text{ A}^b$	-	-	0.38	
Forward Transconductance	$g_{fs}$	$V_{DS} = 50\text{ V}, I_D = 4.6\text{ A}^b$		4.4	-	-	S
<b>Dynamic</b>							
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1.0\text{ MHz}, \text{ see fig. 5}$		-	490	-	pF
Output Capacitance	$C_{oss}$			-	150	-	
Reverse Transfer Capacitance	$C_{riss}$			-	30	-	
Total Gate Charge	$Q_g$	$V_{GS} = 5.0\text{ V}$	$I_D = 9.2\text{ A}, V_{DS} = 80\text{ V}, \text{ see fig. 6 and 13}^b$	-	-	12	nC
Gate-Source Charge	$Q_{gs}$			-	-	3.0	
Gate-Drain Charge	$Q_{gd}$			-	-	7.1	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 50\text{ V}, I_D = 9.2\text{ A}, R_g = 9.0\text{ }\Omega, R_D = 5.2\text{ }\Omega, \text{ see fig. 10}^b$		-	9.8	-	ns
Rise Time	$t_r$			-	64	-	
Turn-Off Delay Time	$t_{d(off)}$			-	21	-	
Fall Time	$t_f$			-	27	-	
Internal Drain Inductance	$L_D$	Between lead, 6 mm (0.25") from package and center of die contact <sup>c</sup>		-	4.5	-	nH
Internal Source Inductance	$L_S$			-	7.5	-	
<b>Drain-Source Body Diode Characteristics</b>							
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode		-	-	7.7	A
Pulsed Diode Forward Current <sup>a</sup>	$I_{SM}$			-	-	31	
Body Diode Voltage	$V_{SD}$	$T_J = 25\text{ }^\circ\text{C}, I_S = 7.7\text{ A}, V_{GS} = 0\text{ V}^b$		-	-	2.5	V
Body Diode Reverse Recovery Time	$t_{rr}$	$T_J = 25\text{ }^\circ\text{C}, I_F = 9.2\text{ A}, di/dt = 100\text{ A}/\mu\text{s}^b$		-	110	140	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$			-	0.80	1.0	$\mu\text{C}$
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$ )					

**Notes**

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$ .



## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



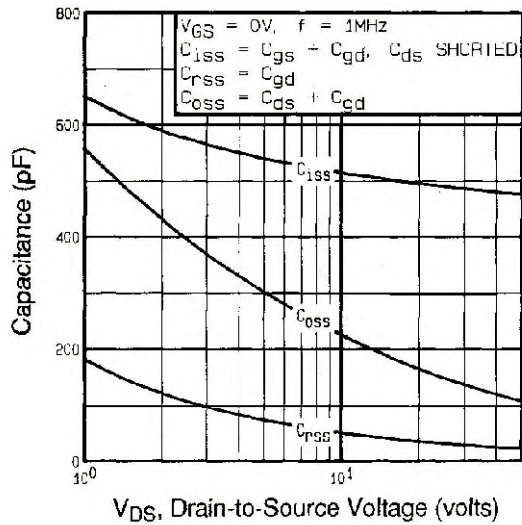


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

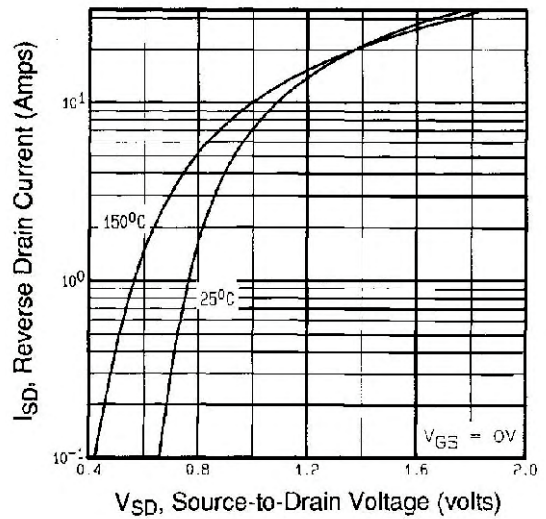


Fig. 7 - Typical Source-Drain Diode Forward Voltage

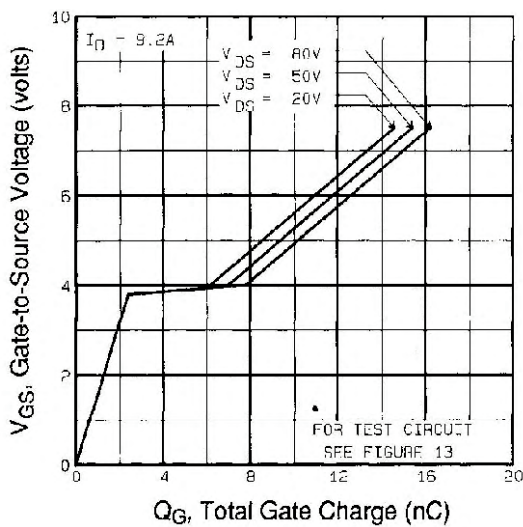


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

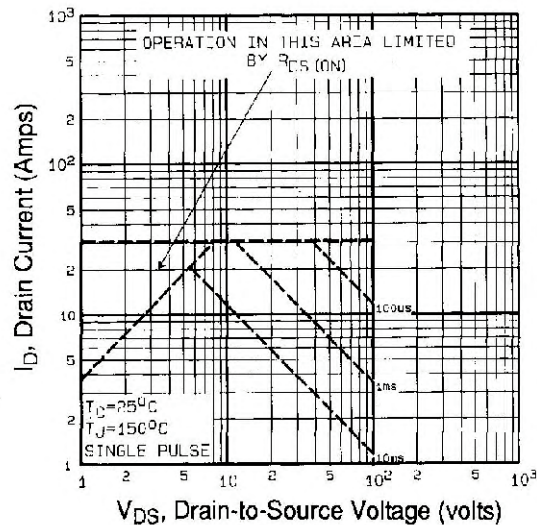


Fig. 8 - Maximum Safe Operating Area

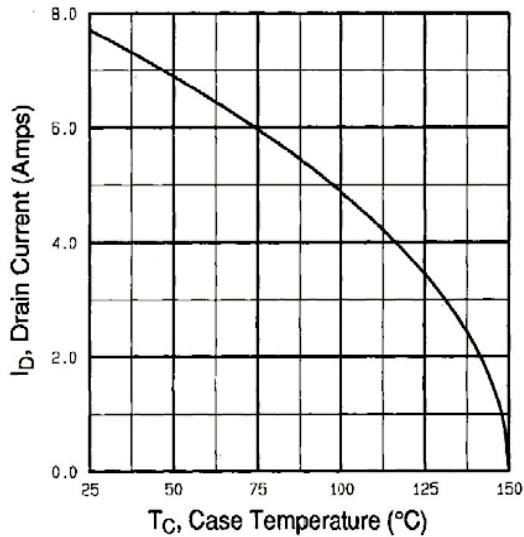


Fig. 9 - Maximum Drain Current vs. Case Temperature

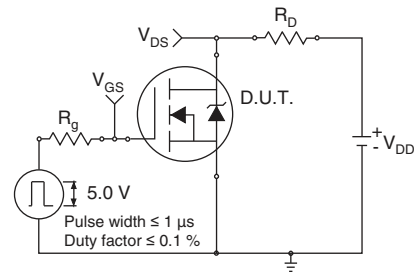


Fig. 10a - Switching Time Test Circuit

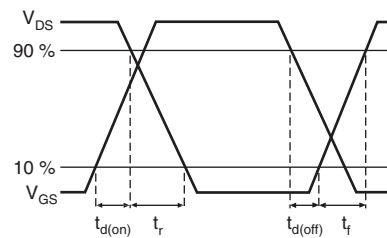


Fig. 10b - Switching Time Waveforms

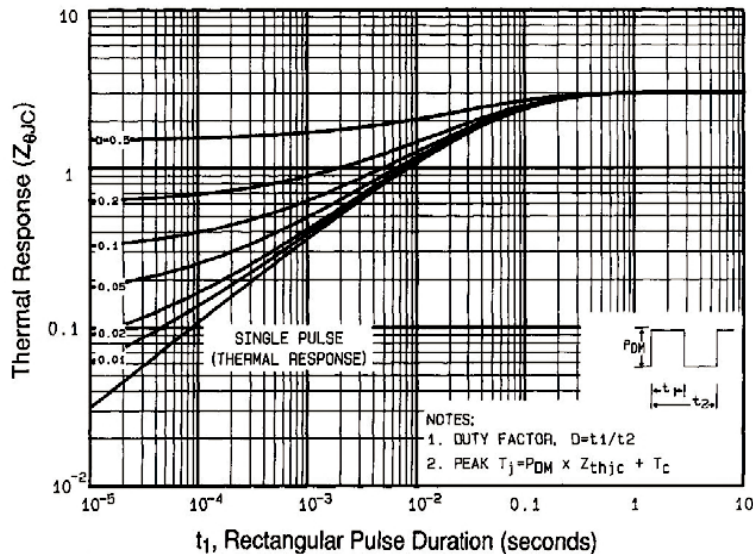


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case



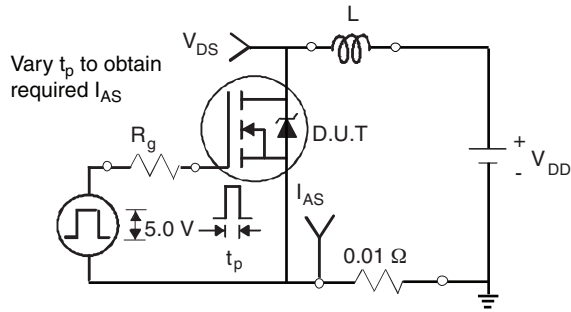


Fig. 12a - Unclamped Inductive Test Circuit

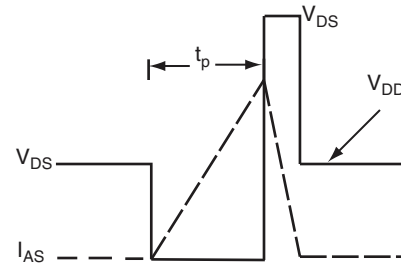


Fig. 12b - Unclamped Inductive Waveforms

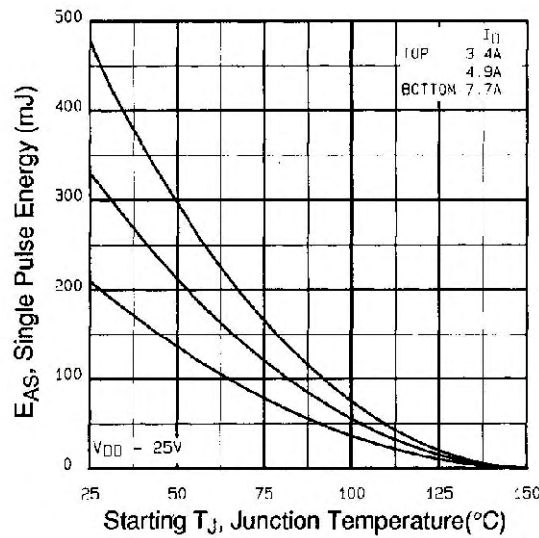


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

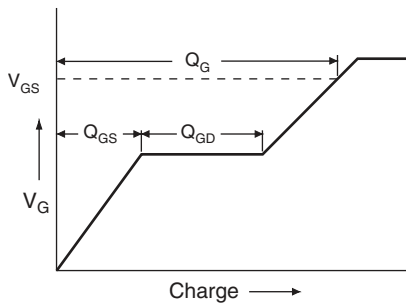


Fig. 13a - Basic Gate Charge Waveform

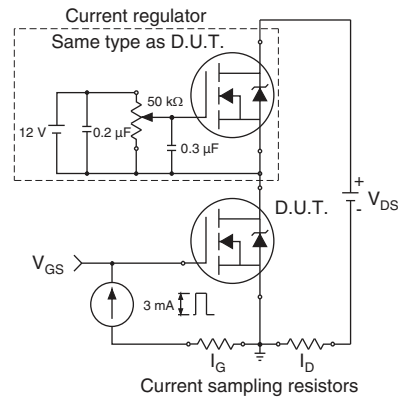
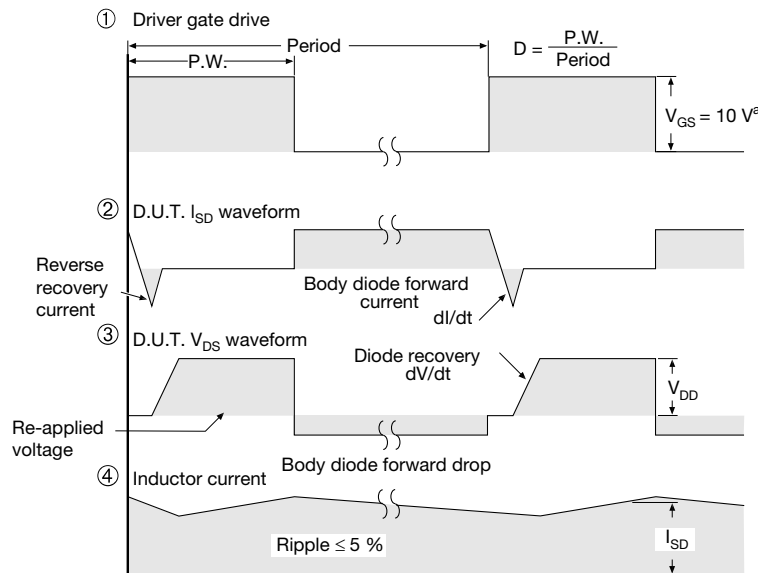
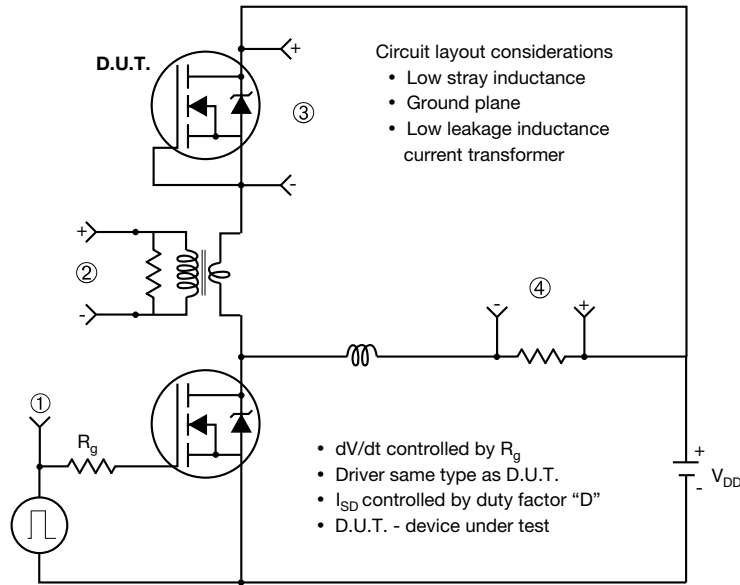


Fig. 13b - Gate Charge Test Circuit

### Peak Diode Recovery dV/dt Test Circuit



**Note**

a.  $V_{GS} = 5 V$  for logic level devices

**Fig. 14 - For N-Channel**

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see [www.vishay.com/ppg?91324](http://www.vishay.com/ppg?91324).



### TO-252AA Case Outline

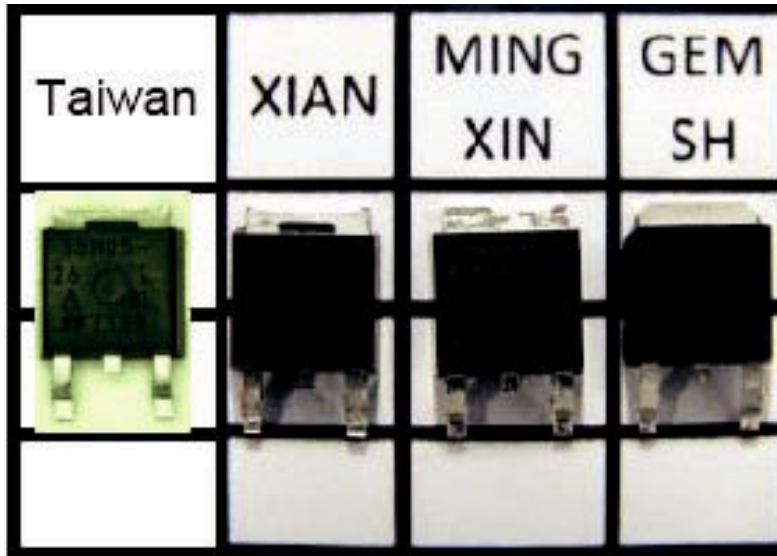


DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.18	2.38	0.086	0.094
A1	-	0.127	-	0.005
b	0.64	0.88	0.025	0.035
b2	0.76	1.14	0.030	0.045
b3	4.95	5.46	0.195	0.215
C	0.46	0.61	0.018	0.024
C2	0.46	0.89	0.018	0.035
D	5.97	6.22	0.235	0.245
D1	4.10	-	0.161	-
E	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
H	9.40	10.41	0.370	0.410
e	2.28 BSC		0.090 BSC	
e1	4.56 BSC		0.180 BSC	
L	1.40	1.78	0.055	0.070
L3	0.89	1.27	0.035	0.050
L4	-	1.02	-	0.040
L5	1.01	1.52	0.040	0.060

ECN: T13-0359-Rev. O, 03-Jun-13  
DWG: 5347

**Notes**

- Dimension L3 is for reference only.
- Xi'an, Mingxin, and GEM SH actual photo.





### TO-251AA (HIGH VOLTAGE)



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.18	2.39	0.086	0.094
A1	0.89	1.14	0.035	0.045
b	0.64	0.89	0.025	0.035
b1	0.65	0.79	0.026	0.031
b2	0.76	1.14	0.030	0.045
b3	0.76	1.04	0.030	0.041
b4	4.95	5.46	0.195	0.215
c	0.46	0.61	0.018	0.024
c1	0.41	0.56	0.016	0.022
c2	0.46	0.86	0.018	0.034
D	5.97	6.22	0.235	0.245

DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
D1	5.21	-	0.205	-
E	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
e	2.29 BSC		2.29 BSC	
L	8.89	9.65	0.350	0.380
L1	1.91	2.29	0.075	0.090
L2	0.89	1.27	0.035	0.050
L3	1.14	1.52	0.045	0.060
θ1	0'	15'	0'	15'
θ2	25'	35'	25'	35'

ECN: S-82111-Rev. A, 15-Sep-08  
 DWG: 5968

#### Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimension are shown in inches and millimeters.
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.13 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body.
4. Thermal pad contour optional with dimensions b4, L2, E1 and D1.
5. Lead dimension uncontrolled in L3.
6. Dimension b1, b3 and c1 apply to base metal only.
7. Outline conforms to JEDEC outline TO-251AA.

## RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads  
Dimensions in Inches/(mm)

[Return to Index](#)



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