National Semiconductor

CLC446
400MHz, 50mW Current-Feedback Op Amp

General Description

The National CLC446 is a very high-speed unity-gain-stable current-feedback op amp that is designed to deliver the highest levels of performance from a mere 50mW quiescent power. It provides a very wide 400MHz bandwidth, a 2000V/μs slew rate and 900ps rise/fall times. The CLC446 achieves its superior speed-vs-power using an advanced complementary bipolar IC process and National's current-feedback architecture.

The CLC446 is designed to drive video loads with very low differential gain and phase errors (0.02%, 0.03°). Combined with its very low power (50mW), the CLC446 makes an excellent choice for NTSC/PAL video switchers and routers. With its very quick edge rates (900ps) and high slew rate (2000V/μs), the CLC446 also makes an excellent choice for high-speed, high-resolution component RGB video systems.

The CLC446 makes an excellent low-power high-resolution A/D converter driver with its very fast 9ns settling time (to 0.1%) and low harmonic distortion.

The combination of high performance and low power make the CLC446 useful in many high-speed general purpose applications. Its current-feedback architecture maintains consistent performance over a wide gain range and signal levels. DC gain and bandwidth can be set independently. Also, either maximally flat AC response or linear phase response can be emphasized.

Features

- 400MHz bandwidth (A_v = +2)
- 5mA supply current
- 0.02%, 0.03° differential gain, phase
- 2000V/μs slew rate
- 9ns settling to 0.1%
- 0.05dB gain flatness to 100MHz
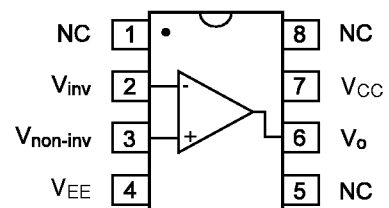- -65/-78dBc HD2/HD3

Applications

- High resolution video
- A/D driver
- Medical imaging
- Video switchers & routers
- RF/IF amplifier
- Communications
- Instrumentation

**Non-Inverting
Frequency Response (A_v = +2)**
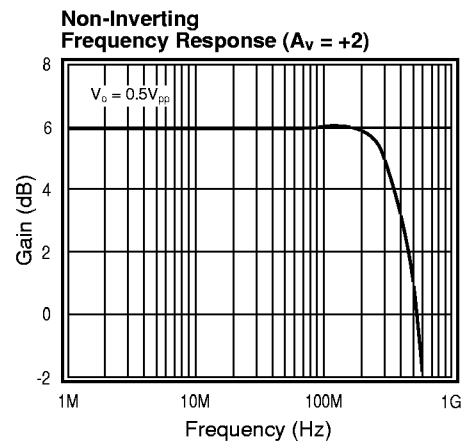
Typical Application
Elliptic-Function Low Pass Filter
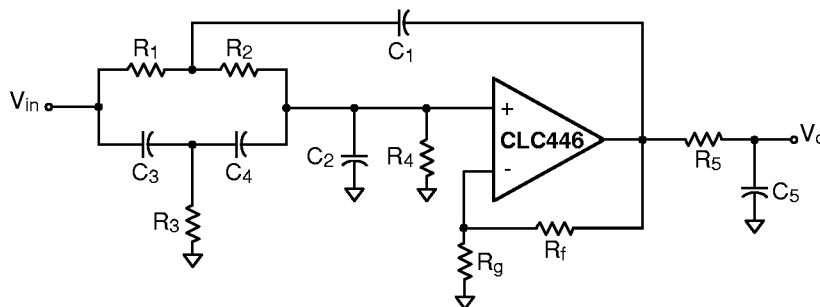
Pinout
DIP & SOIC

Electrical Characteristics (A_V = +2, R_f = 249Ω; V_{CC} = ± 5V, R_L = 100Ω; unless specified)

PARAMETERS	CONDITIONS	TYP	MIN/MAX RATINGS			UNITS	NOTES
Ambient Temperature	CLC446AJ	+25°C	+25°C	0 to 70°C	-40 to 85°C		
FREQUENCY DOMAIN RESPONSE							
-3dB bandwidth	$V_o < 0.2V_{pp}$	400	340	300	300	MHz	
	$V_o < 2.0V_{pp}$	280	210	190	190	MHz	
gain flatness $V_o < 2.0V_{pp}$	<100MHz	±0.05	±0.2	±0.2	±0.2	dB	
linear phase dev. $V_o < 2.0V_{pp}$	<100MHz	0.2	0.5	0.8	0.8	deg	
differential gain	NTSC, R_L=150Ω	0.02	0.04	0.04	0.04	%	
differential phase	NTSC, R_L=150Ω	0.03	0.05	0.05	0.05	deg	
TIME DOMAIN RESPONSE							
rise and fall time	2V step	0.9	1.4	1.5	1.6	ns	
settling time to 0.1%	2V step	9	13	15	15	ns	
overshoot	2V step	6	15	18	18	%	
slew rate	2V step, ±0.5V crossing	2000	1400	1300	1200	V/μs	
DISTORTION AND NOISE RESPONSE							
2nd harmonic distortion	$2V_{pp}$, 5MHz	-65	-59	-58	-58	dBc	
	$2V_{pp}$, 20MHz	-55	-48	-48	-48	dBc	
	$2V_{pp}$, 50MHz	-54	-43	-42	-42	dBc	
3rd harmonic distortion	$2V_{pp}$, 5MHz	-78	-70	-68	-68	dBc	
	$2V_{pp}$, 20MHz	-70	-62	-60	-60	dBc	
	$2V_{pp}$, 50MHz	-50	-45	-42	-42	dBc	
equivalent input noise							
voltage (e_{ni})	>1MHz	3.8	4.8	5.0	5.1	nV/√Hz	
non-inverting current (i_{bn})	>1MHz	2.0	2.6	2.8	3.3	pA/√Hz	
inverting current (i_{bi})	>1MHz	16	19	20	21	pA/√Hz	
STATIC DC PERFORMANCE							
input offset voltage		2	7	10	11	mV	A
average drift		17	–	25	35	μV/°C	
input bias current	non-inverting	3	12	25	25	μA	A
average drift		30	–	90	130	nA/°C	
input bias current	inverting	10	22	30	35	μA	A
average drift		26	–	75	85	nA/°C	
power supply rejection ratio	DC	52	45	43	43	dB	
common-mode rejection ratio	DC	48	44	42	42	dB	
supply current	$R_L = \infty$	4.8	5.8	6.2	6.2	mA	A
MISCELLANEOUS PERFORMANCE							
input resistance	non-inverting	1.5	1.0	0.85	0.70	MΩ	
input capacitance	non-inverting	1	2	2	2	pF	
input range	common-mode	±2.8	±2.6	±2.4	±2.3	V	
output voltage range	$R_L = 100\Omega$	±3.1	±2.8	±2.8	±2.6	V	
	$R_L = \infty$	±3.2	±3.0	±2.9	±2.8	V	
output current		48	48	48	48	mA	
output resistance, closed loop	DC	0.04	0.1	0.1	0.1	Ω	

Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

Absolute Maximum Ratings

supply voltage	±6V
output current	±48mA
common-mode input voltage	±Vcc
maximum junction temperature	+175°C
storage temperature range	-65°C to +150°C
lead temperature (soldering 10 sec)	+300°C
ESD rating (human body model)	1000V

Notes

A) J-level: spec is 100% tested at +25°C.

Ordering Information

Model	Temperature Range	Description
CLC446AJP	-40°C to +85°C	8-pin PDIP
CLC446AJE	-40°C to +85°C	8-pin SOIC
CLC446ALC	-40°C to +85°C	dice
CLC446A8B	-55°C to +125°C	8-pin CerDIP, MIL-STD-883
CLC446AMC	-55°C to +125°C	dice, MIL-STD-883

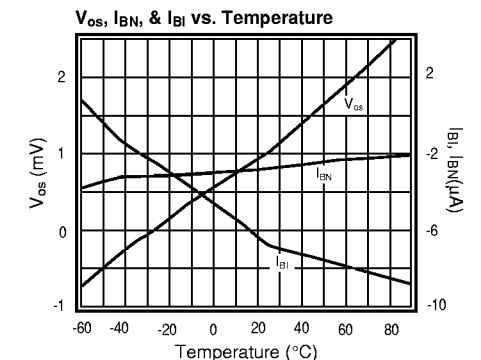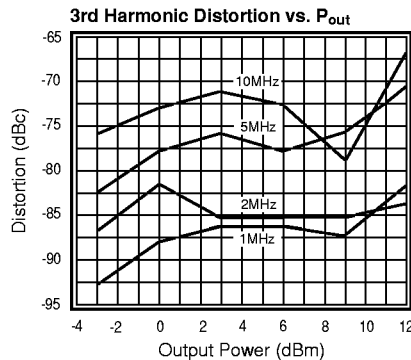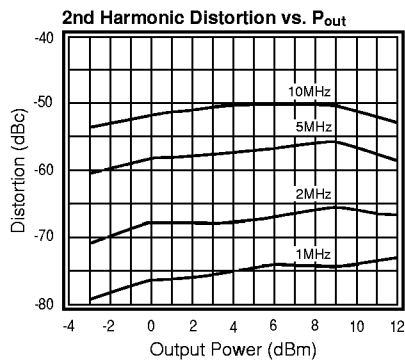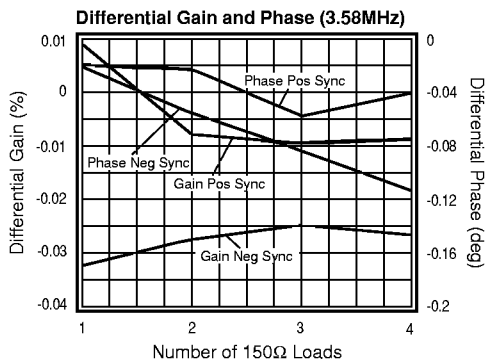Contact the factory for other packages and DESC SMD number.

Package Thermal Resistance

Package	θ_{JC}	θ_{JA}
Plastic (AJP)	70°C/W	125°C/W
Surface Mount (AJE)	60°C/W	140°C/W
Ceramic (A8B)	40°C/W	130°C/W

Reliability Information

Transistor Count	36
MTBF (based on limited test data)	39Mhr

Non-Inverting Frequency Response

$V_o = 0.5V_{pp}$
$A_v = 1V/V$, $R_f = 453\Omega$
$A_v = 2V/V$, $R_f = 249\Omega$
$A_v = 10V/V$, $R_f = 200\Omega$
$A_v = 5V/V$, $R_f = 200\Omega$

Normalized Magnitude (1dB/div)
Phase (deg)
Frequency (Hz)

Inverting Frequency Response

$V_o = 0.5V_{pp}$
$A_v = -1V/V$, $R_f = 249\Omega$
$A_v = -2V/V$, $R_f = 249\Omega$
$A_v = -5V/V$, $R_f = 200\Omega$
$A_v = -10V/V$, $R_f = 200\Omega$

Normalized Magnitude (1dB/div)
Phase (deg)
Frequency (Hz)

Frequency Response vs. R_L

$V_o = 0.5V_{pp}$
$R_L = 1k\Omega$
$R_L = 100\Omega$
$R_L = 500\Omega$

Normalized Magnitude (1dB/div)
Phase (deg)
Frequency (Hz)

Frequency Response vs. V_o

$0.1V_{pp}$
$1V_{pp}$
$4V_{pp}$
$2V_{pp}$

Normalized Magnitude (1dB/div)
Frequency (Hz)

Frequency Response vs. C_L

$C_L = 10pF$, $R_s = 46.4\Omega$
$C_L = 22pF$, $R_s = 33.2\Omega$
$C_L = 47pF$, $R_s = 21\Omega$
$C_L = 100pF$, $R_s = 13.3\Omega$

Normalized Magnitude (1dB/div)
Frequency (Hz)

Recommended R_s vs. C_L

$R_s (\Omega)$
$C_L (pF)$

Small Signal Pulse Response

$A_v = +2V/V$
$A_v = -2V/V$

Output Voltage (0.5V/div)
Time (2ns/div)

Large Signal Pulse Response

$A_v = +2V/V$
$A_v = -2V/V$

Output Voltage (1V/div)
Time (2ns/div)

Equivalent Input Noise

i_{bi}
e_{ni}
i_{bn}

Voltage Noise (nV/√Hz)
Current Noise (pA/√Hz)
Frequency (Hz)

2nd Harmonic Distortion

$V_o = 2V_{pp}$
2nd $R_L = 100\Omega$
2nd $R_L = 1k\Omega$

Distortion (dBc)
Frequency (Hz)

3rd Harmonic Distortion

$V_o = 2V_{pp}$
3rd $R_L = 100\Omega$
3rd $R_L = 1k\Omega$

Distortion (dBc)
Frequency (Hz)

Differential Gain and Phase (3.58MHz)

Phase Pos Sync
Phase Neg Sync
Gain Pos Sync
Gain Neg Sync

Differential Gain (%)
Differential Phase (deg)
Number of 150Ω Loads

2nd Harmonic Distortion vs. P_{out}

10MHz
5MHz
2MHz
1MHz

Distortion (dBc)
Output Power (dBm)

3rd Harmonic Distortion vs. P_{out}

10MHz
5MHz
2MHz
1MHz

Distortion (dBc)
Output Power (dBm)

V_{os}, I_{BN}, & I_{BI} vs. Temperature

V_{os}
I_{BN}
I_{BI}

V_{os} (mV)
I_{BI}, I_{BN} (μA)
Temperature (°C)

Short Term Settling Time

V_o (% Output Step)

V_o = 2V step

0.2
0.1
0
-0.1
-0.2

1n   10n   100n   1μ   10μ

Time (sec)

Long Term Settling Time

V_o (% Output Step)

V_o = 2V step

0.2
0.1
0
-0.1
-0.2

1μ   10μ   100μ   1m   10m   100m   1

Time (s)

CLC446 Operation

The CLC446 has a current-feedback architecture built in an advanced complementary bipolar process. The key features of current-feedback are:

■ AC bandwidth is independent of voltage gain
■ Unity-gain stability
■ Frequency response may be adjusted with R_f
■ High slew rate
■ Low variation in performance for a wide range of gains, signal levels and loads
■ Fast settling

Current-feedback operation can be explained with a simple model. The voltage gain for the circuits in Figures 1 and 2 is approximately:

$$\frac{V_o}{V_{in}} = \frac{A_v}{1 + \dfrac{R_f}{Z(j\omega)}}$$

where

■ A_v is the DC voltage gain
■ R_f is the feedback resistor
■ $Z(j\omega)$ is the CLC446's open-loop transimpedance gain
■ $\dfrac{Z(j\omega)}{R_f}$ is the loop-gain

The denominator of the equation above is approximately 1 at low frequencies. Near the -3dB corner frequency, the interaction between R_f and $Z(j\omega)$ dominates the circuit performance. Increasing R_f does the following:

■ Decreases loop-gain
■ Decreases bandwidth
■ Lowers pulse response overshoot
■ Reduces gain peaking
■ Affects frequency response phase linearity

CLC446 Design Information

The following topics will supply you with:

■ Design parameters, formulas and techniques
■ Interfaces
■ Application circuits
■ Layout techniques
■ SPICE model information

DC Gain (non-inverting)
The non-inverting DC voltage gain for the configuration

shown in Figure 1 is $A_v = 1 + \dfrac{R_f}{R_g}$.

The normalized gain plots in the *Typical Performance Characteristics* section show different feedback resistors (R_f) for different gains. These values of R_f are recommended for obtaining the highest bandwidth with minimal peaking. The resistor R_t provides DC bias for the non-inverting input.

For $A_v < 5$, use linear interpolation on the nearest A_v values to calculate the recommended value of R_f. For $A_v \geq 5$, the minimum recommended R_f is 200Ω.

Select R_g to set the DC gain: $R_g = \dfrac{R_f}{A_v - 1}$.

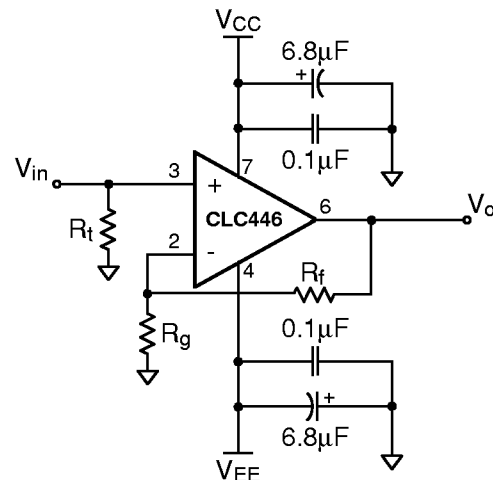DC gain accuracy is usually limited by the tolerance of R_f and R_g.

Figure 1: Non-Inverting Gain

DC Gain (unity gain buffer)
The recommended R_f for unity gain buffers is 453Ω. R_g is left open. Parasitic capacitance at the inverting node may require a slight increase of R_f to maintain a flat frequency response.

DC Gain (inverting)
The inverting DC voltage gain for the configuration shown in Figure 2 is $A_V = -\dfrac{R_f}{R_g}$.
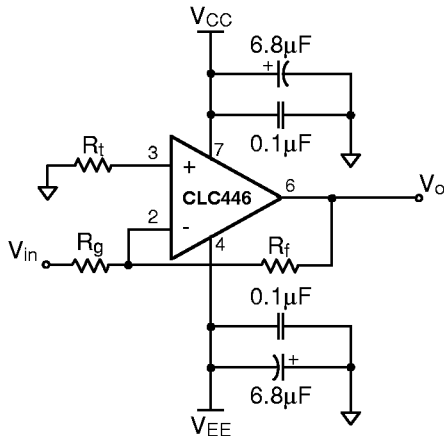

Figure 2: Inverting Gain

The normalized gain plots in the *Typical Performance Characteristics* section show different feedback resistors (R_f) for different gains. These values of R_f are recommended for obtaining the highest bandwidth with minimal peaking. The resistor R_t provides DC bias for the non-inverting input.

For $|A_v| < 5$, use linear interpolation on the nearest A_v values to calculate the recommended value of R_f. For $|A_v| \geq 5$, the minimum recommended R_f is 200Ω.

Select R_g to set the DC gain: $R_g = \dfrac{R_f}{|A_v|}$. At large gains, R_g becomes small and will load the previous stage. This can be solved by driving R_g with a low impedance buffer like the CLC111, or increasing R_f and R_g. See the *AC Design (small signal bandwidth)* sub-section for the tradeoffs.

DC gain accuracy is usually limited by the tolerance of R_f and R_g.

DC Gain (transimpedance)
Figure 3 shows a transimpedance circuit where the current I_{in} is injected at the inverting node. The current source's output resistance is much greater than R_f.

The DC transimpedance gain is: $A_R = \dfrac{V_o}{I_{in}} = -R_f$

The recommended R_f is 453Ω. Parasitic capacitance at the inverting node may require a slight increase of R_f to maintain a flat frequency response.

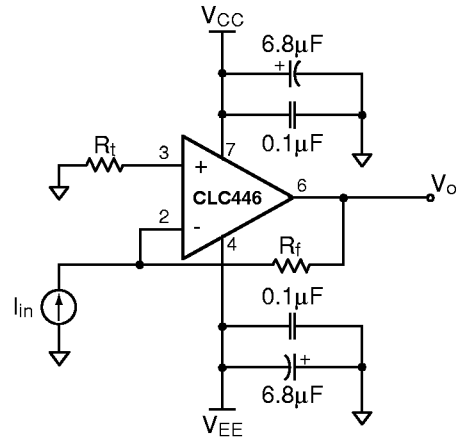DC gain accuracy is usually limited by the tolerance of R_f.

Figure 3: Transimpedance Gain

DC Design (level shifting)
Figure 4 shows a DC level shifting circuit for inverting gain configurations. V_{ref} produces a DC output level shift of $-V_{ref} \cdot \dfrac{R_f}{R_{ref}}$, which is independent of the DC output produced by V_{in}.
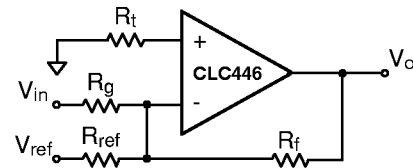

Figure 4: Level Shifting Circuit

DC Design (single supply)
Figure 5 is a typical single-supply circuit. R_1 and R_2 form a voltage divider that sets the non-inverting input DC voltage. This circuit has a DC gain of 1. A low frequency zero is set by R_g and C_2. The coupling capacitor C_1 isolates its DC bias point from the previous stage. Both capacitors make a high pass response; high frequency gain is determined by R_f and R_g.
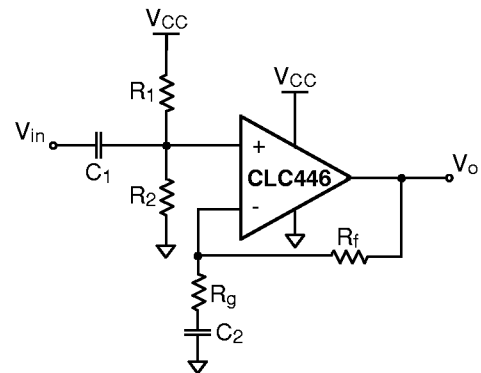

Figure 5: Single Supply Circuit

The complete gain equation for the circuit in Figure 5 is:

$$\frac{V_o}{V_{in}} = \frac{s\tau_1}{1+s\tau_1} \cdot \frac{1+s\tau_2 \cdot \left(1+\dfrac{R_f}{R_g}\right)}{1+s\tau_2}$$

5

where

$$s = j\omega$$

$$\tau_1 = (R_1 \| R_2) \cdot C_1$$

$$\tau_2 = R_g \cdot C_2$$

DC Design (DC offsets)

The DC offset model shown in Figure 6 is used to calculate the output offset voltage. The equation for output offset voltage is:

$$V_o = -\left(V_{os} + I_{BN} \cdot R_{eq1}\right) \cdot \left(1 + \frac{R_f}{R_{eq2}}\right) + \left(I_{BI} \cdot R_f\right)$$

The current offset terms, I_{BN} and I_{BI}, *do not track each other*. The specifications are stated in terms of magnitude only. Therefore, the terms V_{os}, I_{BN}, and I_{BI} can have either polarity. Matching the equivalent resistance seen at both input pins does not reduce the output offset voltage.
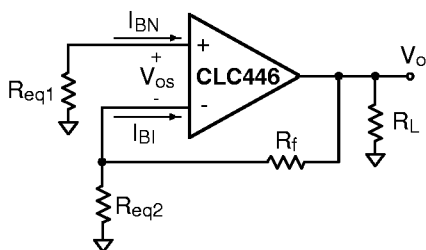

Figure 6: DC Offset Model

DC Design (output loading)

R_L, R_f, and R_g load the op amp output. The equivalent load seen by the output in Figure 6 is:

$R_{L(eq)} = R_L \| (R_f + R_{eq2})$, non-inverting gain
$R_{L(eq)} = R_L \| R_f$, inverting gain

$R_{L(eq)}$ needs to be large enough so that the minimum output current can produce the required output voltage swing.

AC Design (small signal bandwidth)

The CLC446 current-feedback amplifier bandwidth is a function of the feedback resistor (R_f), not of the DC voltage gain (A_V). The bandwidth is approximately proportional to $\frac{1}{R_f}$. As a rule, if R_f doubles, the bandwidth is cut in half. Other AC specifications will also be degraded. Decreasing R_f from the recommended value increases peaking, and *for very small values of* R_f *oscillation will occur.*

AC Design (minimum slew rate)

Slew rate influences the bandwidth of large signal sinusoids. To determine an approximate value of slew rate necessary to support a large sinusoid, use the following equation:

$$SR \cong 5 \cdot f \cdot V_{peak}$$

where V_{peak} is the peak output sinusoidal voltage.

The slew rate of the CLC446 in inverting gains is always higher than in non-inverting gains.

AC Design (linear phase/constant group delay)

The recommended value of R_f produces minimal peaking and a reasonably linear phase response. To improve phase linearity when $|A_V| < 5$, increase R_f approximately 50% over its recommended value. Some adjustment of R_f may be needed to achieve phase linearity for your application. See the ***AC Design (small signal bandwidth)*** sub-section for other effects of changing R_f.

Propagation delay is approximately equal to group delay. Group delay is related to phase by this equation:

$$\tau_{gd} = (f) = -\frac{1}{360°} \cdot \frac{d\phi(f)}{df} \approx -\frac{\Delta\phi(f)}{\Delta f}$$

where $\phi(f)$ is the phase in degrees. Linear phase implies constant group delay. The technique for achieving linear phase also produces a constant group delay.

AC Design (peaking)

Peaking is sometimes observed with the recommended R_f. If a small increase in R_f does not solve the problem, then investigate the possible causes and remedies listed below.

- Capacitance across R_f
    - Do not place a capacitor across R_f
    - Use a resistor with low parasitic capacitance for R_f
- A capacitive load
    - Use a series resistor between the output and a capacitive load (see the ***Recommended R_s vs. C_L*** plot)
- Long traces and/or lead lengths between R_f and the CLC446
    - Keep these traces as short as possible

For non-inverting and transimpedance gain configurations:

- Extra capacitance between the inverting pin and ground (C_g)
    - See the ***Printed Circuit Board Layout*** sub-section below for suggestions on reducing C_g
    - Increase R_f if peaking is still observed after reducing C_g

For inverting gain configurations:

- Inadequate ground plane at the non-inverting pin and/or long traces between non-inverting pin and ground
    - Place a 50 to 200Ω resistor between the non-inverting pin and ground (see R_t in Figure 2)

Capacitive Loads

Capacitive loads, such as found in A/D converters, require a series resistor (R_s) in the output to improve settling performance. The ***Recommended R_s vs. C_L*** plot in the ***Typical Performance Characteristics*** section provides the information for selecting this resistor.

Using a resistor in series with a reactive load will also reduce the load's effect on amplifier loop dynamics. For instance, driving coaxial cables without an output series resistor may cause peaking or oscillation.

Transmission Line Matching
One method for matching the characteristic impedance of a transmission line is to place the appropriate resistor at the input or output of the amplifier. Figure 7 shows the typical circuit configurations for matching transmission lines.
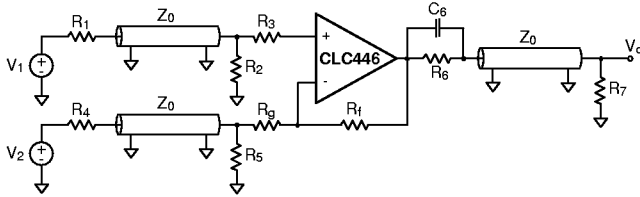
Figure 7: Transmission Line Matching

In non-inverting gain applications, R_g is connected directly to ground. The resistors R_1, R_2, R_6, and R_7 are equal to the characteristic impedance, Z_o, of the transmission line or cable. Use R_3 to isolate the amplifier from reactive loading caused by the transmission line, or by parasitics.

In inverting gain applications, R_3 is connected directly to ground. The resistors R_4, R_6, and R_7 are equal to Z_o. The parallel combination of R_5 and R_g is also equal to Z_o.

The input and output matching resistors attenuate the signal by a factor of 2, therefore additional gain is needed. Use C_6 to match the output transmission line over a greater frequency range. It compensates for the increase of the op amp's output impedance with frequency.

Thermal Design
To calculate the power dissipation for the CLC446, follow these steps:

1. Calculate the no-load op amp power:
$$P_{amp} = I_{CC} \cdot (V_{CC} - V_{EE})$$

2. Calculate the output stage's RMS power:
$$P_o = (V_{CC} - V_{load}) \cdot I_{load},$$ where V_{load} and I_{load} are the RMS voltage and current across the external load.

3. Calculate the total op amp RMS power:
$$P_t = P_{amp} + P_o$$

To calculate the maximum allowable ambient temperature, solve the following equation: $T_{amb} = 175 - P_t \cdot \theta_{JA}$, where θ_{JA} is the thermal resistance from junction to ambient in °C/W, and T_{amb} is in °C. The **Package Thermal Resistance** section contains the thermal resistance for various packages.

Dynamic Range (input /output protection)
ESD diodes are present on all connected pins for protection from static voltage damage. For a signal that

may exceed the supply voltages, we recommend using diode clamps at the amplifier's input to limit the signals to less than the supply voltages.

Dynamic Range (input /output levels)
The **Electrical Characteristics** section specifies the Common-Mode Input Range and Output Voltage Range; these voltage ranges scale with the supplies. Output Current is also specified in the **Electrical Characteristics** section.

Unity gain applications are limited by the Common-Mode Input Range. At greater non-inverting gains, the Output Voltage Range becomes the limiting factor. Inverting gain applications are limited by the Output Voltage Range. For transimpedance gain applications, the sum of the input currents injected at the inverting input pin of the op amp needs to be: $\left| I_{in} \right| \le \dfrac{V_{max}}{R_f}$,

where V_{max} is the Output Voltage Range (see the **DC Gain (transimpedance)** sub-section for details).

The equivalent output load needs to be large enough so that the minimum output current can produce the required output voltage swing. See the **DC Design (output loading)** sub-section for details.

Dynamic Range (noise)
In RF applications, noise is frequently specified as Noise Figure (NF). This allows the calculation of signal to noise ratio into a defined load. Figure 8 plots the NF for a CLC446 at a gain of 10, and with a feedback resistor R_f of 100Ω. The minimum NF (3.9dB) occurs when the source impedance equals 1600Ω.
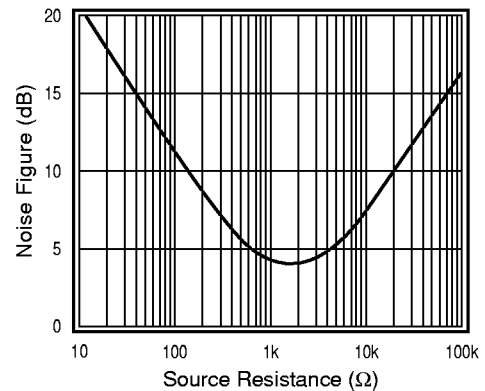
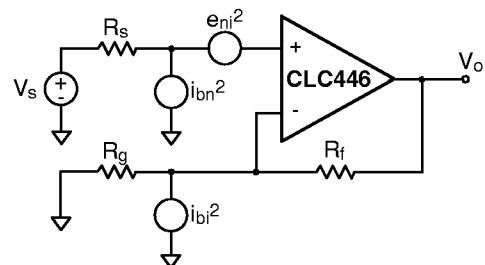**Figure 8: Noise Figure vs. Source Resistance**

Figure 9: Noise Model

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The CLC446 noise model in Figure 9 is used to develop this equation for NF:

$$NF = 10\log\left(\frac{e_{ni}^2 + (i_{bn}R_s)^2 + 4kTR_s + (i_{bi} \cdot R_f \| R_g)^2 + 4kT \cdot R_f \| R_g}{4kTR_s}\right)$$

where:
- R_S is the source resistance at the non-inverting input
- There is no matching resistor from the input to ground
- e_{ni}, i_{bn}, and i_{bi} are the voltage and current noise density terms (see the *Electrical Characteristics* section)
- $4kT = \left(16.0 \times 10^{-21} J\right) \cdot \left(\frac{T}{290°K}\right)$, T is in °K
- R_f is the feedback resistor, and R_g is the gain-setting resistor

To achieve a low Noise Figure while matching the source, use a matching transformer or the **Low Noise Composite Amp With Input Matching** circuit found in the **CLC446 Applications** section.

Dynamic Range (distortion)
The distortion plots in the Typical Performance Characteristics section show distortion as a function of load resistance, frequency, and output amplitude. Distortion places an upper limit on the CLC446's dynamic range.

Realized output distortion is highly dependent upon the external circuit. Some of the common external circuit choices that can improve distortion are:

- Short and equal return paths from the load to the supplies
- De-coupling capacitors of the correct value
- Higher load resistance
- A lower ratio of the output voltage swing to power supply voltage

Printed Circuit Board Layout
High Frequency op amp performance is strongly dependent on proper layout, proper resistive termination and adequate power supply decoupling. The most important layout points to follow are:

- Use a ground plane
- Bypass power supply pins with:
  - ceramic capacitors of about 0.1μF placed less than 0.1" (3mm) from the pin
  - tantalum capacitors of about 6.8μF for large signal current swings or improved power supply noise rejection; we recommend a minimum of 2.2μF for any circuit
- Minimize trace and lead lengths for components between the inverting and output pins
- Remove ground plane underneath the amplifier package and 0.1" (3mm) from all input/output pads

- For prototyping, use flush-mount printed circuit board pins; never use high profile DIP sockets

Evaluation Board
Separate evaluation boards are available for prototyping and measurements. Additional information is available in the evaluation board literature.

CLC446 Applications

Low Noise Composite Amp With Input Matching
The composite amp shown in Figure 10 eliminates the need for a matching resistor to ground at the input. By connecting two amplifiers in series, the first non-inverting and the second inverting, an overall inverting gain is realized. The feedback resistor (R_f) closes the loop, and generates a set input resistance (R_{in}) that can be matched to R_S. R_f generates less noise than a matching resistor to ground at the input.
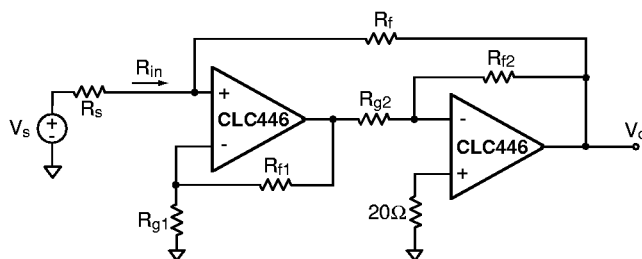

Figure 10: Composite Amplifier

The input resistance and DC voltage gain of the amplifier are:

$$R_{in} = \frac{R_f}{1+G} \text{ , where } G = \left(1 + \frac{R_{f1}}{R_{g1}}\right) \cdot \left(\frac{R_{f2}}{R_{g2}}\right)$$

$$\frac{V_o}{V_s} = -G \cdot \left(\frac{R_{in}}{R_{in} + R_s}\right)$$

Match the source resistance by setting: $R_{in} = R_S$.

The voltage noise produced by R_f, referred to the source V_S, is:

$$e_{Rf}^2 = 4kTR_s \cdot \left(\frac{R_s}{R_{in} \cdot (1+G)}\right)$$

The noise of a simple input matching resistor connected to ground can be calculated by setting G to 0 in this equation. Thus, this circuit reduces the thermal noise power produced by the matching resistor by a factor of (1+G).

Rectifier Circuit
Wide bandwidth rectifier circuits have many applications. Figure 11 shows a 200MHz wideband full-wave rectifier circuit using a CLC446 and a CLC522 amplifier. Schottky or PIN diodes are used for D_1 and D_2. They produce an active half-wave rectifier whose signals are taken at the feedback diode connection. The CLC522 takes the difference of the two half-wave rectified signals, producing a full-wave rectifier. The CLC522 is used at a gain of 5 to achieve high differential bandwidth. For best

high frequency performance, maintain low parasitic capacitance from the diodes D_1 and D_2 to ground, and from the input of the CLC522 to ground.
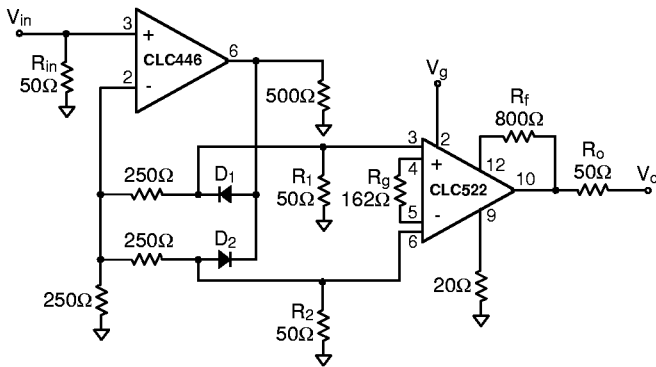

Figure 11: Full-Wave Rectifier

Elliptic Low-pass, Anti-aliasing Filter

Elliptic filters are often used in anti-aliasing applications. If there is noise or undesired signals at frequencies above 1/2 the sampling rate of an A/D converter, then these signals are aliased down into the operating frequency range, degrading the signal of interest. To filter out these undesired signal components, place a low pass filter in front of the A/D converter.

The *Typical Application* depicted on the front page is a 10MHz, third-order elliptic filter. It has a voltage-controlled, voltage source (VCVS) topology using a CLC446. To calculate the component values for this filter, do the following:

1. Select the filter approximation function for your application (see References [1-2]). For this design we chose:
   Filter type = Elliptic
   Filter order (n) = 3
   Passband ripple = 0.18dB
   Mininimum stopband attenuation (A_{min}) = 37.44dB
   Cuttoff frequency = 10MHz (at 0.18dB attenuation)
   These choices produce the following results:
   -3dB frequency = 12.7MHz
   Stopband corner frequency = 29.3MHz

2. Find the pole and zero locations. Reference [1] gave the following for our filter:
   Pole 1: $\alpha = 0.38621$
   Pole 2: $\alpha_o = 0.88668$
   Zero 1: $\beta = 1.13897$
   Zero 2: $\omega_\infty = 3.3505$

3. Denormalize the frequency by multiplying by the cutoff frequency (ω_o) in radians/second. For our filter we have:
   Cutoff frequency: $\omega_o = 2\pi(10\text{MHz}) = 62.832 \times 10^6 \text{rad/s}$
   Pole 1: $\alpha' = \omega_o\alpha = 24.266 \times 10^6 \text{rad/s}$
   Pole 2: $\alpha'_o = \omega_o\alpha_o = 55.712 \times 10^6 \text{rad/s}$
   Zero 1: $\beta' = \omega_o\beta = 21.052 \times 10^6 \text{rad/s}$
   Zero 2: $\omega'_\infty = \omega_o\omega_\infty = 71.564 \times 10^6 \text{rad/s}$

4. Calculate these intermediate coefficients used in Reference [2].

$$c = \sqrt{(\alpha')^2 + (\beta')^2} \qquad a = \frac{2\alpha'}{c} \qquad b = \left(\frac{\omega'_\infty}{c}\right)^2$$

For this design, a = 0.64226, b = 7.7612 and c = 75.556 x 10^6.

5. Set the following resistance and capacitance scaling factors:
   R = an arbitrary value
   C = an arbitrary value
   We chose C = 47pF and R = 1.00kΩ.

6. Calculate the capacitor, resistor and gain (K) values using these equations:

$$C_1 = C$$
$$C_3 = C_4 = \frac{C}{2}$$
$$C_2 \geq \frac{C(b-1)}{4}$$
$$R_3 = \frac{1}{cC\sqrt{b}}$$
$$R_1 = R_2 = \frac{R_3}{2}$$
$$R_4 = \frac{4\sqrt{b}}{cC(1-b)+4cC_2}$$
$$R_5 = R$$
$$C_5 = \frac{1}{R\alpha'_o}$$
$$K = 2 + \frac{2C_2}{C} - \frac{a}{2\sqrt{b}} + \frac{2}{C\sqrt{b}} \cdot \left(\frac{1}{cR_4} - aC_2\right)$$

For this design, the calculated values are:
C_1 = 47pF, C_2 = 91pF, C_3 = C_4 = 23.5pF, C_5 = 17.95pF, R_1 = R_2 = 202.1Ω, R_3 = 101.1Ω, R_4 = 3190Ω, R_5 = 1000Ω and K = 4.928.

7. Select the feedback resistor (R_f) and gain-setting resistor (R_g) values to obtain a non-inverting voltage gain of A_v = K. See the *DC Gain (non-inverting)* sub-section for details on selecting these values.

Figure 12 shows the ideal response of this filter. Some methods to bring actual performance closer to this ideal are:

- Compensate for op amp delay effects (pre-distortion)
- Adjust for parasitic capacitances in the layout
- Use components with small tolerances
- Add trim capacitors

Figure 12: Ideal Elliptic Filter Frequency Response

References:

[1] Anatol I. Zverev, *Handbook of FILTER SYNTHESIS*, John Wiley & Sons, 1967, p. 177

[2] Arthur B. Williams and Fred J. Taylor, *Electronic Filter Design Handbook*, McGraw Hill, 1995, pp. 3-29 to 3-31.
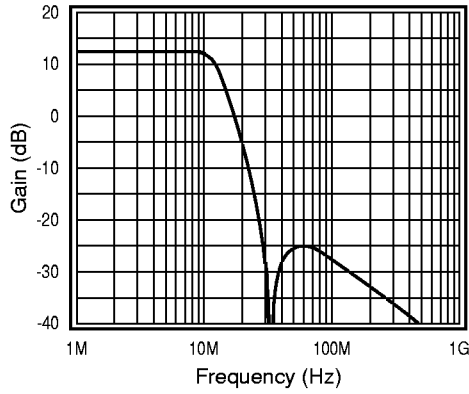
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