HARRIS

HM-6518

1024 x 1 CMOS RAM

Features

- HM-6100 Compatible
- Low Standby Power ..... 50μW Max
- Low Operating Power ..... 20mW/MHz Max.
- Fast Access Time ..... 180ns Max.
- Data Retention Voltage ..... 2.0V Min.
- TTL Compatible In/Out
- High Output Drive - 2 TTL Loads
- High Noise Immunity
- On Chip Address Register
- Two Chip Selects for Easy Array Expansion
- Three-State Outputs
- Wide Operating Temperature Ranges:
  - ▸ HM-6518-5 ..... 0°C to +70°C
  - ▸ HM-6518-9 ..... -40°C to +85°C
  - ▸ HM-6518-8 ..... -55°C to +125°C

Description

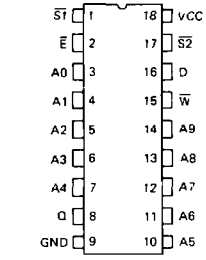
The HM-6518 is a 1024 by 1 static CMOS RAM fabricated using self-aligned silicon gate technology. Synchronous circuit design tecniques are employed to achieve high performance and low power operation.

On chip latches are provided for address and data outputs allowing efficient interfacing with microprocessor systems. The data output buffers can be forced to a high impedance state for use in expanded memory arrays.

The HM-6518 is a fully static RAM and may be maintained in any state for an indefinite period of time. Data retention supply voltage and supply current are guaranteed over temperature.

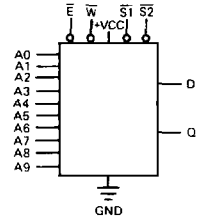
Pinout

TOP VIEW

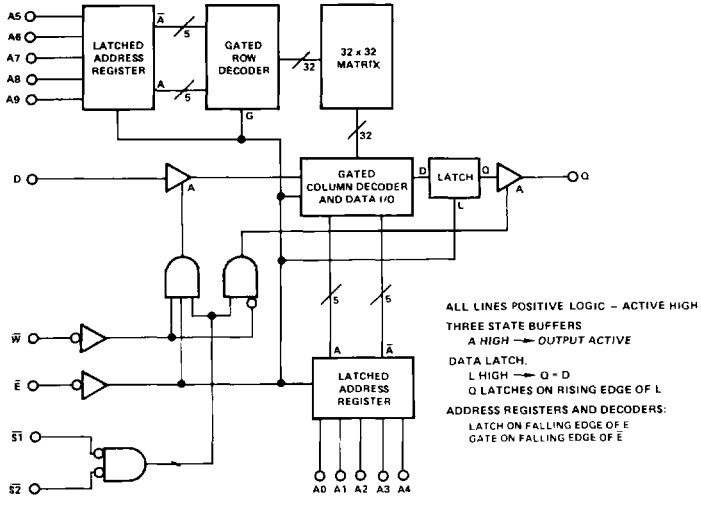


A-Address Input
E-Chip Enable
S-Chip Select
W-Write Enable
D-Data Input
Q-Data Output

Logic Symbol



Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings

Supply Voltage ..... +7.0V
Input, Output or I/O Voltage Applied ..... GND -0.3V to VCC +0.3V
Storage Temperature Range ..... -65°C to +150°C
Maximum Package Power Dissipation ..... 1 Watt
θ_{jc} ..... 18°C/W (CERDIP Package)
θ_{ja} ..... 75°C/W (CERDIP Package)
Gate Count ..... 1936 Gates
Junction Temperature ..... +150°C
Lead Temperature (Soldering, Ten Seconds) ..... +275°C

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V
Operating Temperature Ranges:
HM-6518-9 ..... -40°C to +85°C
HM-6518-8 ..... -55°C to +125°C

D.C. Electrical Specifications

VCC = 5V ± 10%; T_A = HM-6518-9 -40°C to +85°C
T_A = HM-6518-8 -55°C to +125°C

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
ICCSB	Standby Supply Current	-	10	µA	IO = 0, VI = VCC or GND
ICCOP	Operating Supply Current (Note 3)	-	4	mA	$\overline{E}$ = 1MHz, IO = 0, VI = VCC or GND
ICCDR	Data Retention Supply Current	-	10	µA	VCC = 2.0, IO = 0, VI = VCC or GND $\overline{E}$ = VCC
VCCDR	Data Retention Supply Voltage	2.0	-	V	
II	Input Leakage Current	-1.0	+1.0	µA	VI = VCC or GND
IOZ	Output Leakage Current	-1.0	+1.0	µA	VO = VCC or GND
VIL	Input Low Voltage	-0.3	0.8	V	
VIH	Input High Voltage	VCC-2.0	VCC+0.3	V	
VOL	Output Low Voltage	-	0.4	V	IO = 3.2mA
VOH	Output High Voltage	2.4	-	V	IO = -0.4mA

Capacitance

SYMBOL	PARAMETER	MAX	UNITS	TEST CONDITIONS
CI	Input Capacitance (Note 2)	6	pF	VI = VCC or GND, f = 1MHz
CO	Output Capacitance (Note 2)	10	pF	VO = VCC or GND, f = 1MHz

NOTES:
1. Input pulse levels: 0 to 3.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
2. Tested at initial design and after major design changes.
3. Typical derating 1.5mA/MHz increase in ICCOP.
4. VCC = 4.5V and 5.5V.

A.C. Electrical Specifications VCC = 5V ± 10%; T_A = HM-6518-9 -40°C to +85°C
T_A = HM-6518-8 -55°C to +125°C

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
(1) TELQV	Chip Enable Access Time	-	250	ns	(Notes 1, 4)
(2) TAVQV	Address Access Time	-	250	ns	(Notes 1, 4)
(3) TSLQX	Chip Select Output Enable Time	5	160	ns	(Notes 2, 4)
(4) TWLQZ	Write Enable Output Disable Time	-	160	ns	(Notes 2, 4)
(5) TSHQZ	Chip Select Output Disable Time	-	160	ns	(Notes 2, 4)
(6) TELEH	Chip Enable Pulse Negative Width	250	-	ns	(Notes 1, 4)
(7) TEHEL	Chip Enable Pulse Positive Width	100	-	ns	(Notes 1, 4)
(8) TAVEL	Address Setup Time	0	-	ns	(Notes 1, 4)
(9) TELAX	Address Hold Time	50	-	ns	(Notes 1, 4)
(10) TDVWH	Data Setup Time	110	-	ns	(Notes 1, 4)
(11) TWHDX	Data Hold Time	0	-	ns	(Notes 1, 4)
(12) TWLSH	Chip Select Write Pulse Setup Time	130	-	ns	(Notes 1, 4)
(13) TWLEH	Chip Enable Write Pulse Setup Time	130	-	ns	(Notes 1, 4)
(14) TSLWH	Chip Select Write Pulse Hold Time	130	-	ns	(Notes 1, 4)
(15) TELWH	Chip Enable Write Pulse Hold Time	130	-	ns	(Notes 1, 4)
(16) TWLWH	Write Enable Pulse Width	130	-	ns	(Notes 1, 4)
(17) TELEL	Read or Write Cycle Time	350	-	ns	(Notes 1, 4)

NOTES:

1. Input pulse levels: 0 to 3.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent CL = 50pF (min) ~ for CL greater than 50pF, access time is derated by 0.15ns per pF.
2. Tested at initial design and after major design changes.
3. Typical derating 1.5mA/MHz increase in ICCOP.
4. VCC = 4.5V and 5.5V.

Absolute Maximum Ratings

Supply Voltage ..... +7.0V
Input, Output or I/O Voltage Applied ..... GND -0.3V to VCC +0.3V
Storage Temperature Range ..... -65°C to +150°C
Maximum Package Power Dissipation ..... 1 Watt
θ_{jc} ..... 18°C/W (CERDIP Package)
θ_{ja} ..... 75°C/W (CERDIP Package)
Gate Count ..... 1936 Gates
Junction Temperature ..... +150°C
Lead Temperature (Soldering, Ten Seconds) ..... +275°C

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V
Operating Temperature Ranges:
HM-6518B-9 ..... -40°C to +85°C
HM-6518B-8 ..... -55°C to +125°C

D.C. Electrical Specifications

VCC = 5V ± 10%; T_A = HM-6518B-9 -40°C to +85°C
T_A = HM-6518B-8 -55°C to +125°C

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
ICCSB	Standby Supply Current	-	10	µA	IO = 0, VI = VCC or GND
ICCOP	Operating Supply Current (Note 3)	-	4	mA	$\overline{E}$ = 1MHz, IO = 0, VI = VCC or GND
ICCDR	Data Retention Supply Current	-	5	µA	VCC = 2.0, IO = 0, VI = VCC or GND $\overline{E}$ = VCC
VCCDR	Data Retention Supply Voltage	2.0	-	V	
II	Input Leakage Current	-1.0	+1.0	µA	VI = VCC or GND
IOZ	Output Leakage Current	-1.0	+1.0	µA	VO = VCC or GND
VIL	Input Low Voltage	-0.3	0.8	V	
VIH	Input High Voltage	VCC-2.0	VCC+0.3	V	
VOL	Output Low Voltage	-	0.4	V	IO = 3.2mA
VOH	Output High Voltage	2.4	-	V	IO = -0.4mA

Capacitance

SYMBOL	PARAMETER	MAX	UNITS	TEST CONDITIONS
CI	Input Capacitance (Note 2)	6	pF	VI = VCC or GND, f = 1MHz
CO	Output Capacitance (Note 2)	10	pF	VO = VCC or GND, f = 1MHz

NOTES:
1. *Input pulse levels: 0 to 3.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent* CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
2. Tested at initial design and after major design changes.
3. Typical derating 1.5mA/MHz increase in ICCOP.
4. VCC = 4.5V and 5.5V.

A.C. Electrical Specifications VCC = 5V ± 10%; T_A = HM-6518B-9 -40°C to +85°C
T_A = HM-6518B-8 -55°C to +125°C

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
(1) TELQV	Chip Enable Access Time	-	180	ns	(Notes 1, 4)
(2) TAVQV	Address Access Time	-	180	ns	(Notes 1, 4)
(3) TSLQX	Chip Select Output Enable Time	5	120	ns	(Notes 2, 4)
(4) TWLQZ	Write Enable Output Disable Time	-	120	ns	(Notes 2, 4)
(5) TSHQZ	Chip Select Output Disable Time	-	120	ns	(Notes 2, 4)
(6) TELEH	Chip Enable Pulse Negative Width	180	-	ns	(Notes 1, 4)
(7) TEHEL	Chip Enable Pulse Positive Width	100	-	ns	(Notes 1, 4)
(8) TAVEL	Address Setup Time	0	-	ns	(Notes 1, 4)
(9) TELAX	Address Hold Time	40	-	ns	(Notes 1, 4)
(10) TDVWH	Data Setup Time	80	-	ns	(Notes 1, 4)
(11) TWHDX	Data Hold Time	0	-	ns	(Notes 1, 4)
(12) TWLSH	Chip Select Write Pulse Setup Time	100	-	ns	(Notes 1, 4)
(13) TWLEH	Chip Enable Write Pulse Setup Time	100	-	ns	(Notes 1, 4)
(14) TSLWH	Chip Select Write Pulse Hold Time	100	-	ns	(Notes 1, 4)
(15) TELWH	Chip Enable Write Pulse Hold Time	100	-	ns	(Notes 1, 4)
(16) TWLWH	Write Enable Pulse Width	100	-	ns	(Notes 1, 4)
(17) TELEL	Read or Write Cycle Time	280	-	ns	(Notes 1, 4)

NOTES:
1. Input pulse levels: 0 to 3.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
2. Tested at initial design and after major design changes.
3. Typical derating 1.5mA/MHz increase in ICCOP.
4. VCC = 4.5V and 5.5V.

Absolute Maximum Ratings

Supply Voltage ..... +7.0V
Input, Output or I/O Voltage Applied ..... GND -0.3V to VCC +0.3V
Storage Temperature Range ..... -65°C to +150°C
Maximum Package Power Dissipation ..... 1 Watt
θ_{jc} ..... 18°C/W (CERDIP Package)
θ_{ja} ..... 75°C/W (CERDIP Package)
Gate Count ..... 1936 Gates
Junction Temperature ..... +150°C
Lead Temperature (Soldering, Ten Seconds) ..... +275°C

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V
Operating Temperature Ranges:
HM-6518-5 ..... 0°C to +70°C

D.C. Electrical Specifications VCC = 5V ± 10%; T_A = HM-6518-5 0°C to +70°C

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
ICCSB	Standby Supply Current	-	100	µA	IO = 0, VI = VCC or GND
ICCOP	Operating Supply Current (Note 3)	-	4	mA	$\overline{E}$ = 1MHz, IO = 0, VI = VCC or GND
ICCDR	Data Retention Supply Current	-	100	µA	VCC = 2.0, IO = 0, VI = VCC or GND $\overline{E}$ = VCC
VCCDR	Data Retention Supply Voltage	2.0	-	V	
II	Input Leakage Current	-1.0	+1.0	µA	VI = VCC or GND
IOZ	Output Leakage Current	-1.0	+1.0	µA	VO = VCC or GND
VIL	*Input* Low Voltage	-0.3	0.8	V	
VIH	Input High Voltage	VCC-2.0	VCC+0.3	V	
VOL	Output Low Voltage	-	0.4	V	IO = 1.6mA
VOH	Output High Voltage	2.4	-	V	IO = -0.2mA

Capacitance

SYMBOL	PARAMETER	MAX	UNITS	TEST CONDITIONS
CI	Input Capacitance (Note 2)	6	pF	VI = VCC or GND, f = 1MHz
CO	Output Capacitance (Note 2)	10	pF	VO = VCC or GND, f = 1MHz

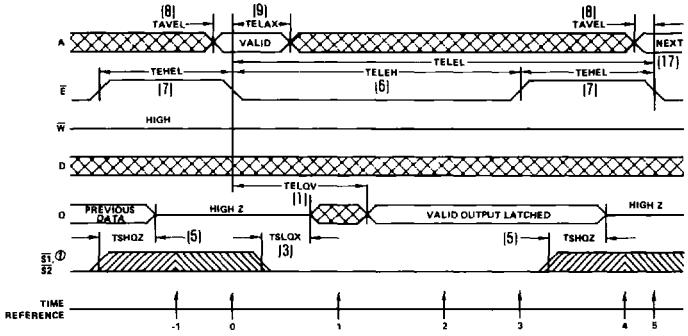
NOTES:
1. Input pulse levels: 0 to 3.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
2. *Tested at initial design and after major design changes.*
3. Typical derating 1.5mA/MHz increase in ICCOP.
4. VCC = 4.5V and 5.5V.

A.C. Electrical Specifications VCC = 5V ± 10%; T_A = HM-6518-5 0°C to +70°C

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
(1) TELQV	Chip Enable Access Time	-	300	ns	(Notes 1, 4)
(2) TAVQV	Address Access Time	-	310	ns	(Notes 1, 4)
(3) TSLQX	Chip Select Output Enable Time	5	200	ns	(Notes 2, 4)
(4) TWLQZ	Write Enable Output Disable Time	-	200	ns	(Notes 2, 4)
(5) TSHQZ	Chip Select Output Disable Time	-	200	ns	(Notes 2, 4)
(6) TELEH	Chip Enable Pulse Negative Width	300	-	ns	(Notes 1, 4)
(7) TEHEL	Chip Enable Pulse Positive Width	150	-	ns	(Notes 1, 4)
(8) TAVEL	Address Setup Time	10	-	ns	(Notes 1, 4)
(9) TELAX	Address Hold Time	50	-	ns	(Notes 1, 4)
(10) TDVWH	Data Setup Time	130	-	ns	(Notes 1, 4)
(11) TWHDX	Data Hold Time	0	-	ns	(Notes 1, 4)
(12) TWLSH	Chip Select Write Pulse Setup Time	160	-	ns	(Notes 1, 4)
(13) TWLEH	Chip Enable Write Pulse Setup Time	160	-	ns	(Notes 1, 4)
(14) TSLWH	Chip Select Write Pulse Hold Time	160	-	ns	(Notes 1, 4)
(15) TELWH	Chip Enable Write Pulse Hold Time	160	-	ns	(Notes 1, 4)
(16) TWLWH	Write Enable Pulse Width	160	-	ns	(Notes 1, 4)
(17) TELEL	Read or Write Cycle Time	450	-	ns	(Notes 1, 4)

NOTES:
1. Input pulse levels: 0 to 3.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
2. Tested at initial design and after major design changes.
3. Typical derating 1.5mA/MHz increase in ICCOP.
4. VCC = 4.5V and 5.5V.

Read Cycle



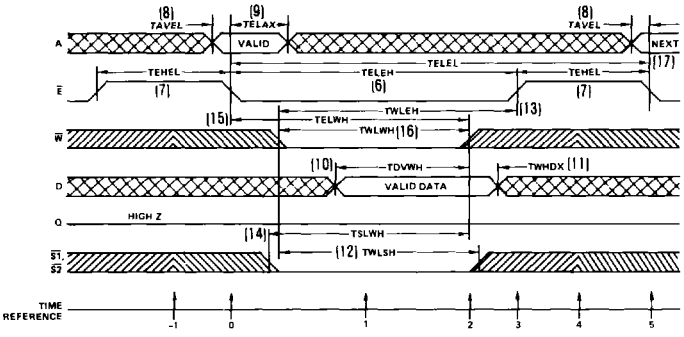
TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	$\overline{S1}$	$\overline{W}$	A	D	OUTPUT Q	FUNCTION
-1	H	H	X	X	X	Z	Memory Disabled
0	↓	X	H	V	X	Z	Cycle Begins, Addresses are Latched
1	L	L	H	X	X	X	Output Enabled
2	L	L	H	X	X	V	Output Valid
3	↑	L	H	X	X	V	Output Latched
4	H	H	X	X	X	Z	Device Disabled, Prepare for Next Cycle (Same as -1)
5	↓	X	H	V	X	Z	Cycle Ends, Next Cycle Begins (Same as 0)

NOTE: 1. Device selected only if both $\overline{S1}$ and $\overline{S2}$ are low, and deselected if either $\overline{S1}$ or $\overline{S2}$ are high

In the HM-6518 read cycle the address information is latched into the on chip registers on the falling edge of $\overline{E}$ (T = 0). Minimum address setup and hold time requirements must be met. After the required hold time the addresses may change state without affecting device operation. In order for the output to be read $\overline{S1}$, $\overline{S2}$ and $\overline{E}$ must be low, $\overline{W}$ must be high. When $\overline{E}$ goes high the output data is latched into an on chip register. Taking either or both $\overline{S1}$ or $\overline{S2}$ high forces the output buffer to a high impedance state. The output data may be re-enabled at any time by taking $\overline{S1}$ and $\overline{S2}$ low. On the falling edge of $\overline{E}$ the data will be unlatched.

Write Cycle



TRUTH TABLE

TIME REFERENCE	INPUTS $\overline{E}$	$\overline{S1}$	$\overline{W}$	A	D	OUTPUT Q	FUNCTION
-1	H	X	X	X	X	Z	Memory Disabled
0	↓	X	X	V	X	Z	Cycle Begins, Addresses are Latched
1	L	L	L	X	V	Z	Write Mode has Begun
2	L	↑	L	X	V	Z	Data is Written
3	↑	X	X	X	X	Z	Write Completed
4	H	X	X	X	X	Z	Prepare for Next Cycle (Same as -1)
5	↓	X	X	V	X	Z	Cycle Ends, Next Cycle Begins (Same as 0)

NOTE: 1. Device selected only if both $\overline{S1}$ and $\overline{S2}$ are low, and deselected if either $\overline{S1}$ or $\overline{S2}$ are high.

The write cycle is initiated by the falling edge of $\overline{E}$ which latches the address information into the on chip registers. The write portion of the cycle is defined as $\overline{E}$, $\overline{W}$, $\overline{S1}$ and $\overline{S2}$ being low simultaneously. $\overline{W}$ may go low anytime during the cycle provided that the write enable pulse setup time (TWLEH) is met. The write portion of the cycle is terminated by the first rising edge of either $\overline{E}$, $\overline{W}$, $\overline{S1}$ or $\overline{S2}$. Data setup and hold times must be referenced to the terminating signal.

If a series of consecutive write cycles are to be performed, the $\overline{W}$ line may remain low until all desired locations have been written. When this method is used, data setup and hold times must be referenced to the rising edge of $\overline{E}$. By positioning the $\overline{W}$ pulse at different times within the $\overline{E}$ low time (TELEH), various types of write cycles may be performed. If the $\overline{E}$ low time (TELEH) is greater than the $\overline{W}$ pulse (TWLWH) plus an output enable time (TSLQX), a combination read write cycle is executed. Data may be modified an indefinite number of times during any write cycle (TELEH).

The data input and data output pins may be tied together for use with a common I/O data bus structure. When using the RAM in this method allow a minimum of one output disable time (TWLQZ) after $\overline{W}$ goes low before applying input data to the bus. This will insure that the output buffers are not active.