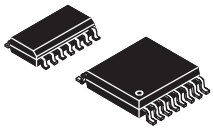




# ADVANCED HIGH-POWER FACTOR PREREGULATOR

## FEATURES

- **Controls Boost PWM to Near-Unity Power Factor**
- **Limits Line Current Distortion To <3%**
- **World-Wide Operation Without Switches**
- **Accurate Power Limiting**
- **Fixed-Frequency Average Current-Mode Control**
- **High Bandwidth (5 MHz), Low-Offset Current Amplifier**
- **Integrated Current- and Voltage-Amplifier Output Clamps**
- **Multiplier Improvements: Linearity, 500 mV $V_{AC}$ Offset (Eliminates External Resistor), 0 V to 5 V Multout Common-Mode Range**
- **$V_{REF}$ GOOD Comparator**
- **Faster and Improved Accuracy ENABLE Comparator**
- **UVLO Options (16 V/10 V or 10.5 V/10 V)**
- **300-μA Start-Up Supply Current**

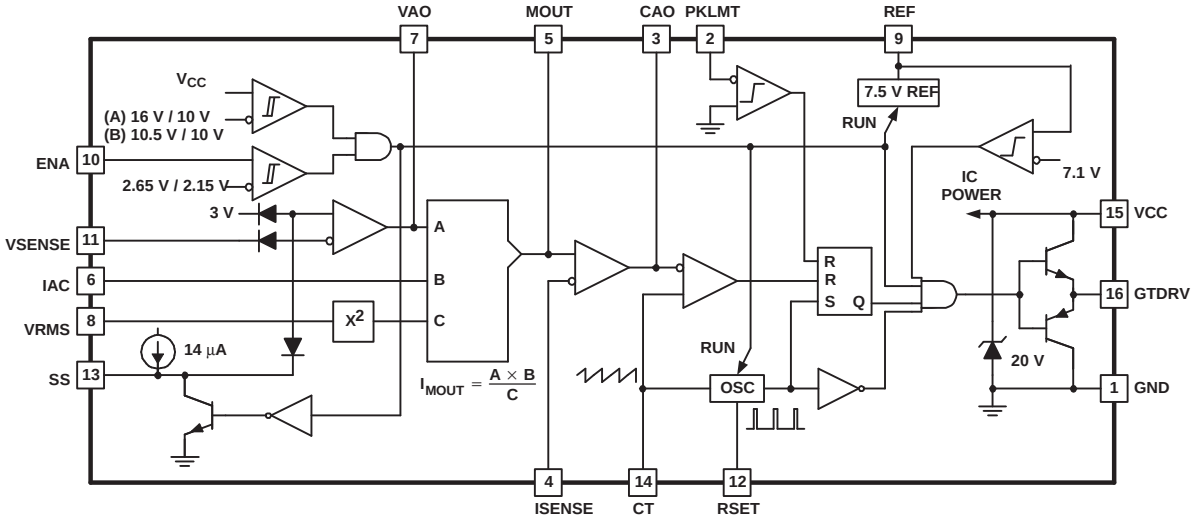
## DESCRIPTION

The UC3854A/B products are pin compatible enhanced versions of the UC3854. Like the UC3854, these products provide all of the functions necessary for active power factor corrected preregulators. The controller achieves near unity power factor by shaping the ac input line current waveform to correspond to the ac input line voltage. To do this the UC3854A/B uses average current mode control. Average current mode control maintains stable, low distortion sinusoidal line current without the need for slope compensation, unlike peak current mode control.

A 1%, 7.5-V reference, fixed frequency oscillator, PWM, voltage amplifierwith soft-start, line voltage feedforward ($V_{RMS}$ squarer), input supply voltage clamp, and over current comparator round out the lilst of feataures.

Available in the 16-pin N (PDIP), DW (SOIC Wide), and J (CDIP) and 20-pin Q (PLCC) package. See Ordering Information table for availability by temperature range.

## BLOCK DIAGRAM



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## DESCRIPTION (CONTINUED)

The UC3854A/B products improve upon the UC3854 by offering a wide bandwidth, low offset current amplifier, a faster responding and improved accuracy enable comparator, a VREF GOOD comparator, UVLO threshold options (16 V/10 V for offline, 10.5 V/10 V for startup from an auxiliary 12-V regulator), lower startup supply current, and an enhanced multiply/divide circuit. New features like the amplifier output clamps, improved amplifier current sinking capability, and low offset VAC pin reduce the external component count while improving performance. Improved common mode input range of the multiplier output/current amplifier input allow the designer greater flexibility in choosing amethod for current sensing. Unlike its predecessor, $R_{SET}$ controls only oscillator charging current and has no effect on clamping the maximum multiplier output current. This current is now clamped to a maximum of $2 \times I_{AC}$ at all times which simplifies the design process and provides foldback power limiting during brownout and extreme low line conditions.

### ORDERING INFORMATION

| $T_A$ | UVLO TURN-ON (V) | UVLO TURN-OFF (V) | PART NUMBERS | | | |
|---|---|---|---|---|---|---|
| | | | CDIP-16 (V) | PDIP-16 (N) | SOIC-16 (DW) | PLCC-20 (Q) |
| –55°C to 125°C | 16 | 10 | – | – | – | – |
| | 10.5 | 10 | UC1854BJ | – | – | – |
| –40°C to 85°C | 16 | 10 | UC2854AJ | UC2854AN | UC2854ADW | UC2854AQ |
| | 10.5 | 10 | UC2854BJ | UC2854BN | UC2854BDW | UC2854BQ |
| 0°C to 70°C | 16 | 10 | – | UC2854AN | UC2854ADW | – |
| | 10.5 | 10 | – | UC2854BN | UC2854BDW | – |

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

| | | | UCX854A, UCX854B | UNIT |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 22 | V |
| $I_{GTDRV}$ | GTDRV current | Continuous | 0.5 | A |
| | | 50% duty cycle | 1.5 | |
| | Input voltage | VSENSE, VRMS, ISENSE MOUT | 11 | V |
| | | PKLMT | 5 | |
| | Input current | RSET, IAC, PKLMT, ENA | 10 | mA |
| | Power dissipation | | 1 | W |
| $T_J$ | Junction temperature | | –55 to 150 | °C |
| $T_{stg}$ | Storage temperature | | –65 to 150 | |
| $T_{sol}$ | Lead temperataure, 1,6 mm (1/16 inch) from case for 10 seconds | | 300 | |

(1) Stresses beyond those listed under *absolutemaximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periodsmayaffect device reliability. All voltages arewith respect to GND. Currents are positive into and negative out of, the specified terminal. ENA input is internally clamped to approximately 10 V.

## RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 10 | 20 | V |
| $T_J$ | Operating junction temperature | UC1854X | –55 | 125 | °C |
| | | UC2854X | –40 | 85 | |
| | | UC3854X | 0 | 70 | |

## THERMAL RESISTANCE

| RESISTANCES | PACKAGED DEVICES | | | |
|---|---|---|---|---|
| | CDIP-16 (J) | PDIP-16 (N) | SOP-16 (DW) | PLCC-20 (Q) |
| $\theta_{JC}$ (°C/W) | 28 (1) | 45 | 27 | 34 |
| $\theta_{JA}$ (°C/W) | 80–120 | 90 (2) | 50–130 (2) | 43–75 (2) |

(1) $\theta_{JC}$ data values stated are derived from MIL-STD-1835B which states gthe baseline values shown are worst case (mean +2s) for a 60 × 60 mil microcircuit device silicon die and applicable for devices with die sizes up to 14,400 square mils. For device die sizes greater than 14,400 square mils use the following values, dual-in-line, 11°C/W; flat pack and pin grid array, 10°C/W.are at the end of each trace.

(2) $\theta_{JA}$ (junction-to-ambient) applies to devices mounted to five square inch FR4 PC board with one ounce copper where noted. When resitance range is given, lower values are for five square inch aluminum PC board. Test PWB is 0.062 inches thick and typically uses 0,635 mm trace widths for power packages and 1,3 mm trace widths for non-power packages with a 100 × 100 mil probe land are at the end of each trace.

## ELECTRICAL CHARACTERISTICS

$V_{CC}$ = 18 V, $R_T$ = 8.2 kΩ, $C_T$ = 1.5 nF, $V_{PKLMT}$ = 1 V, $V_{VRMS}$ = 1.5 V, $I_{IAC}$ = 100 µA, $I_{ISENSE}$ = 0 V, $V_{CAO}$ = 3.5 V, $V_{VAO}$ = 5 V, $V_{VSENSE}$ = 3 V, –40°C < $T_A$ < 85°C for the UC2854A and UC2854B, and 0°C < $T_A$ < 70°C for the UC3854A and UC3854B, and $T_A$ = $T_J$ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **OVERALL** | | | | | | | |
| | Supply current, off | CAO = 0 V, $V_{CC}$ = $V_{UVLO}$–0.3 V | VAO = 0 V, | | 250 | 400 | µA |
| | Supply current, on | | | | 12 | 18 | mA |
| | $V_{CC}$ turn-on threshold voltage | UCx854A | | 15.0 | 16.0 | 17.5 | V |
| | | UCx854B | | 8.0 | 10.5 | 11.2 | |
| | $V_{CC}$ turn-off threshold voltage | UCx854A | | 9 | 10 | 12 | |
| | | UCx854B | | 7.8 | 10.3 | 11.0 | |
| | $V_{CC}$ hysteresis | UCx854A | | 5 | 6 | 7 | |
| | | UCx854B | | 0.10 | 0.22 | 0.50 | |
| | $V_{CC}$ clamp | $I_{VCC}$ = $I_{VCC(on)}$ + 5 mA | | 18 | 20 | 22 | |
| **VOLTAGE AMPLIFIER** | | | | | | | |
| | Input voltage | | | 2.9 | 3.0 | 3.1 | V |
| | $V_{SENSE}$ bias current | | | –500 | —25 | 500 | nA |
| | Open loop gain | 2 V ≤ $V_{OUT}$ ≤ 5 V | | 70 | 100 | | dB |
| $V_{OH}$ | High-level output voltage | $I_{LOAD}$ = –500 µA | | | 6 | | V |
| $V_{OL}$ | Low-level output voltage | $I_{LOAD}$ = 500 µA | | | 0.3 | 0.5 | |
| $I_{SC}$ | Output short-circuit current | $V_{OUT}$ = 0 V | | | 1.5 | 3.5 | mA |
| | Gain bandwidth product(1) | $f_{IN}$ = 100 kHz, | 10 mVp-p | | 1 | | MHz |
| **CURRENT AMPLIFIER** | | | | | | | |
| | Input offset voltage | $V_{CM}$ = 0 V, | $T_A$ = 25°C | –4 | | 0 | mV |
| | | $V_{CM}$ = 0 V, | Overtemperature | –5.5 | | 0 | |
| $I_{SENSE}$ | Input bias current | $V_{CM}$ = 0 V | | –500 | | 500 | nA |
| | Open loop gain | 2 V ≤ $V_{OUT}$ = 6 V | | 80 | 110 | | dB |
| $V_{OH}$ | High-level output voltage | $I_{LOAD}$ = –500 µA | | | 8 | | V |
| $V_{OL}$ | Low-level output voltage | $I_{LOAD}$ = 500 µA | | | 0.3 | 0.5 | |
| $I_{SC}$ | Output short-circuit current | $V_{OUT}$ = 0 V | | | 1.5 | 3.5 | mA |
| CMRR | Common mode rejection range | | | –0.3 | | 5.0 | V |
| | Gain bandwidth product(1) | $f_{IN}$ = 100 kHz, | 10 mVp-p | 3 | 5 | | MHz |
| **REFERENCE** | | | | | | | |
| | Output voltage | $I_{REF}$ = 0 mA, | $T_A$ = 25°C | 7.4 | 7.5 | 7.6 | V |
| | | $I_{REF}$ = 0 mA | | 7.35 | 7.50 | 7.65 | |
| | Load regulation | 1 mA ≤ $I_{REF}$ ≤ 10 mA | | 0 | 8 | 20 | mV |
| | Line regulation | 12 V ≤ $V_{CC}$ ≤ 18 V | | 0 | 14 | 25 | |
| $I_{SC}$ | Short circuit current | $V_{REF}$ = 0 V | | 25 | 35 | 60 | mA |

(1) Ensured by design. Not production tested.

## ELECTRICAL CHARACTERISTICS (Continued)

$V_{CC}$ = 18 V, $R_T$ = 8.2 kΩ, $C_T$ = 1.5 nF, $V_{PKLMT}$ = 1 V, $V_{VRMS}$ = 1.5 V, $I_{IAC}$ = 100 µA, $I_{ISENSE}$ = 0 V, $V_{CAO}$ = 3.5 V, $V_{VAO}$ = 5 V, $V_{VSENSE}$ = 3 V, –40°C < $T_A$ < 85°C for the UC2854A and UC2854B, and 0°C < $T_A$ < 70°C for the UC3854A and UC3854B, and $T_A$ = $T_J$ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **OSCILLATOR** | | | | | | | |
| | Initial accuracy | $T_A$ = 25°C | | 85 | 100 | 115 | kHz |
| | Voltage stability | 12 V ≤ $V_{CC}$ ≤ 18 V | | | 1% | | |
| | Total variation | Line, temperature | | 80 | | 120 | kHz |
| | Ramp amplitude (peak-to-peak) | | | 4.9 | | 5.9 | V |
| | Ramp valley voltage | | | 0.8 | | 1.3 | V |
| **ENABLE/SOFT-START/CURRENT LIMIT** | | | | | | | |
| | Enable threshold voltage | | | 2.35 | 2.55 | 2.80 | V |
| | Enaable hysteresis | $V_{FAULT}$ = 2.5 V | | | 500 | 600 | mV |
| | Enable input bias current | $V_{ENA}$ = 0 V | | | –2 | –5 | µA |
| | Propagation delay to disable time(1) | Enable overdrive = 100 mV | | | 300 | | ns |
| | Soft-start charge current | $V_{SS}$ = 2.5 V | | 10 | 14 | 24 | µA |
| | Peak limit offset voltage | | | –15 | | 15 | mV |
| | Peak limit offset current | $V_{PKLMIT}$ = –0.1 V | | –200 | –100 | | µA |
| | Peak limit propagation delay time(1) | | | | 150 | | ns |
| **MULTIPLIER** | | | | | | | |
| | Output current, $I_A$ limited | $I_{AC}$ = 100 µA, $R_{SET}$ = 10 kΩ | $V_{RMS}$ = 1 V, | –220 | –200 | –170 | µA |
| | Output current, zero | $I_{AC}$ = 0 µA, | $R_{SET}$ = 10 kΩ | –2.0 | –0.2 | 2.0 | µA |
| | Output current, power limited | $V_{RMS}$ = 1.5 V | Va = 6 V | –230 | –200 | –170 | µA |
| | Output current | $V_{RMS}$ = 1.5 V | Va = 2 V | | –22 | | µA |
| | | $V_{RMS}$ = 1.5 V | Va = 5 V | | –156 | | |
| | | $V_{RMS}$ = 5 V | Va = 2 V | | –2 | | |
| | | $V_{RMS}$ = 5 V | Va = 5 V | | –14 | | |
| | Gain constant(2) | $V_{RMS}$ = 1.5 V | Va = 6 V, $T_A$ = 25°C | –1.1 | –1.0 | –0.9 | A/A |
| **GATE DRIVER** | | | | | | | |
| $V_{OH}$ | High-level output voltage | $I_{OUT}$ = –200 mA, | $V_{CC}$ = 15 V | 12.0 | 12.8 | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OUT}$ = 200 mA | | | 1.0 | 2.2 | V |
| | | $I_{OUT}$ = 10 mA | | | 300 | 500 | mV |
| | Low-level UVLO voltage | $I_{OUT}$ = 50 mA, | $V_{CC}$ = 0 V | | 0.9 | 1.5 | V |
| | Output rise time(1) | $C_{LOAD}$ = 1 nF | | | 35 | | ns |
| | Output fall time(1) | $C_{LOAD}$ = 1 nF | | | 35 | | ns |
| | Output peak current(1) | $C_{LOAD}$ = 10 nF | | | 1.0 | | A |

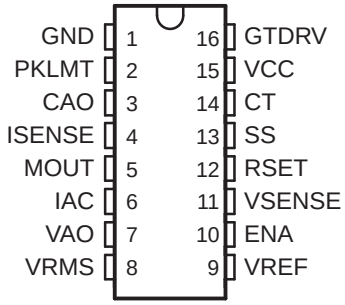
(1) Ensured by design. Not production tested.

$$(K) = \frac{I_{IAC} \times (V_{VAO} - 1.5V)}{\left[ (V_{VRMS})^2 \times I_{MOUT} \right]}$$

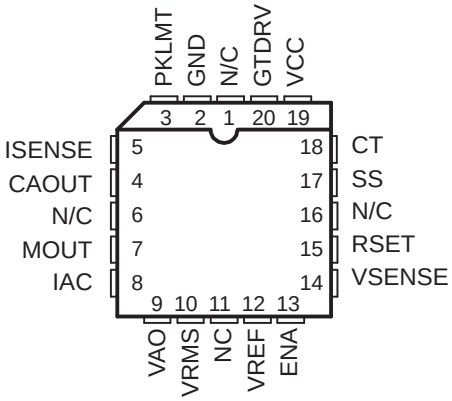
(2) Gain constant.

## PACKAGE DESCRIPTION

**J, N and DW PACKAGES**
**(TOP VIEW)**




**Q PACKAGE**
**(TOP VIEW)**




N/C − No connection

## TERMINAL FUNCTIONS

| TERMINAL | | | I/O | DESCRIPTION |
|---|---|---|---|---|
| NAME | PACKAGES | | | |
| | J/N/DW | Q/L | | |
| CAO | 3 | 4 | O | Output of the wide bandwidth current amplifier and one of the inputs to the PWM duty-cycle comparator. The output signal generated by this amplifier commands the PWM to force the correct input current. The output can swing from 0.1 V to 7.5 V. |
| CT | 14 | 18 | I | Capacitor from CT to GND sets the PWM oscillator frequency. |
| ENA | 10 | 13 | I | A nominal voltage above 2.65 V on this pin allows the device to begin operating. Once operating, the device shuts off if this pin goes below 2.15 V nominal. |
| GND | 1 | 2 | – | All bypass and timing capacitors connected to GND should have leads as short and direct as possible. All voltages are measured with respect GND. |
| GTDRV | 16 | 20 | O | Output of the PWM is a 1.5-A peak totem-pole MOSFET gate driver on GTDRV. Use a series gate resistor of at least 5 Ω to prevent interaction between the gate impedance and the GTDRV output driver that might cause the GTDRV output to overshoot excessively. Some overshoot of the GTDRV output is always expected when driving a capacitive load. |
| IAC | 6 | 8 | I | Current input to the multiplier, proportional to the instantaneous line voltage. This input to the analog multiplier is a current. The multiplier is tailored for very low distortion from this current input (IAC) to MOUT, so this is the only multiplier input that should be used for sensing instantaneous line voltage. |
| ISENSE | 4 | 5 | I | Switch current sensing input. This is the inverting input to the current amplifier. This input and the non-inverting input MOUT remain functional down to and below GND. Care should be taken to avoid taking these inputs below –0.5 V, because they are protected with diodes to GND. |
| MOUT | 5 | 7 | I/O | Multiplier output and current sense plus. The output of the analog multiplier and the non-inverting input of the current amplifier are connected together at MOUT. The cautions about taking ISENSE below –0.5 V also apply to MOUT. As the multiplier output is a current, this is a high-impedance input similar to $I_{SENSE}$, so the current amplifier can be configured as a differential amplifier to reject GND noise. $I_{MOUT} \leq 2 \times I_{AC}$ |
| PKLMT | 2 | 3 | I | Peak limit. The threshold for PKLMT is 0.0 V. Connect this input to the negative voltage on the current sense resistor. Use a resistor to REF to offset the negative current sense signal up to GND. |
| RSET | 12 | 15 | I | Oscillator charging current and multiplier limit set. A resistor from RSET to ground programs oscillator charging current. |
| SS | 13 | 17 | I | Soft-start. SS remains at GND as long as the device is disabled or $V_{CC}$ is too low. SS pulls up to over 3 V by an internal 14-μA current source when both $V_{CC}$ becomes valid and the device is enabled. SS acts as the reference input to the voltage amplifier if SS is below VREF. With a large capacitor from SS to GND, the reference to the voltage regulating amplifier rises slowly, and increase the PWM duty cycle slowly. In the event of a disable command or a supply dropout, SS will quickly discharge to ground and disable the PWM. |
| VAO | 7 | 9 | I | Voltage amplifier output |
| VCC | 15 | 19 | I | Positive supply rail |
| VREF | 9 | 12 | O | Used to set the peak limit point and as an internal reference for various device functions. This voltage must be present for the device to operate. |
| VRMS | 8 | 10 | I | One of the inputs into the multiplier. This pin provides the input RMS voltage to the multiplier circuitry. |
| VSENSE | 11 | 14 | I | This pin provides the feedback from the output. This input goes into the voltage error amplifier and the output of the error amplifier is another of the inputs into the multiplier circuit. |

## FUNCTIONAL DESCRIPTION

The UC3854A and UC3854B family of products are designed as pin compatible upgrades to the industry standard UC3854 active power factor correction circuits. The circuit enhancements allow the user to eliminate in most cases several external components currently required to successfully apply the UC3854. In addition, linearity improvements to the multiply, square and divide circuitry optimizes overall system performance. Detailed descriptions of the circuit enhancements are provided below. For in-depth design applications reference data refer to the application notes, *UC3854 Controlled Power Factor Correction Circuit Design* (SLUA144) and *UC3854A and UC3854B Advanced Power Factor Correction Control ICs* (SLUA177).

### Multiply/Square and Divide

The UC3854A/B multiplier design maintains the same gain constant $\left(K = \frac{-1}{V}\right)$ as the UC3854. The relationship between the inputs and output current is given as:

$$I_{MOUT} = I_{IAC} \times \frac{\left(V_{VAO} - 1.5V\right)}{K \times \left(V_{VRMS}\right)^2} \tag{1}$$

This is nearly the same as the UC3854, but circuit differences have improved the performance and application.

The first difference is with the IAC input. The UC3854A/B regulated this pin voltage to the nominal 500 mV over the full operating temperature range, rather than the 6.0 V used on the UC3854. The low offset voltage eliminates the need for a line zero crossing compensating resistor to VREF from IAC that UC3854 designs require. The maximum current at high line into IAC should be limited to 250 µA for best performance.

Therefore, if $V_{VAC(max)}$ = 270 V,

$$R_{IAC} = \frac{270 \times 1.414}{250\mu A} = 1.53M\Omega \tag{2}$$

The $V_{RMS}$ pin linear operating range is improved with the UC3854A/B as well. The input range for VRMS extends from 0 V to 5.5 V. Since the UC3854A squaring circuit employs an analog multiplier, rather than a linear approximation, accuracy is improved, and discontinuities are eliminated. The external divider network connected to VRMS should produce 1.5 V at low line (85 VAC). This puts 4.77 V on VRMS at high line (270 VAC) which is well within its operating range.

The voltage amplifier output forms the third input to the multiplier and is internally clamped to 6.0 V. This eliminated an external zener clamp often used in UC3854 designs. The offset voltage at this input to the multiplier has been raised on the UC3854A/B to 1.5 V.

The multiplier output pin, which is also common to the current amplifier non-inverting input, has a –0.3 V to 5.0 V output range, compared to the –0.3 V to 2.5 V range of the UC3854. This improvement allows the UC3854A/B to be used in applications where the current sense signal amplitude is very large.

### Voltage Amplifier

The UC3854A/B voltage amplifier design is essentially similar to the UC3854 with two exceptions. The first is with the internal connection. The lower voltage reduces the amount of charge on the compensation capacitors, which provides improved recovery form large signal events, such as line dropouts, or power interruption. It also minimizes the dc current flowing through the feedback. The output of the voltage amplifier is also changed. In addition to a 6.0-V temperature compensated clamp, the output short circuit current has been lowered to 2 mA typical, and an active pull down has replaced the passive pull down of the UC3854.

### Current Amplifier

The current amplifier for an average current PFC controller needs a low offset voltage in order to minimize ac line current distortion. With this in mind, the UC3854A/B current amplifier has improved the input offset voltage from ±4 mV to 0 V to ±3 mV. The negative offset of the UC3854A/B assures that the PWM circuit will not drive the MOSFET is the current command is zero (both current amplifier inputs zero.) Previous designs required an external offset cancellation network to implement this key feature. The bandwidth of the current amplifier has been improved as well to 5 MHz typical. While this is not generally an issue at 50 Hz or 60 Hz inputs, it is essential for 400 Hz input avionics applications.

### Miscellaneous

Several other important enhancements have been implemented in the UC3854A/B. $AV_{CC}$ supply voltage clamp at 20 V allows the controller to be current fed if desired. The lower startup supply current (250 μA typical), substantially reduces the power requirements of an offline startup resistor. The 10.5 V/10 V UVLO option (UC3854B) enables the controller to be powered off of an auxiliary 12-V supply.

The VREF GOOD comparator assures that the MOSFET driver output remains low if the supply of the 7.5 V reference are not yet up. This improvement eliminates the need for external Schottky diodes on the PKLMT and Mult Out pins that some UC3854 designs require. The propagation delay of the disable feature has been improved to 300 ns typical. This delay was proportional to the size of the VREF capacitor on the UC3854, and is typically several orders of magnitude slower.

## TYPICAL CHARACTERISTICS

GATE DRIVE TIMING
vs
LOAD CAPACITANCE

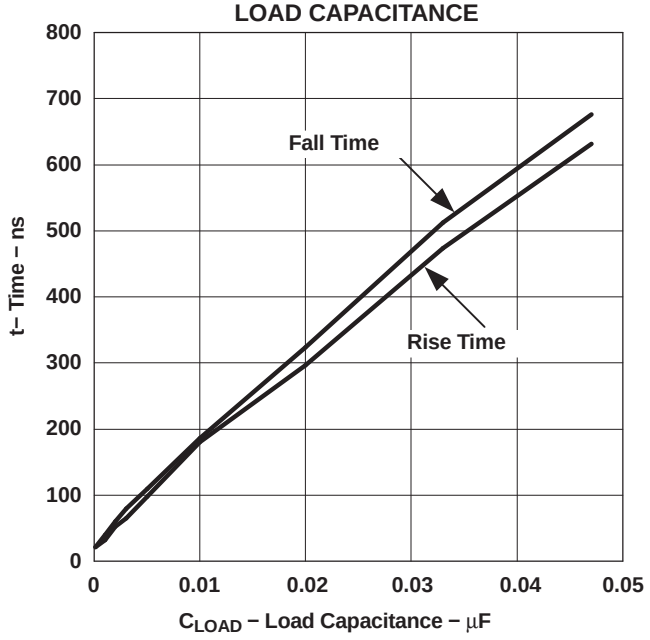



Figure 1.

GATE DRIVE MAXIMUM DUTY CYCLE
vs
OSCILLATOR CHARGING RESISTANCE

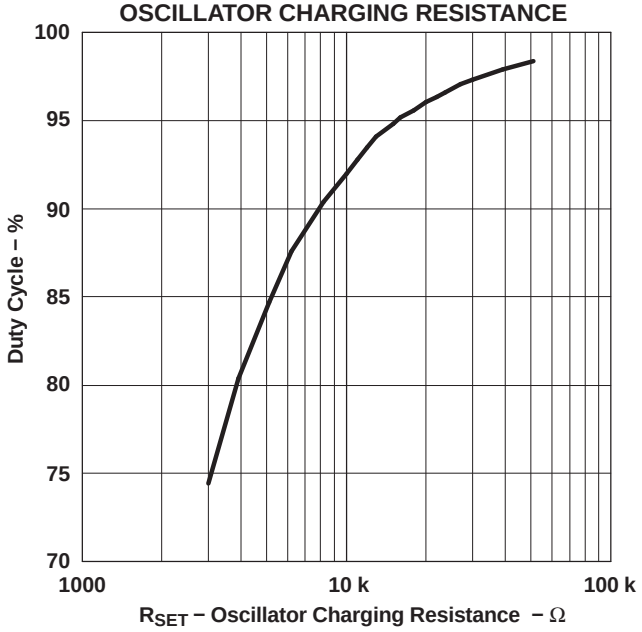



Figure 2.

MULTIPLIER GAIN CONSTANT
vs
SUPPLY CURRENT

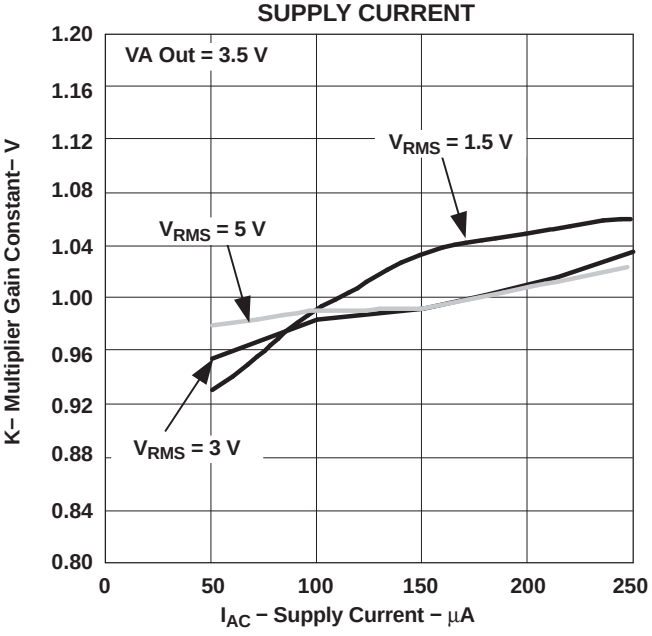



Figure 3.

MULTIPLIER GAIN CONSTANT
vs
SUPPLY CURRENT

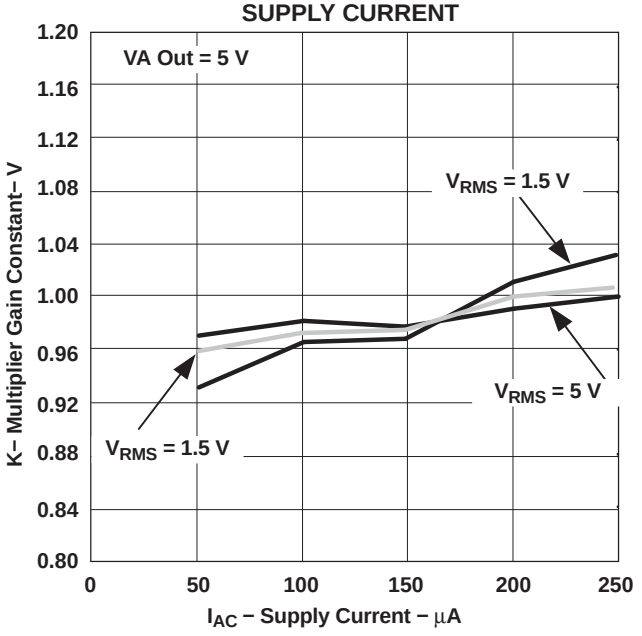



Figure 4.

## TYPICAL CHARACTERISTICS (continued)

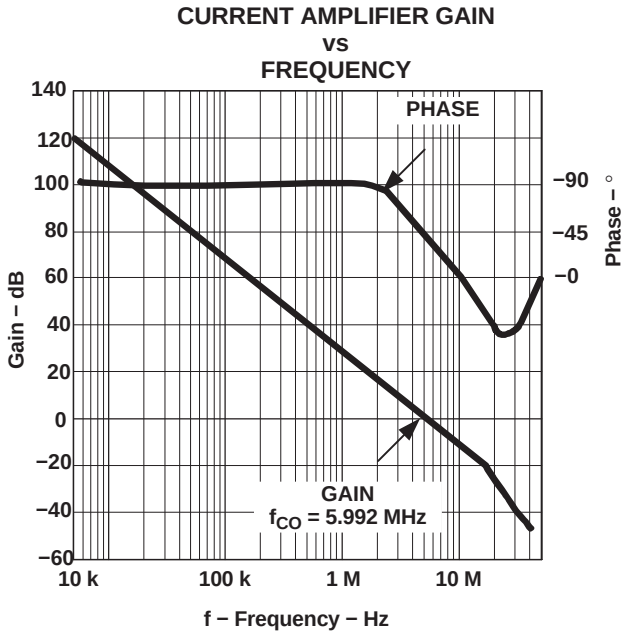



Figure 5.

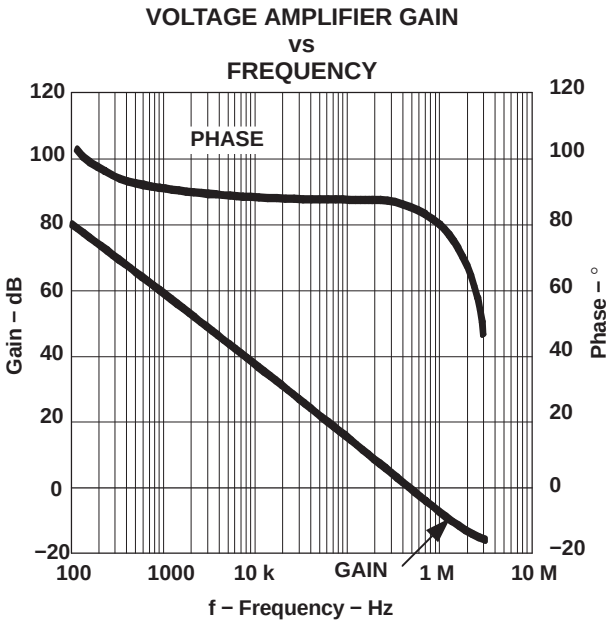



Figure 6.

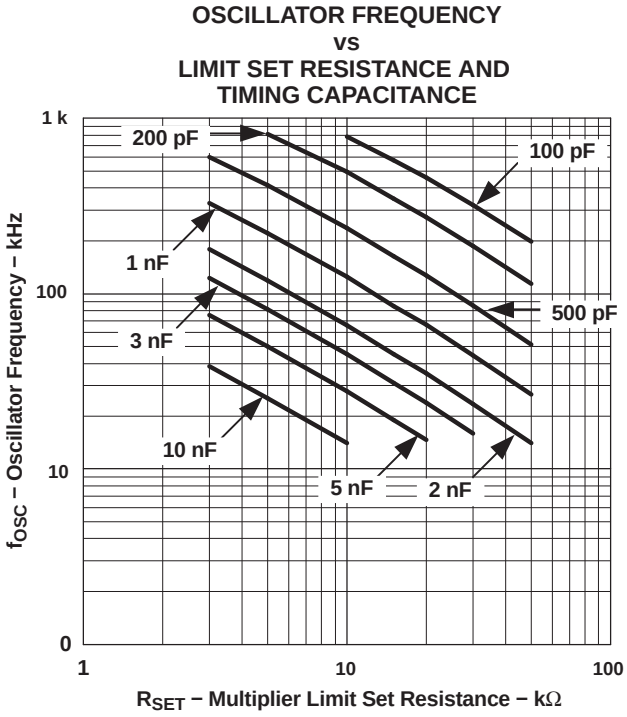



Figure 7.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 5962-9326102MEA | ACTIVE | CDIP | J | 16 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9326102MEA UC1854BJ/883B | Samples |
| UC1854BJ | ACTIVE | CDIP | J | 16 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | UC1854BJ | Samples |
| UC1854BJ883B | ACTIVE | CDIP | J | 16 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9326102MEA UC1854BJ/883B | Samples |
| UC2854ADW | ACTIVE | SOIC | DW | 16 | 40 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | UC2854ADW | Samples |
| UC2854ADWTR | ACTIVE | SOIC | DW | 16 | 2000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | UC2854ADW | Samples |
| UC2854AN | ACTIVE | PDIP | N | 16 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | -40 to 85 | UC2854AN | Samples |
| UC2854ANG4 | ACTIVE | PDIP | N | 16 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | -40 to 85 | UC2854AN | Samples |
| UC2854BDW | ACTIVE | SOIC | DW | 16 | 40 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | UC2854BDW | Samples |
| UC2854BDWG4 | ACTIVE | SOIC | DW | 16 | 40 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | UC2854BDW | Samples |
| UC2854BDWTR | ACTIVE | SOIC | DW | 16 | 2000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | UC2854BDW | Samples |
| UC2854BDWTRG4 | ACTIVE | SOIC | DW | 16 | 2000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | UC2854BDW | Samples |
| UC2854BN | ACTIVE | PDIP | N | 16 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | -40 to 85 | UC2854BN | Samples |
| UC2854J | ACTIVE | CDIP | J | 16 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -40 to 85 | UC2854J | Samples |
| UC3854ADW | ACTIVE | SOIC | DW | 16 | 40 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | 0 to 70 | UC3854ADW | Samples |
| UC3854ADWG4 | ACTIVE | SOIC | DW | 16 | 40 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | 0 to 70 | UC3854ADW | Samples |
| UC3854ADWTR | ACTIVE | SOIC | DW | 16 | 2000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | 0 to 70 | UC3854ADW | Samples |
| UC3854ADWTRG4 | ACTIVE | SOIC | DW | 16 | 2000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | 0 to 70 | UC3854ADW | Samples |
| UC3854AN | ACTIVE | PDIP | N | 16 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | 0 to 70 | UC3854AN | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| UC3854ANG4 | ACTIVE | PDIP | N | 16 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | 0 to 70 | UC3854AN | Samples |
| UC3854BDW | ACTIVE | SOIC | DW | 16 | 40 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | 0 to 70 | UC3854BDW | Samples |
| UC3854BDWG4 | ACTIVE | SOIC | DW | 16 | 40 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | 0 to 70 | UC3854BDW | Samples |
| UC3854BDWTR | ACTIVE | SOIC | DW | 16 | 2000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | 0 to 70 | UC3854BDW | Samples |
| UC3854BDWTRG4 | ACTIVE | SOIC | DW | 16 | 2000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | 0 to 70 | UC3854BDW | Samples |
| UC3854BN | ACTIVE | PDIP | N | 16 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | 0 to 70 | UC3854BN | Samples |
| UC3854BNG4 | ACTIVE | PDIP | N | 16 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | 0 to 70 | UC3854BN | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**OTHER QUALIFIED VERSIONS OF UC1854B, UC2854B, UC2854M, UC3854B :**

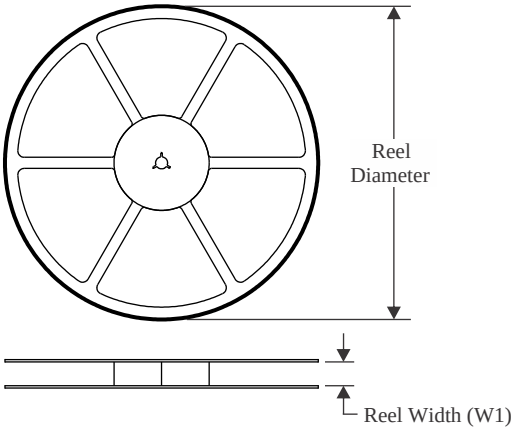
- Catalog : UC3854B, UC2854
- Enhanced Product : UC2854B-EP
- Military : UC2854BM, UC1854B

NOTE: Qualified Version Definitions:

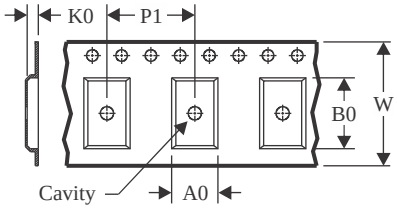
- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

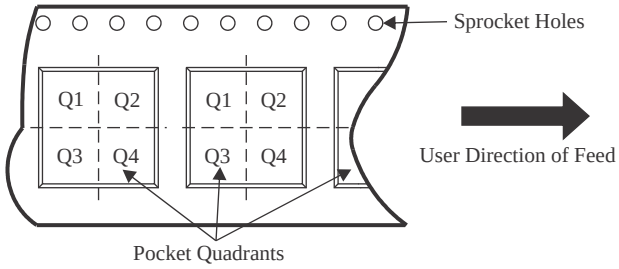



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

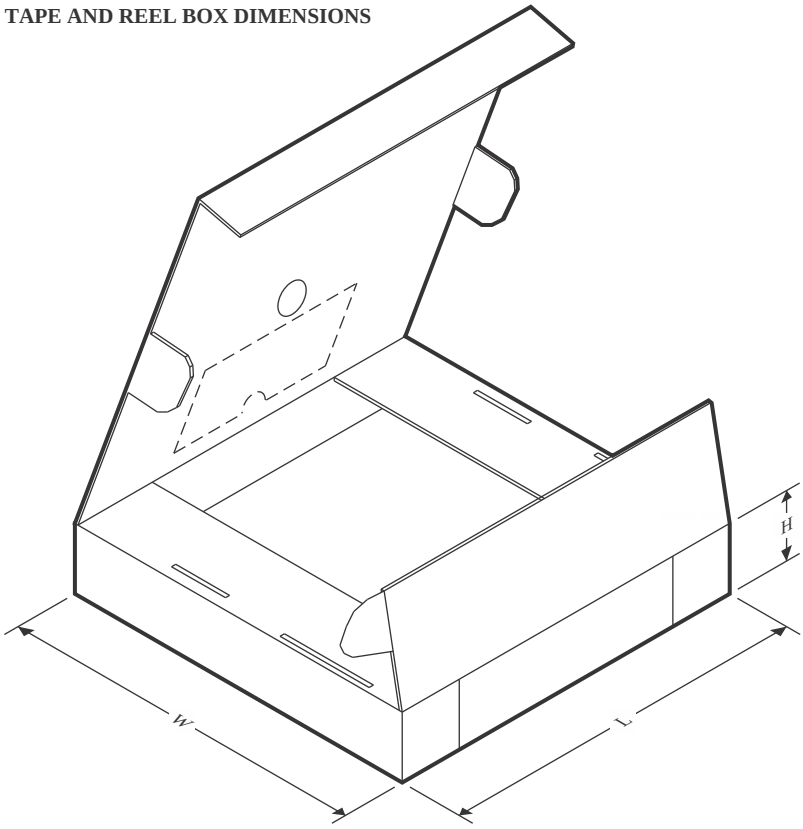
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| UC2854ADWTR | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |
| UC2854BDWTR | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |
| UC3854ADWTR | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |
| UC3854BDWTR | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |

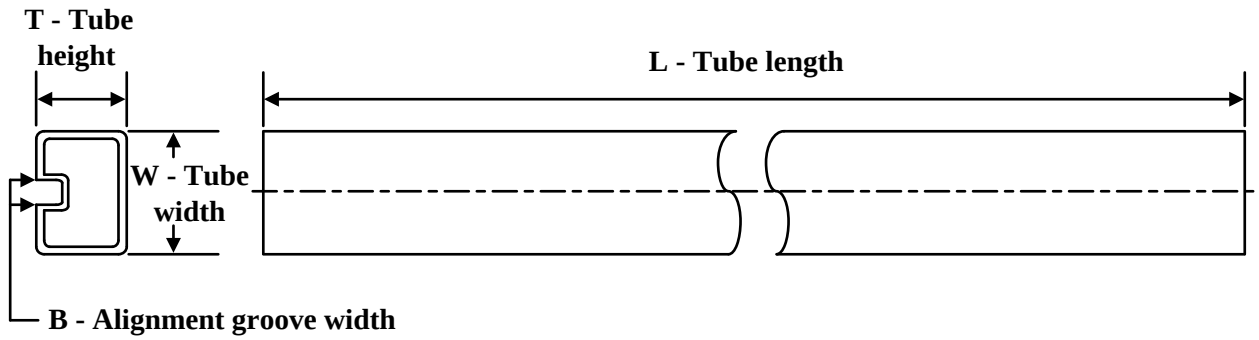
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| UC2854ADWTR | SOIC | DW | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| UC2854BDWTR | SOIC | DW | 16 | 2000 | 367.0 | 367.0 | 38.0 |
| UC3854ADWTR | SOIC | DW | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| UC3854BDWTR | SOIC | DW | 16 | 2000 | 356.0 | 356.0 | 35.0 |

## TUBE

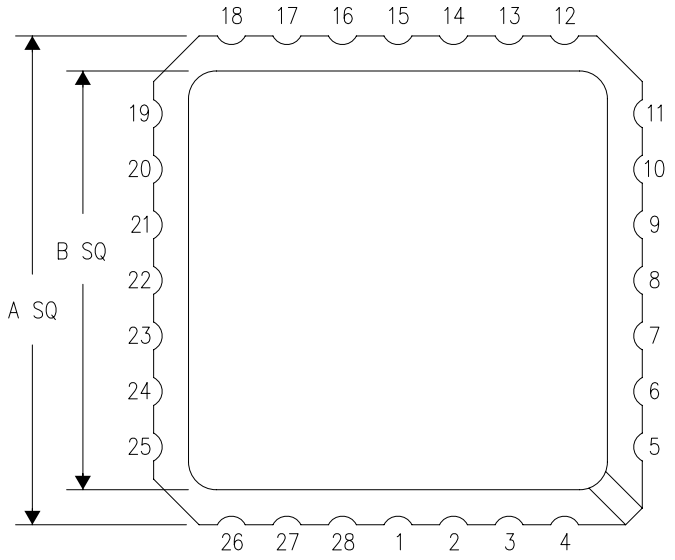



*All dimensions are nominal

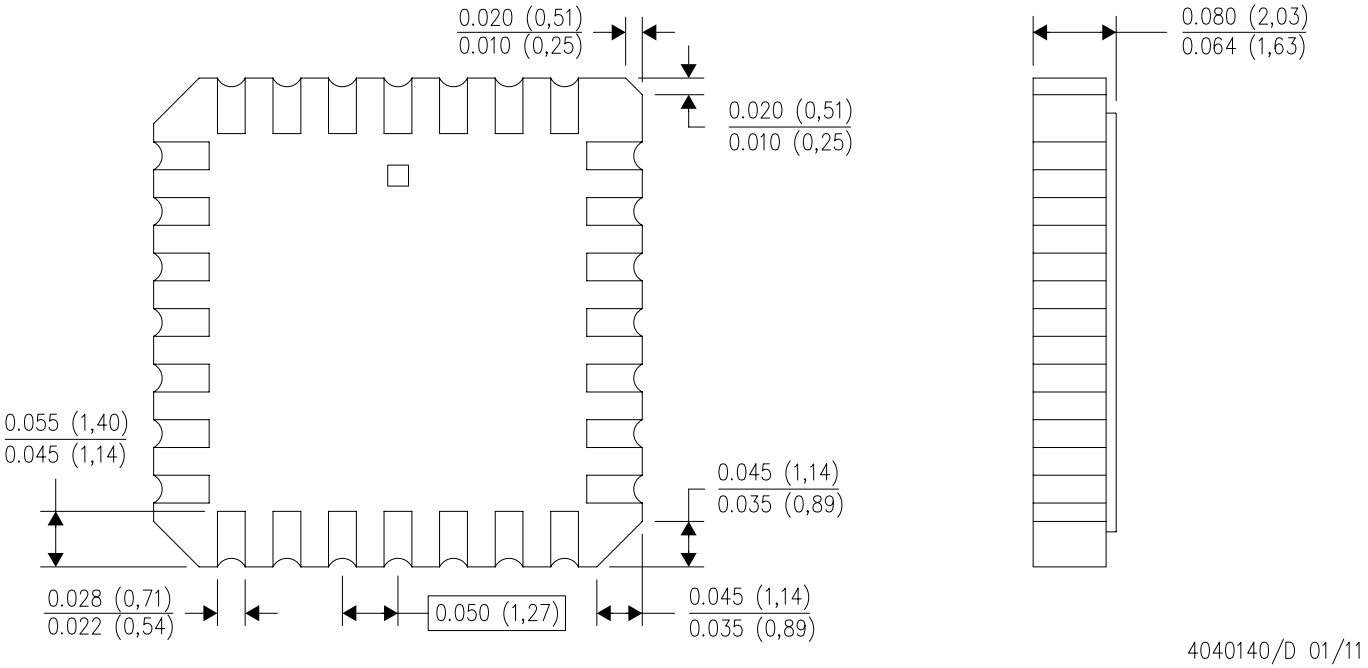
| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| UC2854ADW | DW | SOIC | 16 | 40 | 507 | 12.83 | 5080 | 6.6 |
| UC2854AN | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| UC2854ANG4 | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| UC2854BDW | DW | SOIC | 16 | 40 | 507 | 12.83 | 5080 | 6.6 |
| UC2854BDWG4 | DW | SOIC | 16 | 40 | 507 | 12.83 | 5080 | 6.6 |
| UC2854BN | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| UC3854ADW | DW | SOIC | 16 | 40 | 507 | 12.83 | 5080 | 6.6 |
| UC3854ADWG4 | DW | SOIC | 16 | 40 | 507 | 12.83 | 5080 | 6.6 |
| UC3854AN | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| UC3854ANG4 | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| UC3854BDW | DW | SOIC | 16 | 40 | 507 | 12.83 | 5080 | 6.6 |
| UC3854BDWG4 | DW | SOIC | 16 | 40 | 507 | 12.83 | 5080 | 6.6 |
| UC3854BN | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| UC3854BNG4 | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |

FK (S–CQCC–N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN




| NO. OF TERMINALS ** | A | | B | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| 20 | 0.342 (8,69) | 0.358 (9,09) | 0.307 (7,80) | 0.358 (9,09) |
| 28 | 0.442 (11,23) | 0.458 (11,63) | 0.406 (10,31) | 0.458 (11,63) |
| 44 | 0.640 (16,26) | 0.660 (16,76) | 0.495 (12,58) | 0.560 (14,22) |
| 52 | 0.740 (18,78) | 0.761 (19,32) | 0.495 (12,58) | 0.560 (14,22) |
| 68 | 0.938 (23,83) | 0.962 (24,43) | 0.850 (21,6) | 0.858 (21,8) |
| 84 | 1.141 (28,99) | 1.165 (29,59) | 1.047 (26,6) | 1.063 (27,0) |



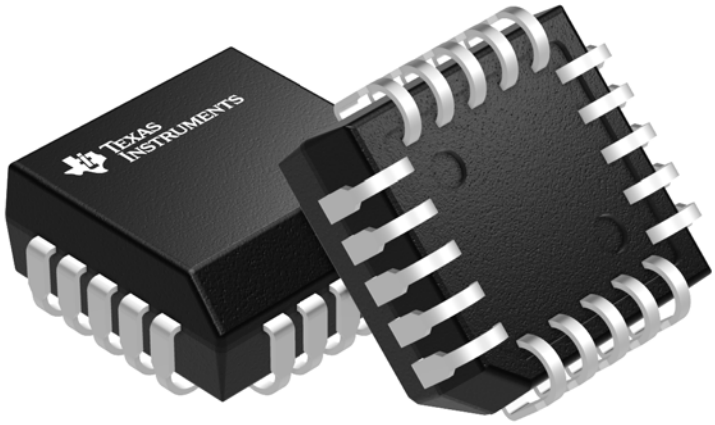

4040140/D 01/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS–004

# GENERIC PACKAGE VIEW

## FN 20 PLCC - 4.57 mm max height

PLASTIC CHIP CARRIER




Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

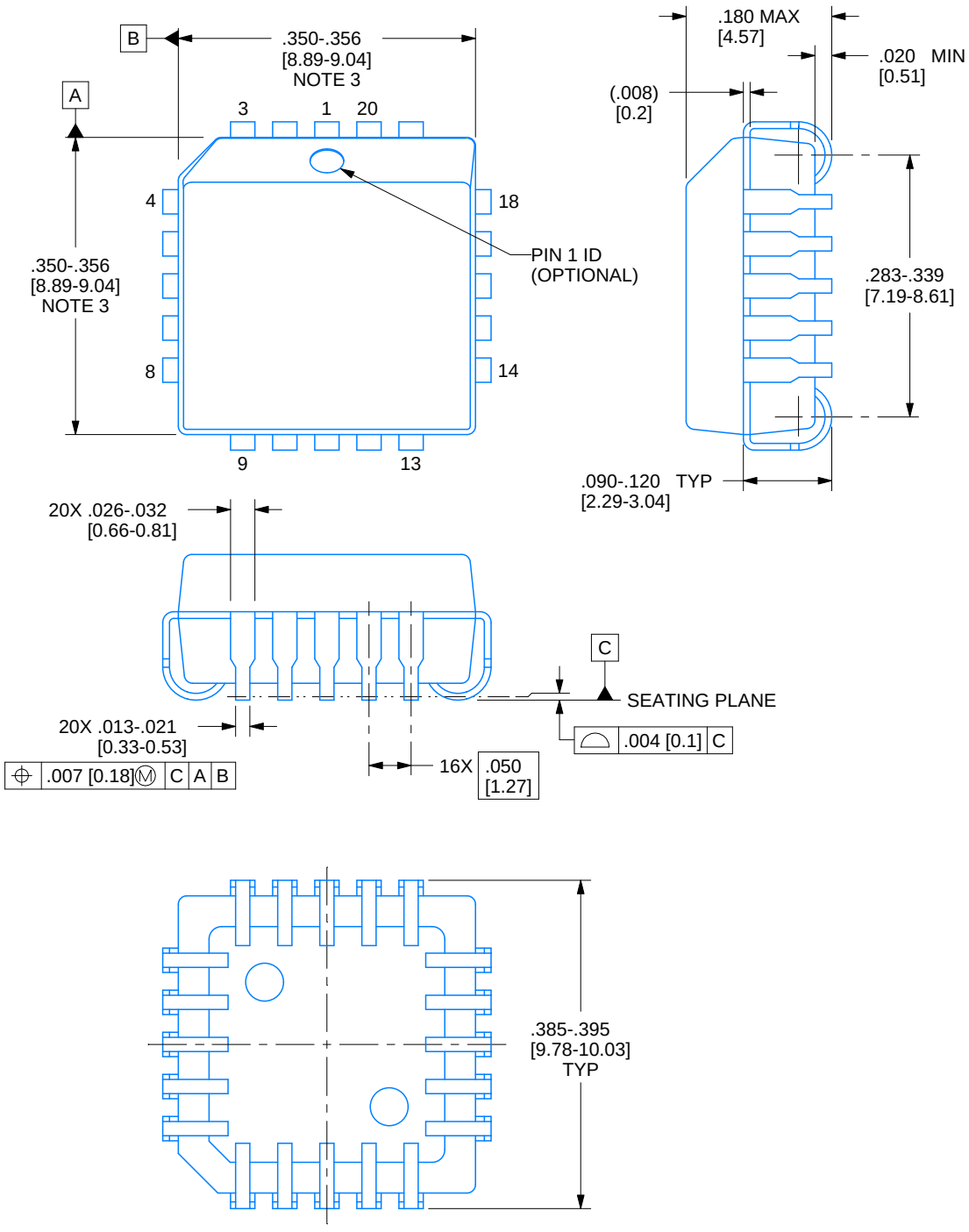
4040005-2/C

# PACKAGE OUTLINE

## FN0020A

## PLCC - 4.57 mm max height

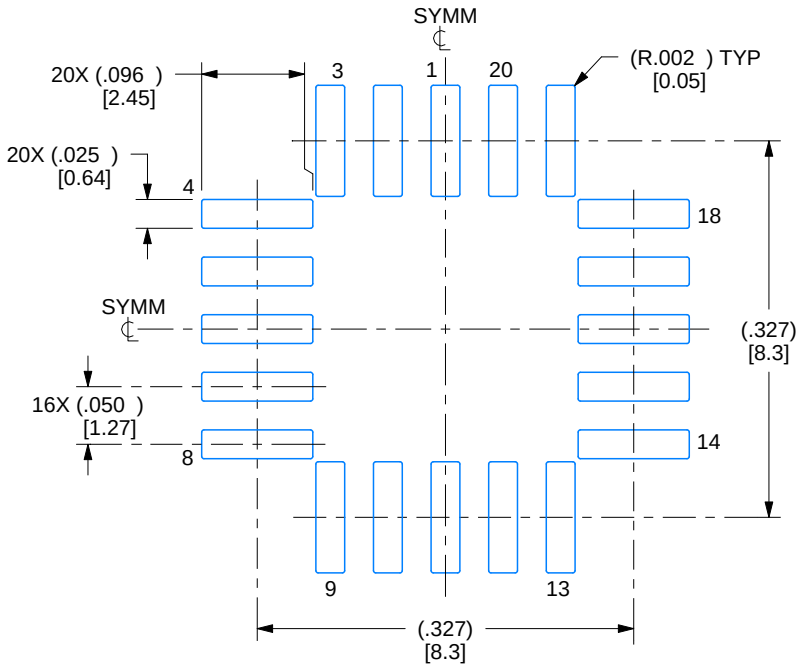
PLASTIC CHIP CARRIER



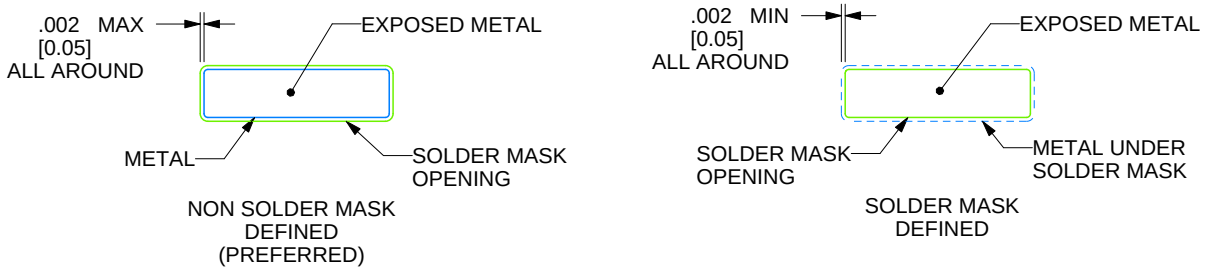

4215152/B 04/2017

NOTES:

1. All linear dimensions are in inches. Any dimensions in brackets are in millimeters. Any dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Dimension does not include mold protrusion. Maximum allowable mold protrusion .01 in [0.25 mm] per side.
4. Reference JEDEC registration MS-018.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X

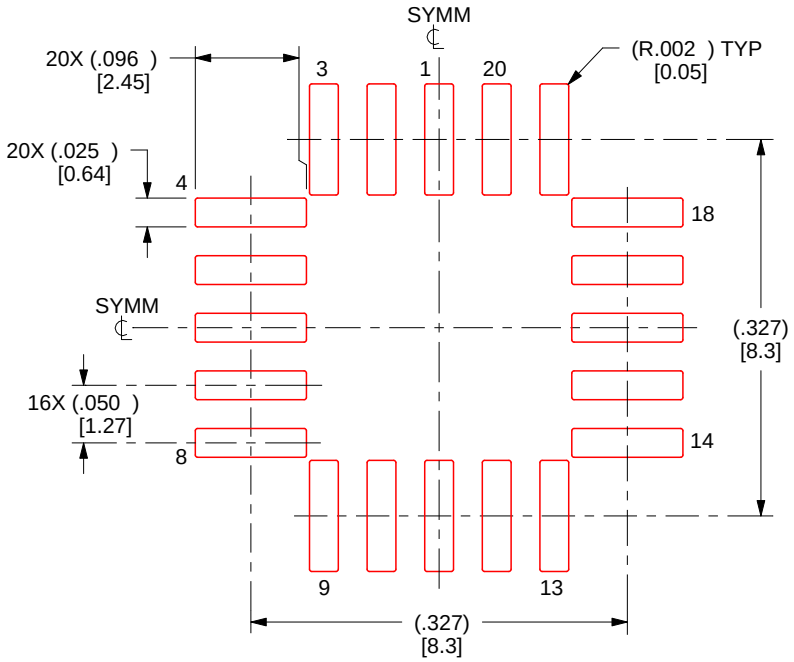



SOLDER MASK DETAILS

4215152/B 04/2017

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4215152/B 04/2017

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

# GENERIC PACKAGE VIEW

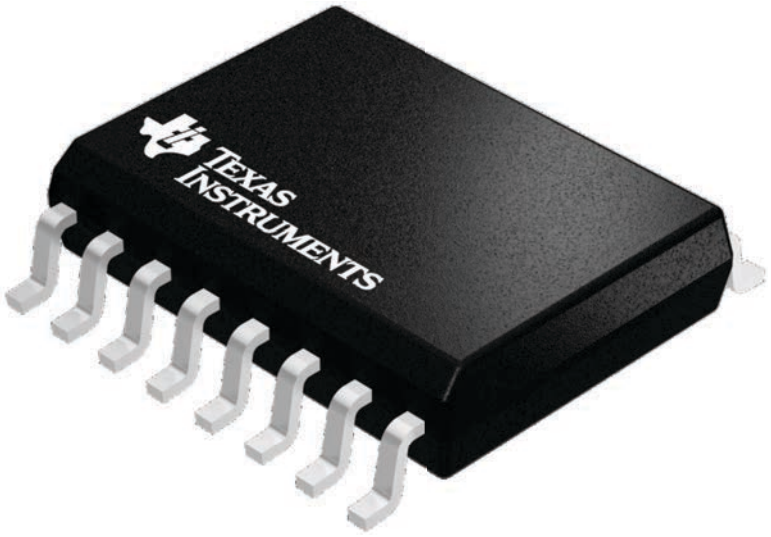
## DW 16

## SOIC - 2.65 mm max height

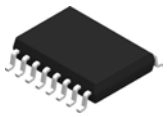
**7.5 x 10.3, 1.27 mm pitch**

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.




4224780/A

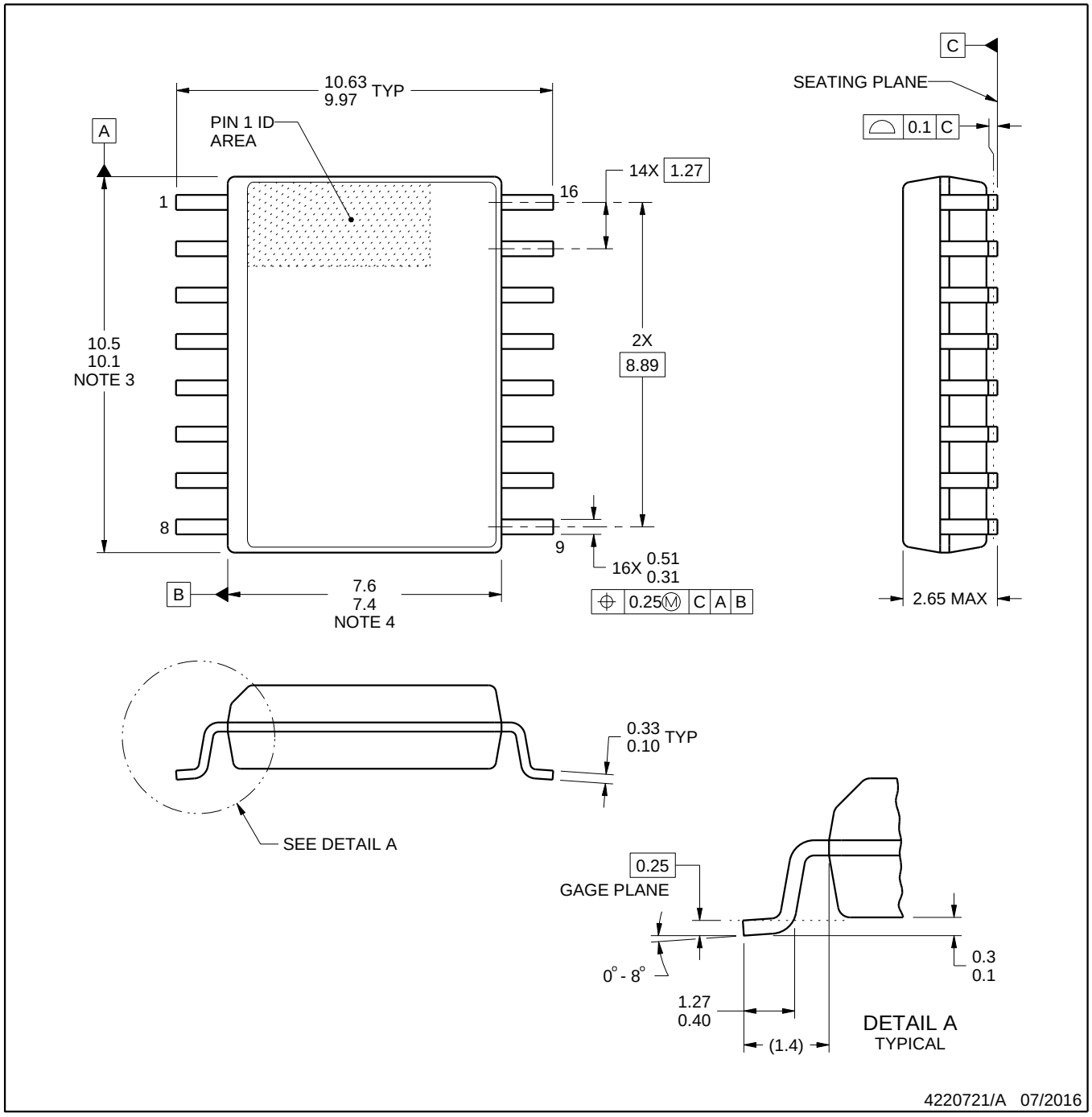


# PACKAGE OUTLINE

## DW0016A

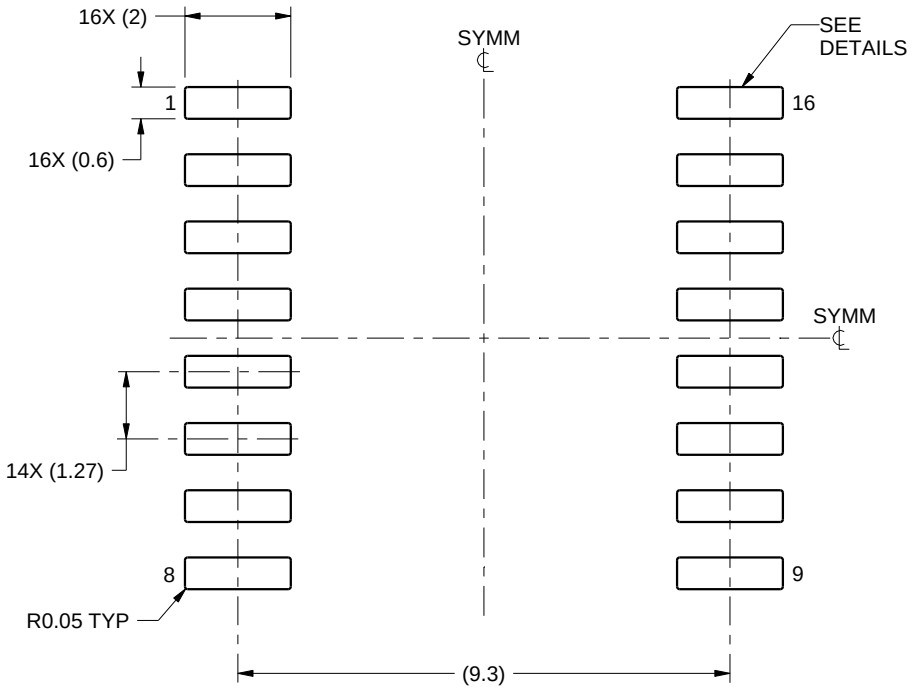
## SOIC - 2.65 mm max height

SOIC

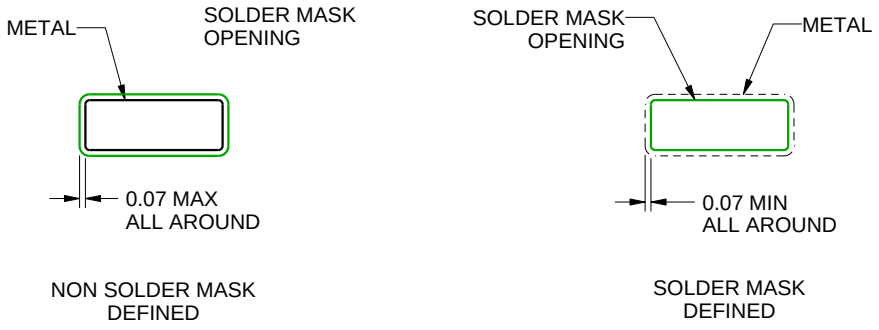



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.




LAND PATTERN EXAMPLE
SCALE:7X

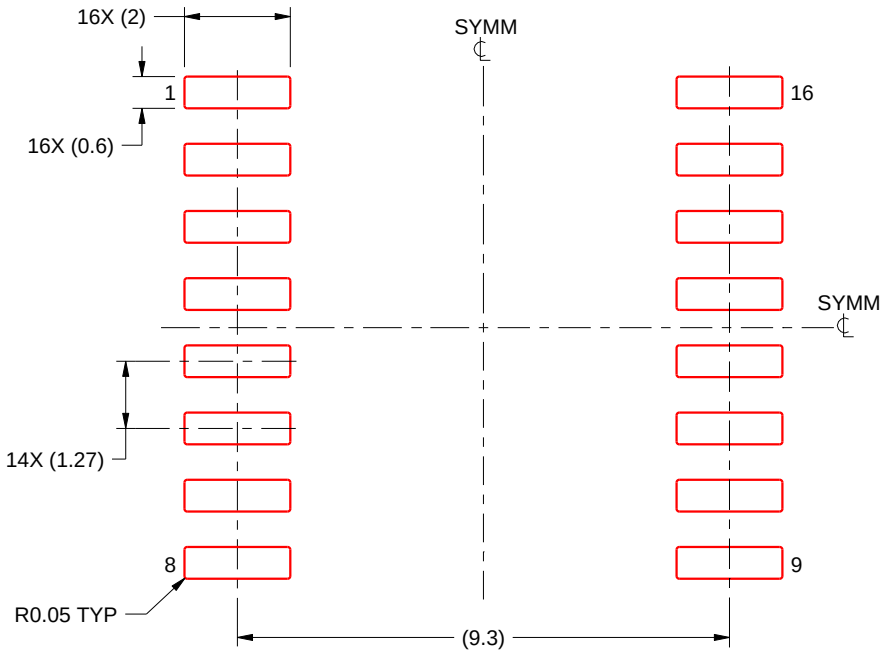



SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220721/A 07/2016

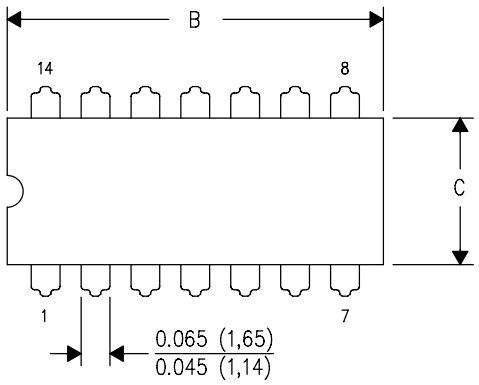
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

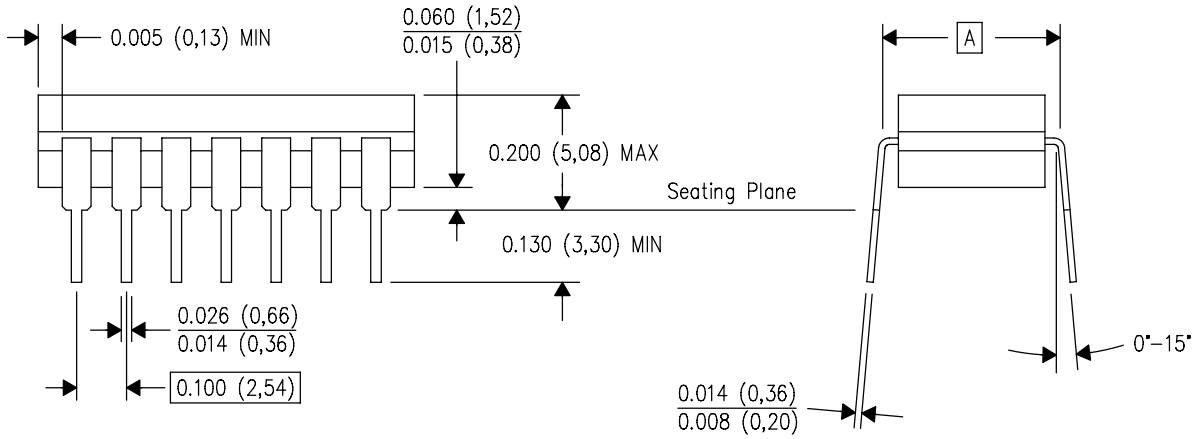
J (R–GDIP–T**)

14 LEADS SHOWN

# CERAMIC DUAL IN–LINE PACKAGE




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



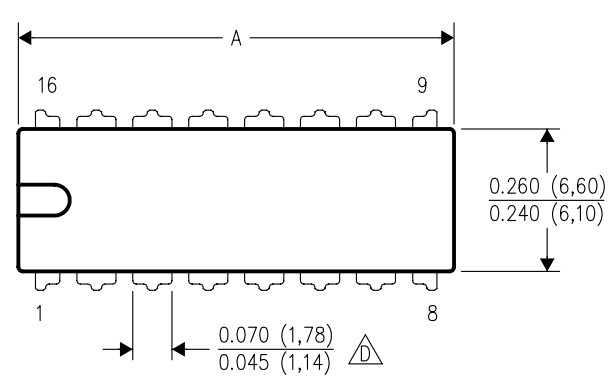

4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

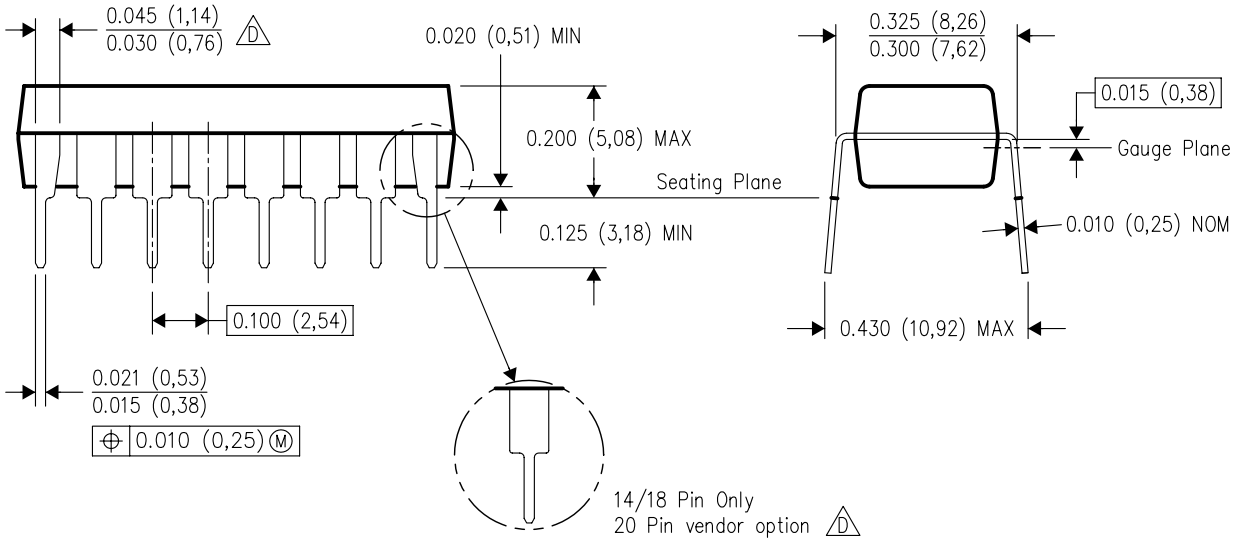
## N (R–PDIP–T**)

## PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |




4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

# IMPORTANT NOTICE AND DISCLAIMER

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