



Embedded Storage

FerriSSD[®] Module

PCIe/NVMe SSD Ax Series

Datasheet

(Simplified Edition)

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Revision History

| Revision | Date | Description |
|----------|--------------|-------------------------------------|
| 0.1 | Dec 4, 2018 | Released the simplified edition |
| 0.2 | Feb 19, 2019 | Updated the Endurance section (5.2) |

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1. Overview

1.1 Product Description

Silicon Motion leverages the industry leading technologies and experiences to introduce the fully integrated FerriSSD® module in small and light form factors for enterprise/industrial applications such as node/blade server, navigation, thin-client, as well as a variety of embedded applications. The FerriSSD module series are designed optimally for a wide range of embedded applications that requires the highest reliability with blazing fast read/write performance.

FerriSSD can provide a shock-protected and quiet-operating environment for mobile storage requirements. The new generation PCIe NVMe FerriSSD Ax series with 3D NAND Flash equips Silicon Motion's advanced technologies including IntelligentScan, DataRefresh, high bandwidth LDPC code correction with proprietary RAID engine, and end-to-end data path protection — enabling unsurpassed data integrity in a non-volatile storage device designed for mission critical application.

With high reliability, industry-leading performance and programmable firmware, the FerriSSD is the ultimate storage solution for today's fast-moving consumer electronics and industrial level applications. The FerriSSD module is available in various densities for different storage needs.

1.2 Key Features

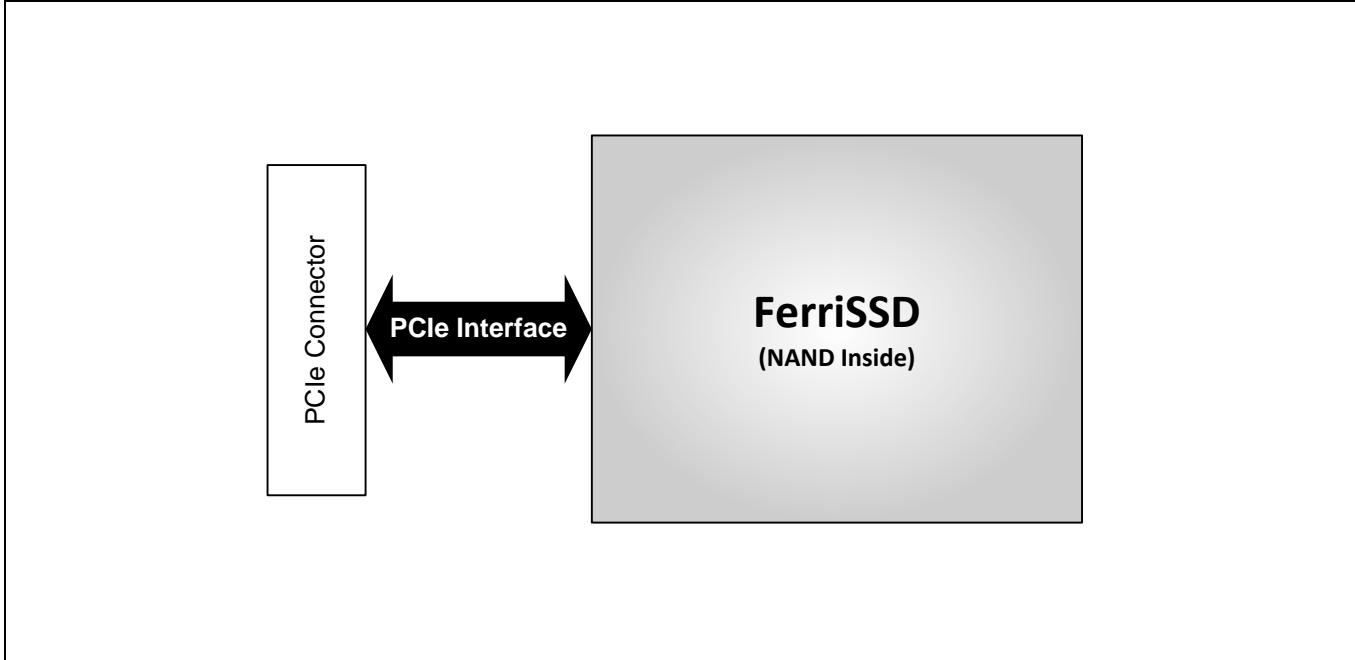
- Host Interface
 - PCIe Gen 3 x4/x2 Lane
 - Compliant with PCI Express 3.1
 - NVMe 1.3 register interface and command set
- Dual ARM Cortex R5 CPU
- Data Reliability
 - Performance-optimized LDPC engine provides maximum error correction capability
 - End-to-end data path protection with CRC parity
 - Embedded DRAM for added data protection capability (option)
 - SRAM and DRAM ECC error handling and prevention on major memory buffers
 - RAID engine provides multi-page protection for NAND flash data
- Robust Data Protection
 - Advanced system level protection against unstable power supply
 - RAID engine offers additional level of data protection
 - StaticDataRefresh and EarlyRetirement technologies ensure data integrity and prevent read disturbance
 - Early weak block retirement feature
 - PowerShield and DataPhoenix technologies support power-down data protection and recovery

- Data Integrity and Security
 - Built-in AES-128/256 Encryption
 - TCG Opal 2.0 compliant
 - Built-in hardware SHA256 and True Random Number Generator (TRNG)
- Available Capacity
 - Supports unformatted capacity up to 256GB¹
- Small Form Factor
 - FerriSSD M.2: M.2 SSD (type 2242 and type 2280)
- Easy-to-Use
 - The Plug & Play device only requires format/disk prior to use
- Temperature Range
 - Operating Temperature: 0°C ~ 70°C
 - Extended Operating Temperature: -40°C ~ +85°C
 - Non-Operating and Storage Temperature: -55°C ~ +85°C

¹ 512GB will be available by Q1 2019.

1.3 Block Diagram

Figure 1: FerriSSD Block Diagram



2. Product Specifications

2.1 Host Interface

The FerriSSD complies to the following industrial standards:

- PCIe Gen 3 Interface x4/x2 Lane
- Compliant with PCIe Express 3.1
- NVMe 1.3 register interface and command set

2.2 Supply Voltage

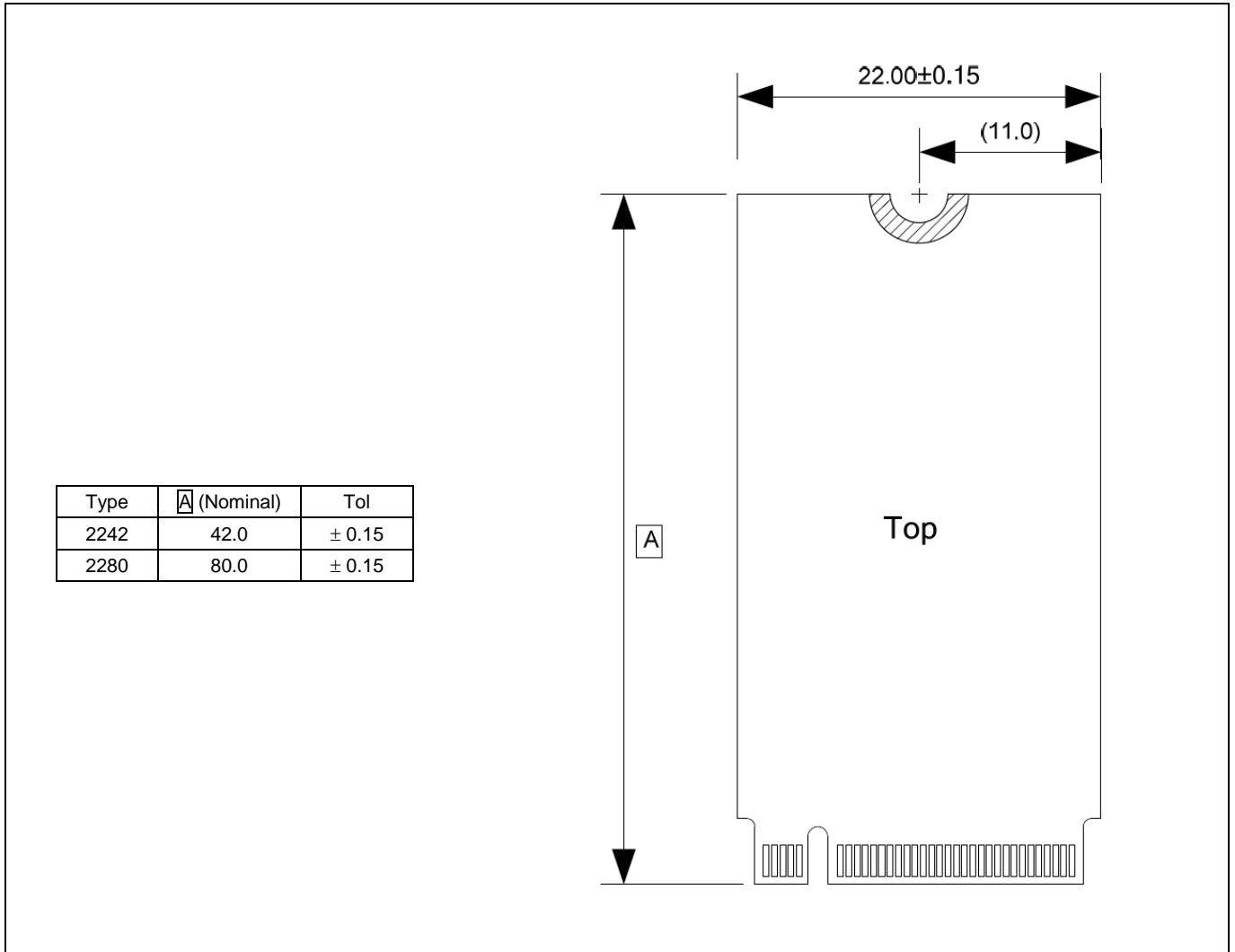
Table 1: FerriSSD Module Supply Voltage

| Model | Min | Typ | Max | Unit |
|--------------|-------|-----|-------|------|
| FerriSSD M.2 | 3.135 | 3.3 | 3.465 | V |

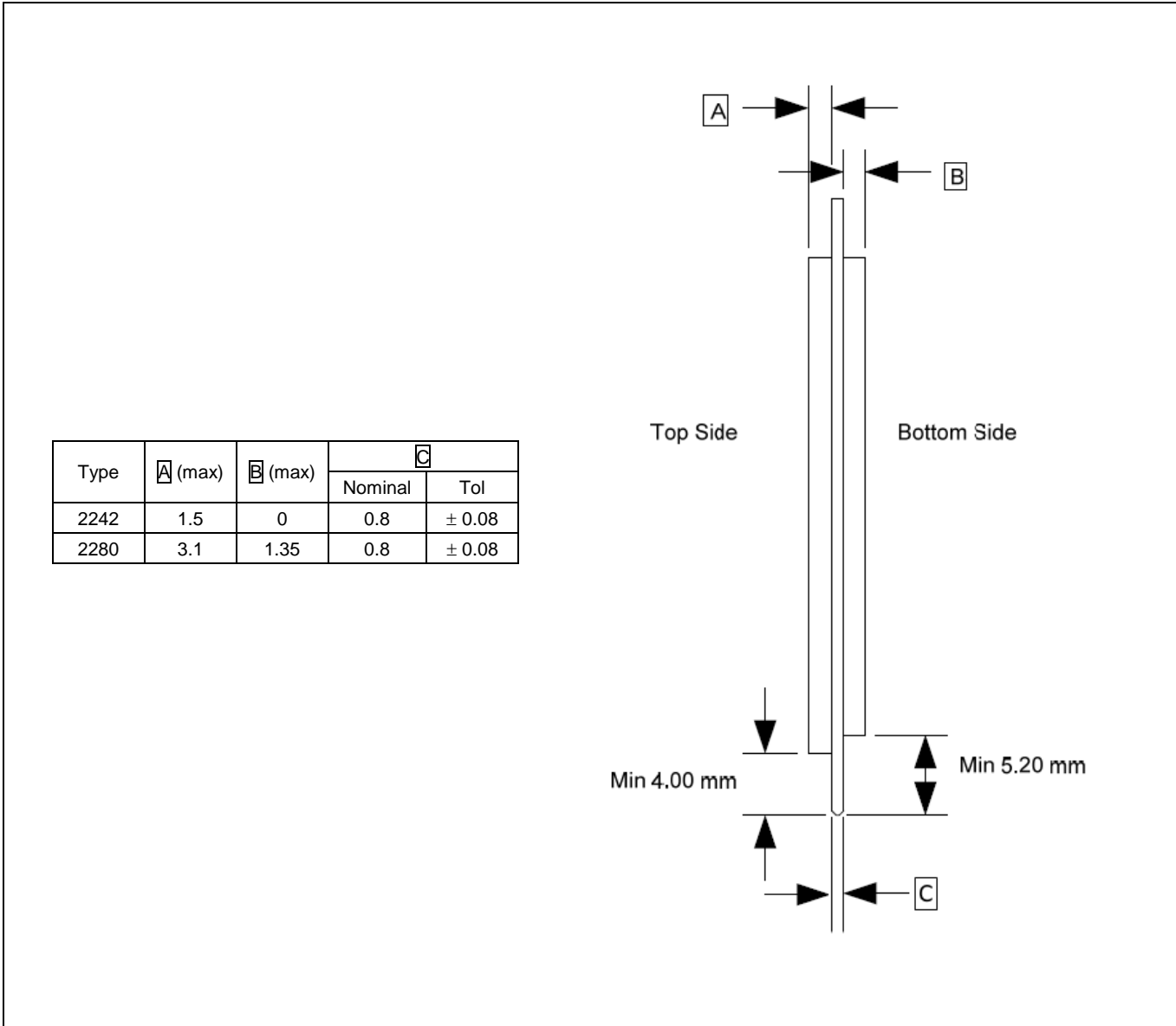
3. Physical Specifications

3.1 FerriSSD M.2

3.1.1 FerriSSD M.2 Mechanical Drawing



Unit: mm



| Type | A (max) | B (max) | C | |
|------|---------|---------|---------|--------|
| | | | Nominal | Tol |
| 2242 | 1.5 | 0 | 0.8 | ± 0.08 |
| 2280 | 3.1 | 1.35 | 0.8 | ± 0.08 |

Unit: mm

3.1.2 FerriSSD M.2 Pin Assignments

| Pin | Type | Description |
|-----|-----------|---------------------------------------|
| 1 | GND | Ground |
| 2 | 3.3V | Supply pin, 3.3V |
| 3 | GND | Ground |
| 4 | 3.3V | Supply pin, 3.3V |
| 5 | PETn3 | PCIe Transmit data differential pair |
| 6 | NC | No connect |
| 7 | PETp3 | PCIe Transmit data differential pair |
| 8 | PLP_INIT# | Power Loss Protection Initial signal |
| 9 | GND | Ground |
| 10 | LED_1# | Device Activity Signal |
| 11 | PERn3 | PCIe Received data differential pair |
| 12 | 3.3V | Supply pin, 3.3V |
| 13 | PERp3 | PCIe Received data differential pair |
| 14 | 3.3V | Supply pin, 3.3V |
| 15 | GND | Ground |
| 16 | 3.3V | Supply pin, 3.3V |
| 17 | PETn2 | PCIe Transmit data differential pair |
| 18 | 3.3V | Supply pin, 3.3V |
| 19 | PETp2 | PCIe Transmit data differential pair |
| 20 | NC | No connect |
| 21 | GND | Ground |
| 22 | NC | No connect |
| 23 | PERn2 | PCIe Received data differential pair |
| 24 | NC | No connect |
| 25 | PERp2 | PCIe Received data differential pair |
| 26 | NC | No connect |
| 27 | GND | Ground |
| 28 | NC | No connect |
| 29 | PETn1 | PCIe Transmit data differential pair |
| 30 | PLP_FBCK# | Power Loss Protection Feedback signal |
| 31 | PETp1 | PCIe Transmit data differential pair |
| 32 | NC | No connect |
| 33 | GND | Ground |
| 34 | NC | No connect |
| 35 | PERn1 | PCIe Received data differential pair |

| Pin | Type | Description |
|-----|------------------------|---|
| 36 | NC | No connect |
| 37 | PERp1 | PCIe Received data differential pair |
| 38 | NC | No connect |
| 39 | GND | Ground |
| 40 | SMB_CLK | SMBus Clock |
| 41 | PETn0 | PCIe Transmit data differential pair |
| 42 | SMB_DATA | SMBus Data |
| 43 | PETp0 | PCIe Transmit data differential pair |
| 44 | ALERT# | Alert notification |
| 45 | GND | Ground |
| 46 | NC | No connect |
| 47 | PERn0 | PCIe Received data differential pair |
| 48 | NC | No connect |
| 49 | PERp0 | PCIe Received data differential pair |
| 50 | PERST# | PE-Reset is a functional reset to the card |
| 51 | GND | Ground |
| 52 | CLKREQ# | Clock Request is a reference clock request signal |
| 53 | REFCLKn | PCIe Reference Clock signals (100 MHz) |
| 54 | PEWAKE# | No connect |
| 55 | REFCLKp | PCIe Reference Clock signals (100 MHz) |
| 56 | Reserved for MFG_DATA | No connect |
| 57 | GND | Ground |
| 58 | Reserved for MFG_CLOCK | No connect |
| 59 | (removed for key) | Mechanical notch M |
| 60 | (removed for key) | Mechanical notch M |
| 61 | (removed for key) | Mechanical notch M |
| 62 | (removed for key) | Mechanical notch M |
| 63 | (removed for key) | Mechanical notch M |
| 64 | (removed for key) | Mechanical notch M |
| 65 | (removed for key) | Mechanical notch M |
| 66 | (removed for key) | Mechanical notch M |
| 67 | NC | No connect |
| 68 | SUSCLK | No connect |
| 69 | PEDET(NC-PCIE) | No connect |
| 70 | 3.3V | Supply pin, 3.3V |
| 71 | GND | Ground |
| 72 | 3.3V | Supply pin, 3.3V |

| Pin | Type | Description |
|-----|------|------------------|
| 73 | GND | Ground |
| 74 | 3.3V | Supply pin, 3.3V |
| 75 | GND | Ground |

4. Environmental Conditions

4.1 Temperature

Table 2: Temperature Related Specifications

| Parameter | Specifications |
|------------------------------|----------------|
| C-temp Operating Temperature | 0°C ~ 70°C |
| I-temp Operating Temperature | -40°C ~ +85°C |
| Non-Operating Temperature | -55°C to +85°C |
| Storage Temperature | -55°C to +85°C |

4.2 Humidity

Table 3: Humidity Related Specifications

| Parameter | Specifications |
|------------------------------------|------------------------------|
| Operating Humidity | |
| Humidity | 5% to 95% (Non condensation) |
| Non-Operating Humidity | |
| Humidity (Non condensation) | 5% to 95% |
| Maximum Relative Humidity Gradient | 20% per hour |

4.3 RoHS

Compliant to RoHS (Restriction of Hazardous Substances Directive) 2.0.

5. Reliability

5.1 Reliability Specifications

Table 4: Reliability Specifications

| Type | UBER | MTBF |
|------------|---------------------------------------|-----------------|
| 3D TLC | 1 sector in 10^{16} bits read, max. | 1,200,000 hours |
| 3D SLCmode | 1 sector in 10^{17} bits read, max. | 2,000,000 hours |

Notes:

1. UBER: Uncorrectable bit error rate will not exceed one sector in the specified number of bits read. Refer to the JEDEC SSD specifications for detailed definition.
2. Mean Time Between Failure is estimated based on FIT value. FIT (Failure in Time) test is conducted at SMI internal test lab with SMI RDT (Reliability Demonstration Test).

5.2 Endurance

Please contact SMI representative for the endurance information.

5.3 Preventive Maintenance

No preventive maintenance is required.

6. Ordering Information

6.1 Product Coding Rule

Table 5: Product Code Definitions

| Example: MD 6 8 9 G X C H AE 3 | |
|--------------------------------|--|
| M | Ferri Module |
| D | Form Factor <ul style="list-style-type: none"> • D = FerriSSD M.2 (22 x 42 mm) • E = FerriSSD M.2 (22 x 80 mm) |
| 6 | Ferri Family |
| 8 | Type / Interface <ul style="list-style-type: none"> • 8 = PCIe/NVMe |
| 9 | <ul style="list-style-type: none"> • 9 = Embedded DRAM • 1 = DRAM-Less |
| G | BGA SSD Type <ul style="list-style-type: none"> • G = Default BGA • H = High-performance BGA |
| X | Operating Temperature <ul style="list-style-type: none"> • X = 0°C ~ 70°C (C-temp) • E = -40°C ~ +85°C (I-temp) |
| C | Density <ul style="list-style-type: none"> • A = 16GB • B = 32GB • C = 64GB • D = 128GB • E = 256GB |
| H | PCB Revision H = Revision H |
| AE | BGA SSD Product Revision |
| 3 | BOM Version 3 = Default setting 6 = With DataFlush option |

Note: See the Selection Guide for detailed information on available product ordering numbers.