Product Document

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AS1363

1A Low Dropout Linear Voltage Regulator

1 General Description

The AS1363 is a low-dropout linear regulator that operates from a +2.0V to +5.5V supply and delivers a guaranteed 500mA load current with low 150mV dropout.

The device is available in two versions (see Table 1). One version has a high-accuracy output with a preset voltage (1.2V, 1.5V, 1.8V, 3.0V, 3.3V, or 4.5V). This voltage is internally trimmed and also offers a Bypass pin. With a capacitor connected to this Bypass pin, the PSRR and the Noise performance is improved.

At the other version the output voltage is user-adjustable (1.2V to 5.3V) and offers an SET pin for setting the output voltage.

Table 1. Standard Products

Model	Output Type	BYP	SET
AS1363-AD	Adjustable	No	Yes
AS1363-_ _	Fixed	Yes	No

A low supply current (65µA typ.) at maximum load is making the device ideal for portable battery-operated equipment.

Other features are included such as an active-low open-drain reset output that indicates when the output is out of regulation, a low-current (30nA typ.) shutdown mode, an integrated short-circuit and a thermal shutdown protection.

When in shutdown, a 5kΩ (typ) discharge path is connected between the output pin and ground. The AS1363 is available in a 6-pin SOT23 package.

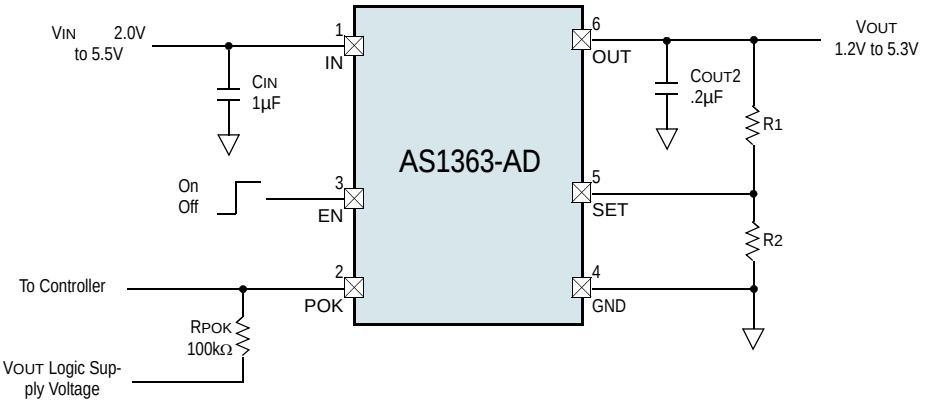
2 Key Features

- Guaranteed Output Current: 500mA
- Low Dropout: 150mV @ 500mA
- 2.0V to 5.5V Input Voltage
- Fixed Output Voltage: 1.2V to 5.0V
- User-Adjustable Output Voltage: 1.2V to 5.3V
- Power OK Output
- Low Quiescent Current: 40µA
- Low Shutdown Current: 30nA
- Thermal Overload Protection
- Output Current Limit
- Output discharge path during shutdown
- 6-pin SOT23 Package

3 Applications

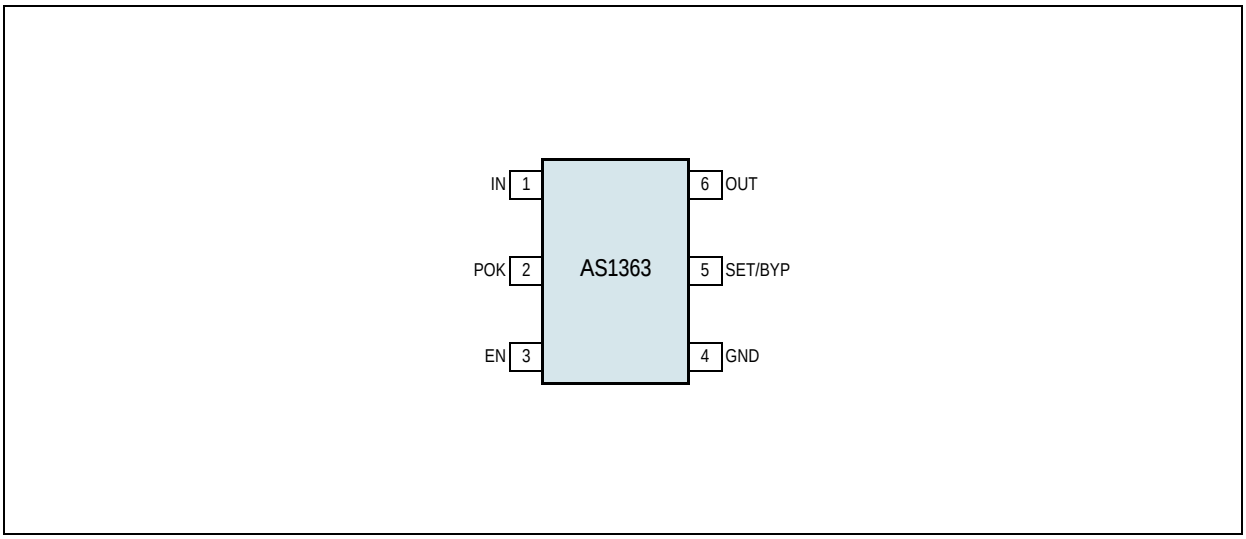
The device is ideal for laptops, PDAs, portable audio devices, mobile phones, cordless phones, and any other battery-operated portable device.

Figure 1. AS1363 - Typical Application Circuit



4 Pin Assignments

Figure 2. Pin Assignments (Top View)



4.1 Pin Descriptions

Table 2. Pin Descriptions

Pin Number	Pin Name	Description
1	IN	**+2.0V to +5.5V Supply Voltage.** Bypass this pin with a 1µF capacitor to GND (see Package Drawings and Markings on page 16).
2	POK	**Open-Drain POK Output.** POK remains low while VOUT is below the POK threshold. Connect a 100kΩ pull-up resistor from this pin to OUT to obtain an output voltage (see Figure on page 1).
3	EN	**Active-High Enable Input.** A logic low reduces supply current below 30nA. In shutdown mode, the POK output is low, and OUT is high impedance. Connect this pin to IN for normal operation.
4	GND	**Ground**
5	SET	**Voltage-Setting Input.** Connect to GND for preset output or Connect to a resistive voltage-divider between OUT and GND to set the output voltage between 1.2V and 5.3V (see Figure on page 1).
	BYP	**Bypass Pin.** Connect a 10nF capacitor from this pin to VOUT to improve PSRR and noise performance (see Figure 16 on page 9).
6	OUT	**Output.** Sources up to 500mA. Bypass this pin with a 2.2µF low-ESR capacitor to GND (see Figure on page 1). **Note:** For output voltages below 2V a 4.7µF capacitor should be used.

5 Absolute Maximum Ratings

Stresses beyond those listed in Table 3 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Electrical Characteristics on page 4 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3. Absolute Maximum Ratings

Parameter	Min	Max	Units	Comments
IN, POK, EN, SET/BYP to GND	-0.3	+6	V	
OUT to GND	-0.3	VIN +0.3	V	
Output Short-Circuit Duration		1	min	
Continuous Power Dissipation		800	mW	TAMB = +70ºC; derate 10mW/ºC above +70ºC
Operating Temperature Range	-40	+85	ºC	
Storage Temperature Range	-65	+150	ºC	
Junction Temperature		+125	ºC	
Package Body Temperature		+260	ºC	The reflow peak soldering temperature (body temperature) specified is in accordance with *IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices".* The lead finish for Pb-free leaded packages is matte tin (100% Sn).
Moisture Sensitive Level	1			Represents an unlimited floor life time

6 Electrical Characteristics

All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

V_{IN} = $V_{OUT(NOM)}$ + 500mV or V_{IN} = +2.0V (whichever is greater), C_{IN} = 1µF, C_{OUT} = 2.2µF, EN = IN, T_{AMB} = -40 to +85ºC (unless otherwise specified). Typical values are at T_{AMB} = +25ºC.

Table 4. Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IN}	Input Voltage		2.0		5.5	V
V_{POR}	Power On reset	Falling, 100mV hysteresis	1.78	1.87	1.96	V
	Output Voltage Accuracy (Preset Mode)	I_{OUT} = 100µA, T_{AMB} = +25ºC,	-0.75		+0.75	%
		I_{OUT} = 100mA	-1.5		+1.5	
		I_{OUT} = 1 to 500mA, V_{IN} > (V_{OUT} + 0.5V)[1]	-2		+2	
V_{OUT}	Adjustable Output Voltage Range		1.2		5.3	V
$V_{SET/BYP}$	SET/BYP Voltage Threshold (Adjustable Mode)	V_{IN} = 2.5V, I_{OUT} = 1mA, V_{OUT} set to 2.0V	1.17	1.20	1.23	V
I_{OUT}	Guaranteed Output Current (RMS)		500			mA
I_{LIMIT}	Short-Circuit Current Limit	V_{OUT} = 0V	0.55	0.8	1.2	A
	In-Regulation Current Limit	V_{OUT} > 96% of nominal value		0.8		A
	SET/BYP Threshold		50	100	150	mV
I_{SET}	SET/BYP Input Bias Current	$V_{SET/BYP}$ = 1.2V	-100		+100	nA
I_Q	Quiescent Current	I_{OUT} = 100µA		40	150	µA
		I_{OUT} = 500mA		65	200	
V_{IN} - V_{OUT}	Dropout Voltage [2]	I_{OUT} = 500mA, V_{OUT} = 2.5V		150	320	mV
ΔV_{LNR}	Line Regulation	V_{IN} from (V_{OUT} + 100mV) to 5.5V, I_{LOAD} = 5mA	-0.125		+0.125	%/V
ΔV_{LDR}	Load Regulation	I_{OUT} = 1 to 500mA	-0.001		+0.001	%/mA
PSRR	Ripple Rejection	f = 1kHz, I_{OUT} = 10mA, adjustable Output		65		dB
		f = 10kHz, I_{OUT} = 10mA, adjustable Output		70		
		f = 100kHz, I_{OUT} = 10mA, adjustable Output		60		
	Output Voltage Noise	10Hz to 100kHz, I_{OUT} = 10mA, adjustable Output		80		μV_{RMS}
		100Hz to 100kHz, I_{OUT} = 10mA, adjustable Output		65		
Shutdown						
I_{OFF}	Shutdown Supply Current	EN = GND, V_{IN} = 5.5V, T_{AMB} = 25°C		0.03	0.5	µA
		EN = GND, V_{IN} = 5.5V			15	
V_{IH}	EN Input Threshold	2.0V < V_{IN} < 5.5V	1.6			V
V_{IL}		2.0V < V_{IN} < 5.5V			0.6	V
I_{EN}	EN Input Bias Current	EN = IN or GND, T_{AMB} = +25ºC		1		nA
		T_{AMB} = +85ºC		5		

Table 4. Electrical Characteristics (Continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
POK Output						
V_{OL}	POK Output Low Voltage	POK sinking 1mA		0.05	0.25	V
	Operating Voltage Range for Valid POK Signal	POK sinking 100µA	1.1		5.5	V
	POK Output High leakage Current	POK = 5.5V, T_{AMB} = +25ºC		1		nA
		T_{AMB} = +85ºC		5		
	POK Threshold	Rising edge (referenced to $V_{OUT(NOM)}$)	90	94	98	%
Thermal Protection						
T_{SHDNN}	Thermal Shutdown Temperature			170		ºC
ΔT_{SHDNN}	Thermal Shutdown Hysteresis			20		ºC
C_{OUT}	Output Capacitor	Load Capacitor Range	1	2.2		µF
		Load Capacitor ESR			500	mΩ

1. Guaranteed by production test of load regulation and line regulation.
2. Dropout voltage is defined as V_{IN} - V_{OUT}, when V_{OUT} is 100mV below the value of V_{OUT} measured for V_{IN} = ($V_{OUT(NOM)}$ + 500mV). Since the minimum input voltage is 2.0V, this specification is only valid when $V_{OUT(NOM)}$ > 2.0V.

7 Typical Operating Characteristics

V_{IN} = $V_{OUT(NOM)}$ + 0.5V, C_{IN} = 1µF, C_{OUT} = 2.2µF, T_{AMB} = 25°C (unless otherwise specified).

Figure 3. V_{DROP} vs. I_{OUT};

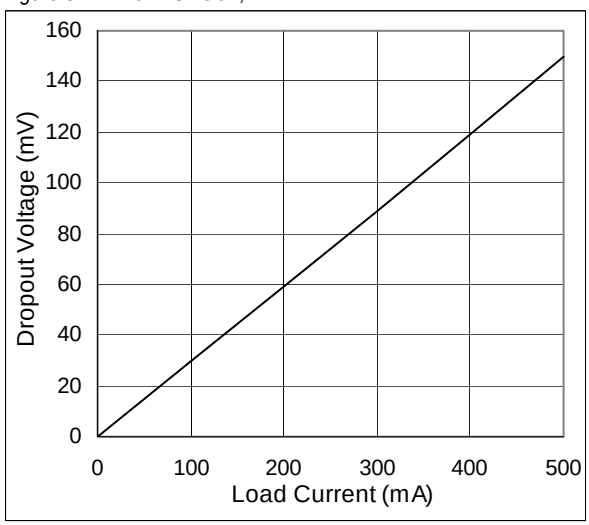


Figure 4. V_{OUT} vs. I_{OUT}; $V_{OUT(NOM)}$ = 2.5V

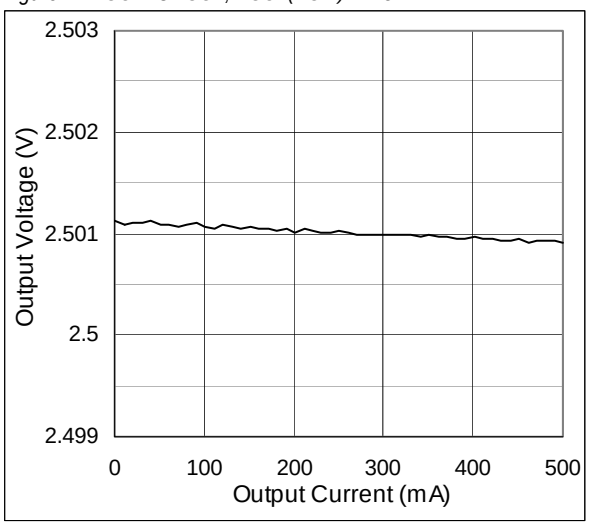


Figure 5. V_{OUT} vs. Temperature; $V_{OUT(NOM)}$ = 2.5V

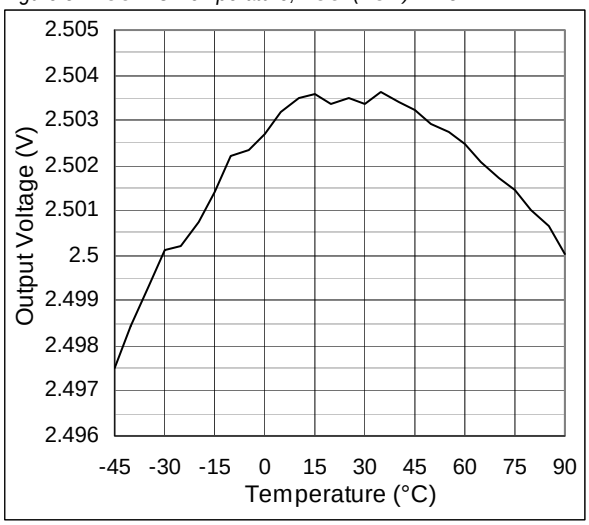


Figure 6. V_{OUT} vs. V_{IN}; $V_{OUT(NOM)}$ = 2.5V

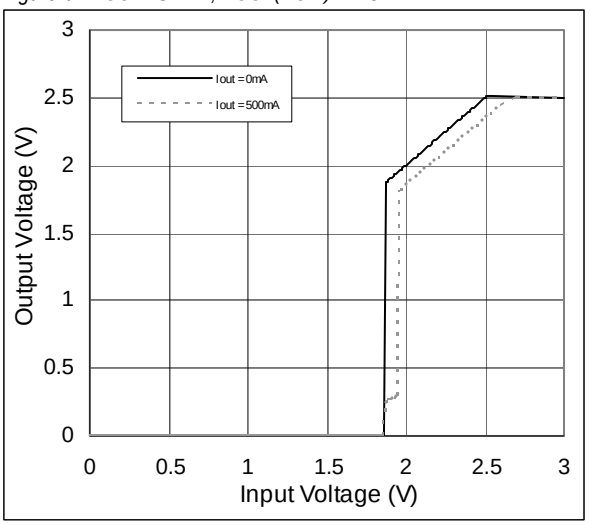


Figure 7. Quiescent Current vs. V_{IN}; no load

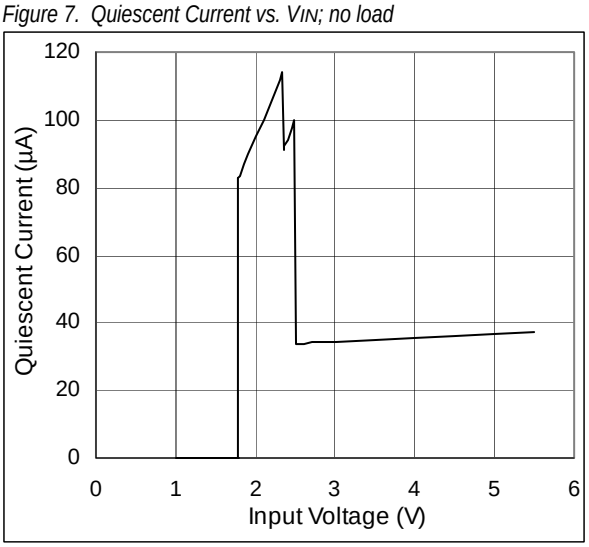


Figure 8. Quiescent Current vs. I_{OUT}; V_{IN} = 3.0V;

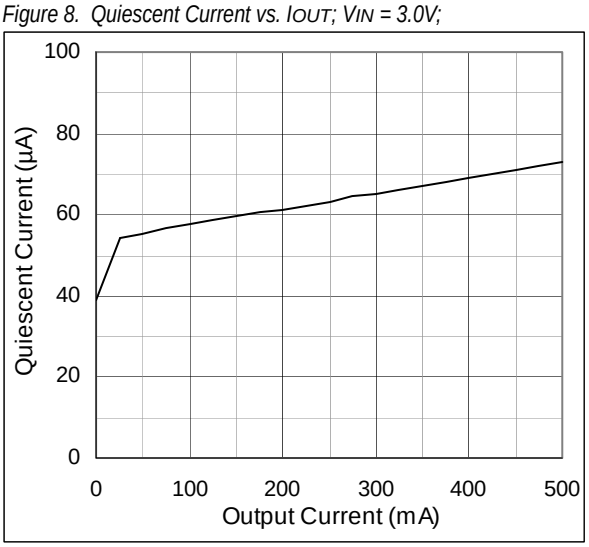


Figure 9. Quiescent Current vs. Temperature; VIN = 3.0V

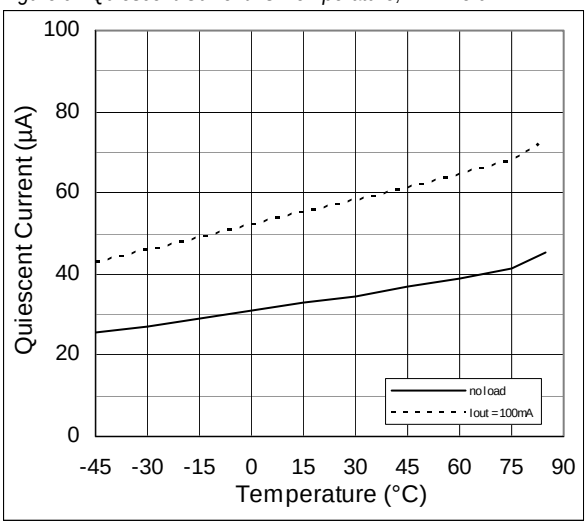


Figure 10. PSRR vs. Frequency; IOUT = 10mA, CIN = 68nF,

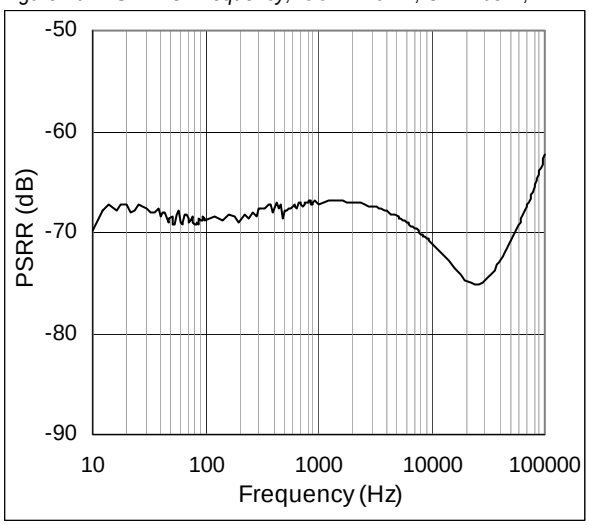


Figure 11. Line Transient Response; VIN = 3.0V to 3.5V, IOUT = 100mA

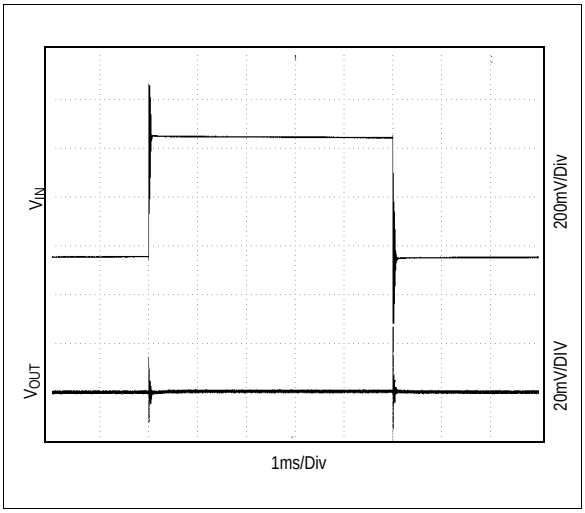


Figure 12. Load Transient Response; VIN = 3.0V, IOUT = 50mA to 250mA

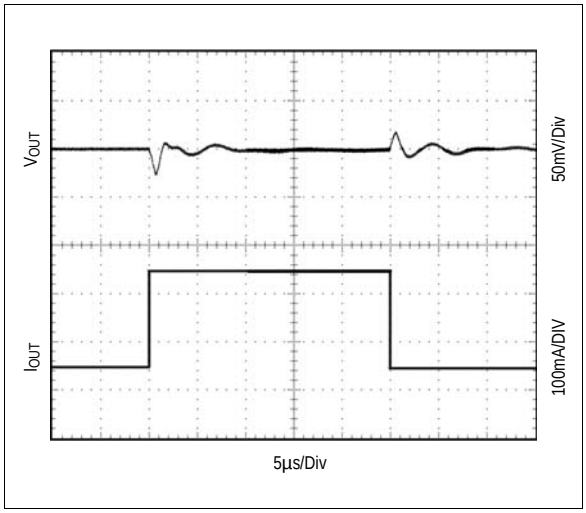


Figure 13. Startup; VIN = 3.0V, IOUT = 100mA

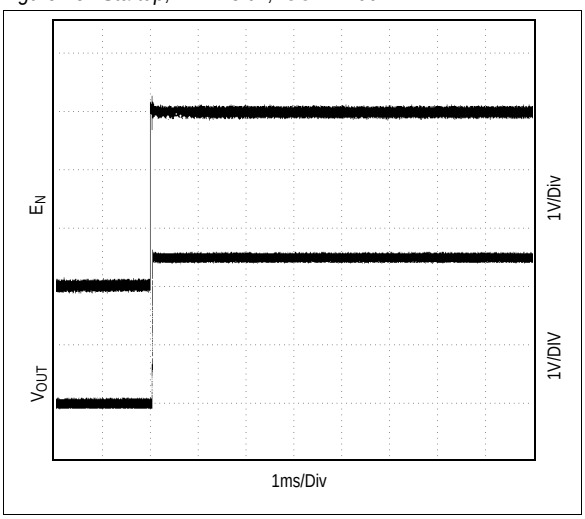
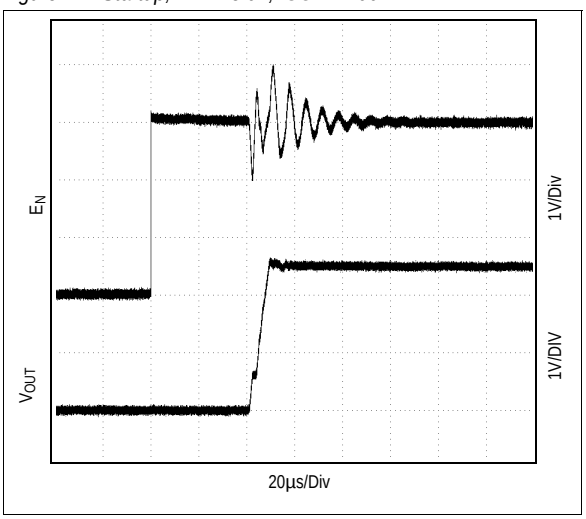


Figure 14. Startup; VIN = 3.0V, IOUT = 100mA



8 Detailed Description

The AS1363 is a low-dropout, low-quiescent-current linear regulator specifically designed for battery-powered devices. The regulator supplies loads of up to 500mA and can deliver a factory-preset output voltage or user-adjustable output voltage.

Figure 15. Block Diagram

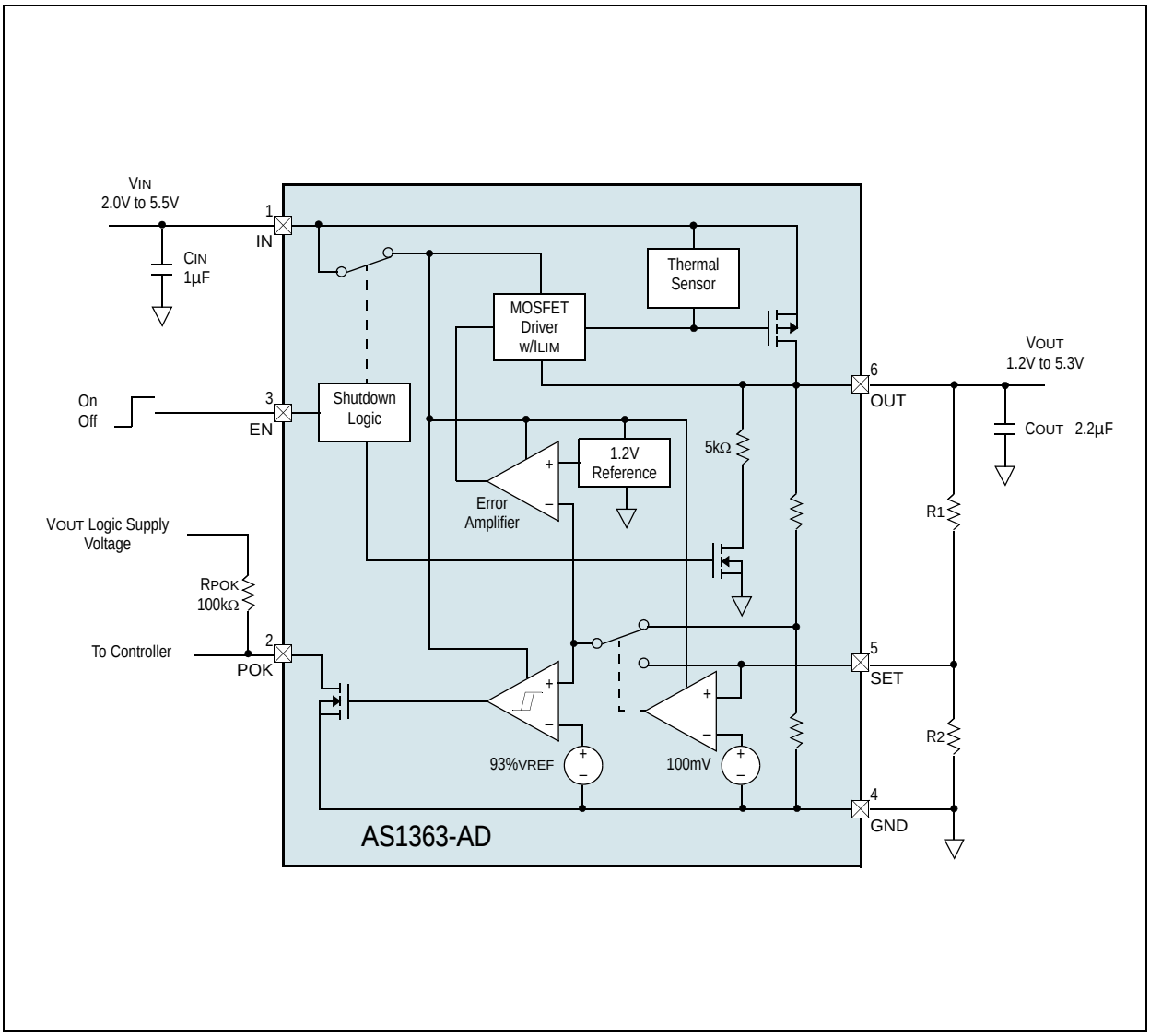


Figure 15 shows the block diagram of the AS1363. It identifies the basics of a series linear regulator employing a P-Channel MOSFET as the control element. A stable voltage reference (1.2VREF in Figure 15) is compared with an attenuated sample of the output voltage. Any difference between the two voltages (reference and sample) creates an output from the error amplifier that drives the series control element to reduce the difference to a minimum. The error amplifier incorporates additional buffering to drive the relatively large gate capacitance of the series pass P-channel MOSFET, when additional drive current is required under transient conditions.. Input supply variations are absorbed by the series element, and output voltage variations with loading are absorbed by the low output impedance of the regulator.

The device features a 1.2V reference, error amplifier, P-channel pass transistor, and internal feedback voltage-divider (see Figure 15). Additional blocks include an output current limiter, thermal sensor, and shutdown logic.

8.1 Shutdown

If pin EN is connected to GND the AS1363 is disabled. In shutdown mode all internal circuits are turned off, reducing supply current to 30nA typical. For normal operation pin EN must be connected to IN. During shutdown, POK is low.

8.2 Output Voltage Selection

The AS1363 is available in two versions (see Ordering Information on page 18). One version can only operate at one fixed output voltage and the other version can operate with a preset output voltage or with user-adjustable output voltages (1.2V to 5.3V).

- For the fixed output voltage version connect a capacitor CBYP from pin BYP to VOUT to improve PSRR and Noise performance (see Figure 16).
- To use the factory preset output voltage of the user-adjustable output voltage version, connect pin SET to GND (see Figure 17).
- For configurations using an output voltage other than the factory preset, a voltage-divider from OUT to SET to GND is required, as shown in (see Figure on page 1). A value for R2 in the 25kΩ to 100kΩ range should be sufficient. Calculate the value for R1 as:

$$R_1 = R_2 \times \left(\frac{V_{OUT}}{V_{SETBYP}} - 1 \right) \quad \textit{(EQ 1)}$$

Where:

VOUT is in a range from 1.2V to 5.3V.
VSET/BYP = 1.2V.

Figure 16. Fixed Output Voltage

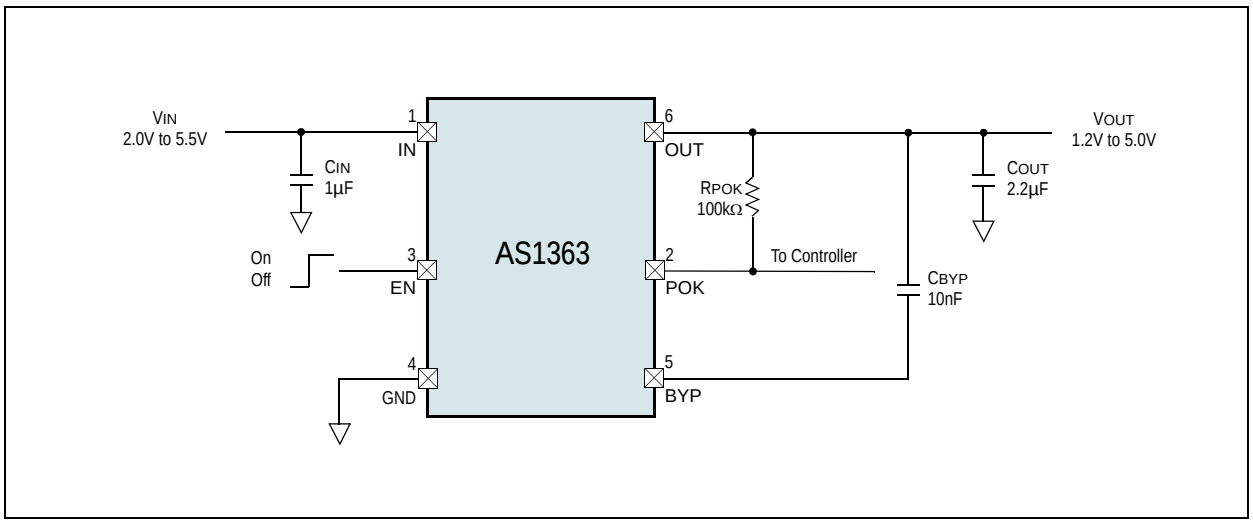
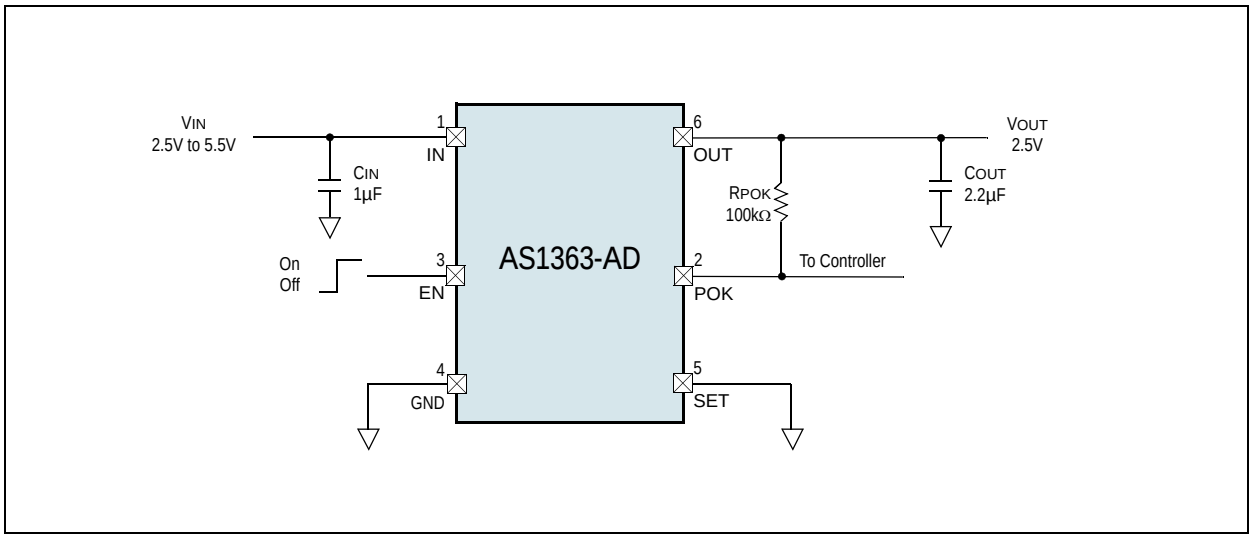


Figure 17. Adjustable Output using preset Output Voltage



8.3 Power-OK

The AS1363 features a power-ok indicator that asserts when the output voltage falls out of regulation. The open-drain POK output goes low when output voltage at OUT falls 6% below its nominal value. A 100kΩ pull-up resistor from POK to a (typically OUT) provides a logic control signal.

POK can be used as a power-on-reset (POR) signal to a microcontroller or can drive an external LED to indicate a power failure condition.

Note: POK is low during shutdown.

8.4 Current Limit

The AS1363 features current limiting circuitry that monitors the pass transistor, limiting short-circuit output current to 0.8A (typ). The circuitry of the AS1363 allows that the output can be shorted to ground for an indefinite period of time without damaging the device.

8.5 Thermal Overload Protection

Integrated thermal overload protection limits the total power dissipation in the AS1363. When the junction temperature (T_J) exceeds +170ºC typically, the pass transistor is turned off. Normal operation is continued when T_J drops approximately 20ºC.

Note: Regardless of the hysteresis, continuous short-circuit condition will result in a pulsed output.

9 Application Information

9.1 Dropout Voltage

Dropout is the input to output voltage difference, below which the linear regulator ceases to regulate. At this point, the output voltage change follows the input voltage change. Dropout voltage may be measured at different currents and, in particular at the regulator maximum one. From this is obtained the MOSFET maximum series resistance over temperature etc. More generally:

$$V_{DROPOUT} = I_{LOAD} \times R_{SERIES} \quad \text{(EQ 2)}$$

Dropout is probably the most important specification when the regulator is used in a battery application. The dropout performance of the regulator defines the useful “end of life” of the battery before replacement or re-charge is required.

Figure 18. Graphical Representation of Dropout Voltage

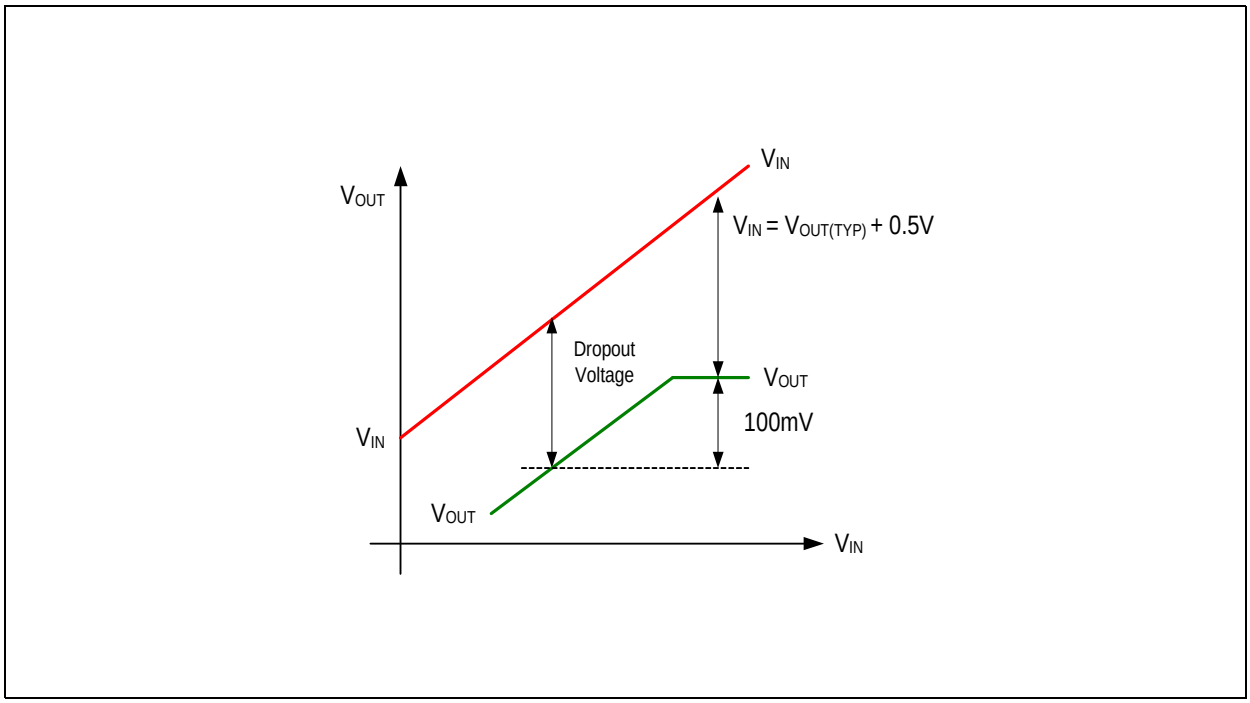


Figure 18 shows the variation of VOUT as VIN is varied for a certain load current. The practical value of dropout is the differential voltage (VOUT-VIN) measured at the point where the LDO output voltage has fallen by 100mV below the nominal, fully regulated output value. The nominal regulated output voltage of the LDO is that obtained when there is 500mV (or greater) input-output voltage differential.

9.2 Efficiency

Low quiescent current and low input-output voltage differential are important in battery applications amongst others, as the regulator efficiency is directly related to quiescent current and dropout voltage. Efficiency is given by:

$$\textit{Efficiency} = \frac{V_{LOAD} \times I_{LOAD}}{V_{IN}(I_Q + I_{LOAD})} \times 100\ \% \quad \text{(EQ 3)}$$

Where:
I_Q = Quiescent current of LDO measured at VBIAS.

9.3 Power Dissipation

Maximum power dissipation (PD) of the LDO is the sum of the power dissipated by the internal series MOSFET and the quiescent current required to bias the internal voltage reference and the internal error amplifier, and is calculated as:

$$PD_{(MAX)}(Seriespass) = I_{LOAD(MAX)}(V_{IN(MAX)} - V_{OUT(MIN)}) \ Watts \quad (EQ\ 4)$$

Internal power dissipation as a result of the bias current for the internal voltage reference and the error amplifier is calculated as:

$$PD_{(MAX)}(Bias) = V_{IN(MAX)}I_Q \ Watts \quad (EQ\ 5)$$

Total LDO power dissipation is calculated as:

$$PD_{(MAX)}(Total) = PD_{(MAX)}(Seriespass) + PD_{(MAX)}(Bias) \ Watts \quad (EQ\ 6)$$

9.4 Junction Temperature

Under all operating conditions, the maximum junction temperature should not be allowed to exceed 125ºC (unless the data sheet specifically allows). Limiting the maximum junction temperature requires knowledge of the heat path from junction to case (θ_{JC}ºC/W fixed by the IC manufacturer), and adjustment of the case to ambient heat path (θ_{CA}ºC/W) by manipulation of the PCB copper area adjacent to the IC position.

Figure 19. Package Physical Arrangements

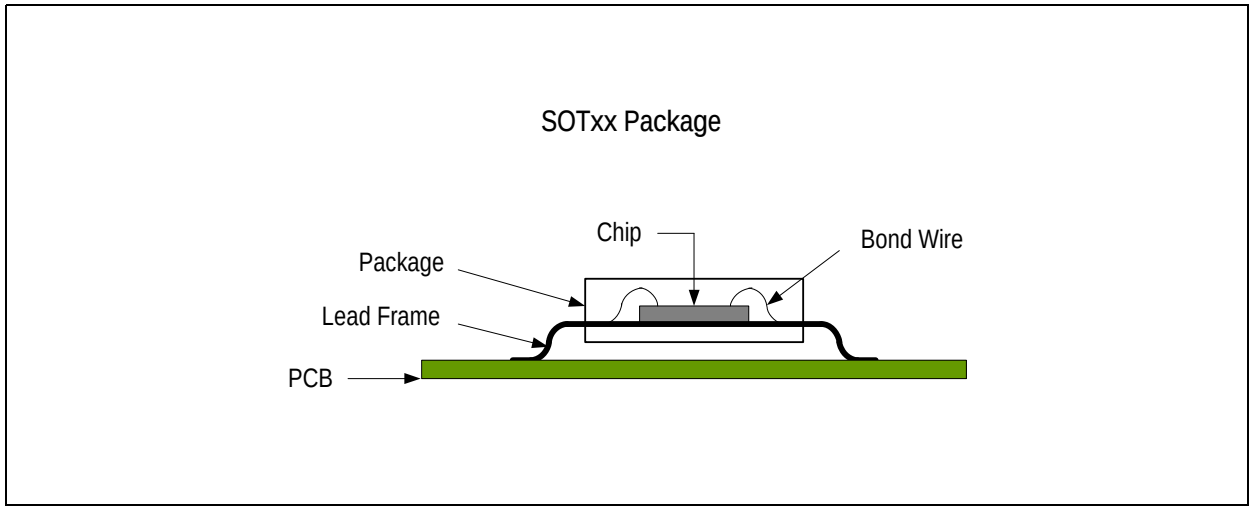
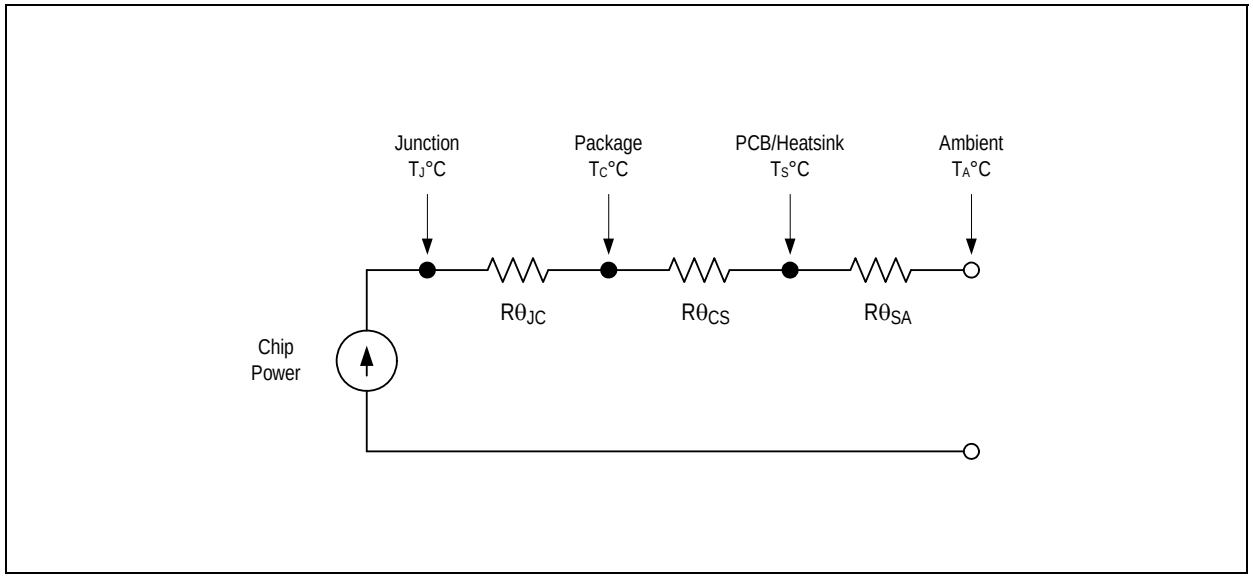


Figure 20. Steady State Heat Flow Equivalent Circuit



Total Thermal Path Resistance:

$$R\theta_{JA} = R\theta_{JC} + R\theta_{CS} + R\theta_{SA} \quad \textit{(EQ 7)}$$

Junction Temperature (T_JºC) is determined by:

$$T_J = (PD_{(MAX)} \times R\theta_{JA}) + T_{AMB} \ ºC \quad \textit{(EQ 8)}$$

9.5 Explanation of Steady State Specifications

9.5.1 Line Regulation

Line regulation is defined as the change in output voltage when the input (or line) voltage is changed by a known quantity. It is a measure of the regulator's ability to maintain a constant output voltage when the input voltage changes. Line regulation is a measure of the DC open loop gain of the error amplifier. More generally:

Line Regulation = $\frac{\Delta V_{OUT}}{\Delta V_{IN}}$ and is a pure number

In practise, line regulation is referred to the regulator output voltage in terms of % / VOUT. This is particularly useful when the same regulator is available with numerous output voltage trim options.

$$\textit{Line Regulation} = \frac{\Delta V_{OUT}}{\Delta V_{IN}} \times \frac{100}{V_{OUT}} \ \textit{\% / V} \quad \textit{(EQ 9)}$$

9.5.2 Load Regulation

Load regulation is defined as the change of the output voltage when the load current is changed by a known quantity. It is a measure of the regulator's ability to maintain a constant output voltage when the load changes. Load regulation is a measure of the DC closed loop output resistance of the regulator. More generally:

$$\textit{Load Regulation} = \frac{\Delta V_{OUT}}{\Delta I_{OUT}} \ \textit{and is units of ohms (Ω)} \quad \textit{(EQ 10)}$$

In practise, load regulation is referred to the regulator output voltage in terms of % / mA. This is particularly useful when the same regulator is available with numerous output voltage trim options.

$$\textit{Load Regulation} = \frac{\Delta V_{OUT}}{\Delta I_{OUT}} \times \frac{100}{\Delta V_{OUT}} \ \textit{\% / mA} \quad \textit{(EQ 11)}$$

9.5.3 Setting Accuracy

Accuracy of the final output voltage is determined by the accuracy of the ratio of R1 and R2, the reference accuracy and the input offset voltage of the error amplifier. When the regulator is supplied pre-trimmed, the output voltage accuracy is fully defined in the output voltage specification.

When the regulator has a SET terminal, the output voltage may be adjusted externally. In this case, the tolerance of the external resistor network must be incorporated into the final accuracy calculation. Generally:

$$V_{OUT} = (V_{SET} \pm \Delta V_{SET})\left(1 + \frac{R1 \pm \Delta R1}{R2 \pm \Delta R2}\right) \quad \textit{(EQ 12)}$$

The reference tolerance is given both at 25ºC and over the full operating temperature range.

9.5.4 Total Accuracy

Away from dropout, total steady state accuracy is the sum of setting accuracy, load regulation and line regulation. Generally:

Total % Accuracy = Setting % Accuracy + Load Regulation % + Line Regulation % *(EQ 13)*

9.6 Explanation of Dynamic Specifications

9.6.1 Power Supply Rejection Ratio (PSRR)

Known also as Ripple Rejection, this specification measures the ability of the regulator to reject noise and ripple beyond DC. PSRR is a summation of the individual rejections of the error amplifier, reference and AC leakage through the series pass transistor. The specification, in the form of a typical attenuation plot with respect to frequency, shows up the gain bandwidth compromises forced upon the designer in low quiescent current conditions. Generally:

$$PSSR = 20Log\frac{\delta V_{OUT}}{\delta V_{IN}}\ dB \text{ using lower case } \delta \text{ to indicate AC values} \qquad (EQ\ 14)$$

Power supply rejection ratio is fixed by the internal design of the regulator. Additional rejection must be provided externally.

9.6.2 Output Capacitor ESR

The series regulator is a negative feedback amplifier, and as such is conditionally stable. The ESR of the output capacitor is usually used to cancel one of the open loop poles of the error amplifier in order to produce a single pole response. Excessive ESR values may actually cause instability by excessive changes to the closed loop unity gain frequency crossover point. The range of ESR values for stability is usually shown either by a plot of stable ESR versus load current, or a limit statement in the datasheet.

Some ceramic capacitors exhibit large capacitance and ESR variations with temperature. Z5U and Y5V capacitors may be required to ensure stability at temperatures below T_{AMB} = -10ºC. With X7R or X5R capacitors, a 2.2µF capacitor should be sufficient at all operating temperatures.

Larger output capacitor values (10µF max) help to reduce noise and improve load transient-response, stability and power-supply rejection.

9.6.3 Input Capacitor

An input capacitor at VIN is required for stability. It is recommended that a 1.0µF capacitor be connected between the AS1363 power supply input pin VIN and ground (capacitance value may be increased without limit subject to ESR limits). This capacitor must be located at a distance of not more than 1cm from the VIN pin and returned to a clean analog ground. Any good quality ceramic, tantalum, or film capacitor may be used at the input.

9.6.4 Noise

The regulator output is a DC voltage with noise superimposed on the output. The noise comes from three sources; the reference, the error amplifier input stage, and the output voltage setting resistors. Noise is a random fluctuation and if not minimized in some applications, will produce system problems.

9.6.5 Transient Response

The series regulator is a negative feedback system, and therefore any change at the output will take a finite time to be corrected by the error loop. This “propagation time” is related to the bandwidth of the error loop. The initial response to an output transient comes from the output capacitance, and during this time, ESR is the dominant mechanism causing voltage transients at the output. More generally:

$$\delta V_{TRANSIENT} = \delta I_{OUTPUT} \times R_{ESR} \quad \text{Units are Volts, Amps, Ohms.} \qquad (EQ\ 15)$$

Thus an initial +50mA change of output current will produce a -12mV transient when the ESR=240mΩ. Remember to keep the ESR within stability recommendations when reducing ESR by adding multiple parallel output capacitors.

After the initial ESR transient, there follows a voltage droop during the time that the LDO feedback loop takes to respond to the output change. This drift is approx. linear in time and sums with the ESR contribution to make a total transient variation at the output of:

$$\delta V_{TRANSIENT} = \delta I_{OUTPUT} \times \left(R_{ESR} + \frac{T}{C_{LOAD}}\right) \quad \text{Units are Volts, Seconds, Farads, Ohms.} \qquad (EQ\ 16)$$

Where:
C_{LOAD} is output capacitor
T = Propagation delay of the LDO

This shows why it is convenient to increase the output capacitor value for a better support for fast load changes. Of course the formula holds for t < “propagation time”, so that a faster LDO needs a smaller cap at the load to achieve a similar transient response. For instance 50mA load current step produces 50mV output drop if the LDO response is 1usec and the load cap is 1µF.

There is also a steady state error caused by the finite output impedance of the regulator. This is derived from the load regulation specification discussed above.

9.6.6 Turn On Time

This specification defines the time taken for the LDO to awake from shutdown. The time is measured from the release of the enable pin to the time that the output voltage is within 5% of the final value. It assumes that the voltage at V_{IN} is stable and within the regulator Min and Max limits. Shutdown reduces the quiescent current to very low, mostly leakage values (<1µA).

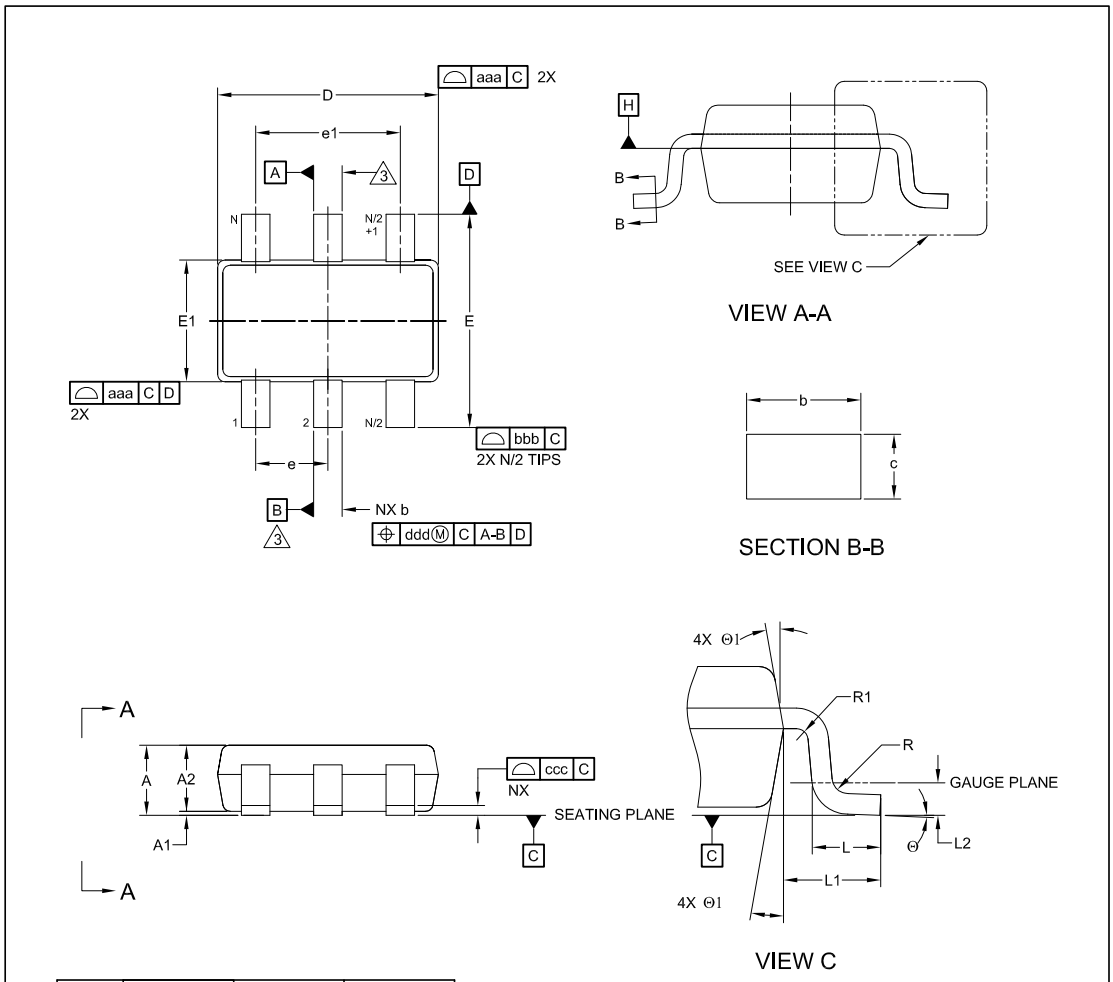
9.6.7 Thermal Protection

To prevent operation under extreme fault conditions, such as a permanent short circuit at the output, thermal protection is built into the device. Die temperature is measured, and when a 170ºC (AS1363) threshold is reached, the device enters shutdown. When the die cools sufficiently, the device will restart (assuming input voltage exists and the device is enabled). Hysteresis of 20ºC prevents low frequency oscillation between start-up and shutdown around the temperature threshold.

10 Package Drawings and Markings

The device is available in an 6-pin SOT23 package.

Figure 21. 6-pin SOT23 Package



REF.	MIN	NOM	MAX
A	-	-	1.10
A1	0	-	0.10
A2	0.70	0.90	1.00
b	0.30	-	0.50
c	0.08	-	0.20
D		2.90 BSC	
E		2.80 BSC	
E1		1.60 BSC	
e		0.95 BSC	
e1		1.90 BSC	
L	0.30	0.45	0.60
L1		0.60 REF	
L2		0.25 BSC	
Θ	0°	4°	8°
Θ1	4°	10°	12
aaa	-	0.15	-
bbb	-	0.20	-
ccc	-	0.10	-
ddd	-	0.20	-
N		6	

NOTE:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGELS ARE IN DEGREES.
3. DATUMS A & B TO BE DTERMINED AT DATUM H.

	ASSEMBLY ENGINEERING		
	Title: TSOT 6 LEAD		Reference Document: JEDEC MO - 193 Latest Revision
Drawn by: RH8	Date: 04.04.2013		
Checked by: GBO	Date: 04.04.2013	Drawing No.: JDW	Scale: Not in Scale
Approved by: MKR	Date: 04.04.2013	Dimension and Tolerance:	Sheet: 1 of 1

Figure 22. Package Markings

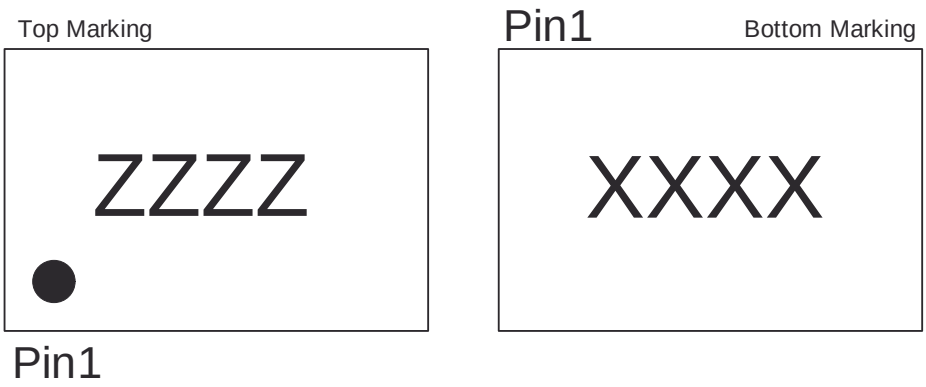


Table 5. Package Code

ZZZZ	XXXX
Marking	Encoded Datecode

11 Ordering Information

The device is available as the standard products shown in Table 6.

Table 6. Ordering Information

Ordering Code	Marking	Output	SET/BYP	Delivery Form	Package
AS1363-BSTT-AD	ASQ9	adjustable (preset to 2.5V)	SET	Tape and Reel	6-pin SOT23
AS1363-BSTT-12*	ASRY	1.2V	BYP	Tape and Reel	6-pin SOT23
AS1363-BSTT-15	ASRA	1.5V	BYP	Tape and Reel	6-pin SOT23
AS1363-BSTT-18	ASRB	1.8V	BYP	Tape and Reel	6-pin SOT23
AS1363-BSTT-30	ASRC	3.0V	BYP	Tape and Reel	6-pin SOT23
AS1363-BSTT-33	ASRD	3.3V	BYP	Tape and Reel	6-pin SOT23
AS1363-BSTT-45	ASRE	4.5V	BYP	Tape and Reel	6-pin SOT23

*Future product.

Non-standard devices are available between 1.4V and 4.6V in 50mV steps and between 4.6V and 5.0V in 100mV steps. For more information and inquiries contact http://www.ams.com/contact

Note: All products are RoHS compliant.
Buy our products or get free samples online at ICdirect: http://www.ams.com/ICdirect

Technical Support is available at http://www.ams.com/Technical-Support

For further information and requests, please contact us mailto:sales@ams.com
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