



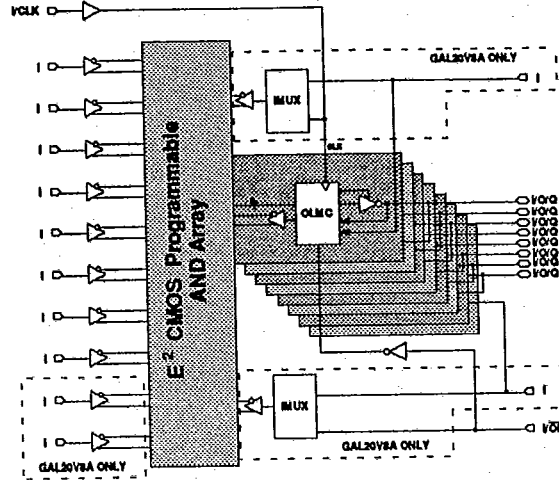
# GAL16V8A GAL20V8A

High Performance E<sup>2</sup>CMOS®  
Generic Array Logic™

**FEATURES**

- HIGH PERFORMANCE E<sup>2</sup>CMOS TECHNOLOGY
  - 10 ns Maximum Propagation Delay
  - F<sub>max</sub> = 62.5 MHz
  - 7 ns Maximum from Clock Input to Data Output
  - TTL Compatible 24 mA Outputs
  - UltraMOS® III Advanced CMOS Technology
- 50% REDUCTION IN POWER
  - 75mA Typ I<sub>cc</sub>
- E<sup>2</sup> CELL TECHNOLOGY
  - Reconfigurable Logic
  - Reprogrammable Cells
  - 100% Tested/Guaranteed 100% Yields
  - High Speed Electrical Erasure (<50ms)
  - 20 Year Data Retention
- EIGHT OUTPUT LOGIC MACROCELLS
  - Maximum Flexibility for Complex Logic Designs
  - Programmable Output Polarity
  - GAL16V8A Emulates 20-pin PAL® Devices with Full Function/Fuse Map/Parametric Compatibility
  - GAL20V8A Emulates 24-pin PAL® Devices with Full Function/Fuse Map/Parametric Compatibility
- PRELOAD AND POWER-ON RESET OF ALL REGISTERS
  - 100% Functional Testability
- ELECTRONIC SIGNATURE FOR IDENTIFICATION

**GAL16V8A / GAL20V8A BLOCK DIAGRAM**



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**DESCRIPTION**

The GAL16V8A and GAL20V8A, at 10 ns maximum propagation delay time, combine a high performance CMOS process with Electrically Erasable (E<sup>2</sup>) floating gate technology to provide the highest speed performance available in the PLD market. CMOS circuitry allows the GAL16V8A and GAL20V8A to consume just 75mA typical I<sub>cc</sub>, which represents a 50% savings in power when compared to their bipolar counterparts. The E<sup>2</sup> technology offers high speed (50ms) erase times, providing the ability to reprogram or reconfigure the devices quickly and efficiently.

The generic architecture provides maximum design flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user. The GAL16V8A and GAL20V8A are capable of emulating standard 20 and 24-pin PAL® devices. The GAL16V8A is capable of emulating standard 20-pin PAL architectures with full function/fuse map/parametric compatibility. The GAL20V8A is capable of emulating standard 24-pin PAL architectures with full function/fuse map/parametric compatibility. On the right is a table listing the PAL architectures that the GAL16V8A and GAL20V8A can replace.

Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. Therefore, Lattice guarantees 100% field programmability and functionality of all GAL products. Lattice also guarantees 100 erase/rewrite cycles and that data retention exceeds 20 years.

**GAL16V8A / GAL20V8A ARCHITECTURE EMULATION**

GAL20V8A PAL Architecture Emulation	GAL16V8A PAL Architecture Emulation
20L8	16L8
20H8	16H8
20R8	16R8
20R6	16R6
20R4	16R4
20P8	16P8
20RP8	16RP8
20RP6	16RP6
20RP4	16RP4
14L8	10L8
16L8	12L8
18L4	14L4
20L2	16L2
14H8	10H8
16H6	12H6
18H4	14H4
20H2	16H2
14P8	10P8
16P6	12P6
18P4	14P4
20P2	16P2

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 Specifications GAL16V8A  
 GAL20V8A

**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

Supply voltage  $V_{CC}$  ..... -5 to +7V  
 Input voltage applied ..... -2.5 to  $V_{CC} + 1.0V$   
 Off-state output voltage applied ..... -2.5 to  $V_{CC} + 1.0V$   
 Storage Temperature ..... -65 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

**SWITCHING TEST CONDITIONS**

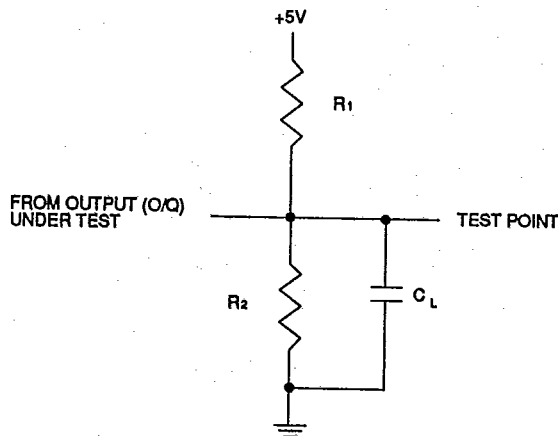
Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% - 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

Tri-state levels are measured 0.5V from steady-state active level.

COMMERCIAL		INDUSTRIAL		MILITARY	
$R_1$	$R_2$	$R_1$	$R_2$	$R_1$	$R_2$
200	390	200	390	390	750

AC Test Conditions:

- Cond. 1)  $R_1$  per table;  $C_L = 50pF$ ;  $R_2$  per above table
- Cond. 2) Active High  $R_1 = \infty$ ; Active Low  $R_1$  per table;  
 $C_L = 50pF$ ;  $R_2$  per above table
- Cond. 3) Active High  $R_1 = \infty$ ; Active Low  $R_1$  per table;  
 $C_L = 5pF$ ;  $R_2$  per above table



$C_L$  INCLUDES JIG AND PROBE TOTAL CAPACITANCE

**CAPACITANCE ( $T_A = 25^\circ C, f = 1.0 MHz$ )**

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
$C_i$	Input Capacitance	8	pF	$V_{CC} = 5.0V, V_i = 2.0V$
$C_{I/OQ}$	I/O/Q Capacitance	10	pF	$V_{CC} = 5.0V, V_{I/OQ} = 2.0V$

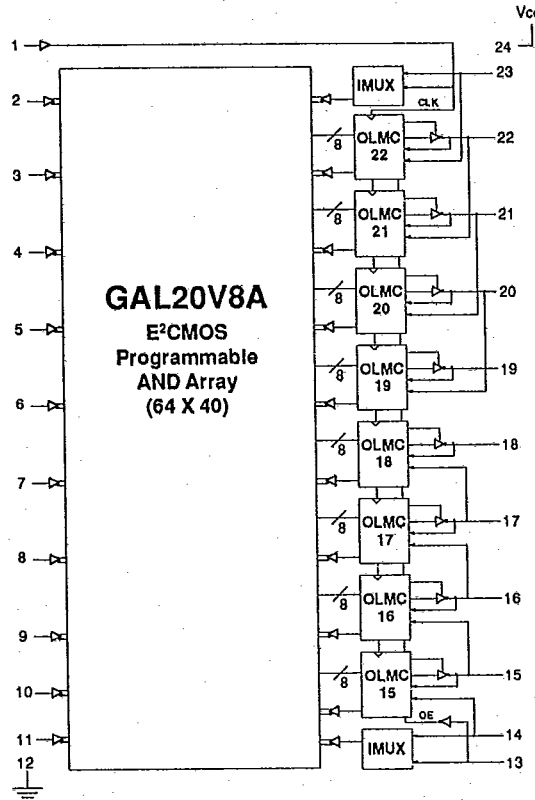
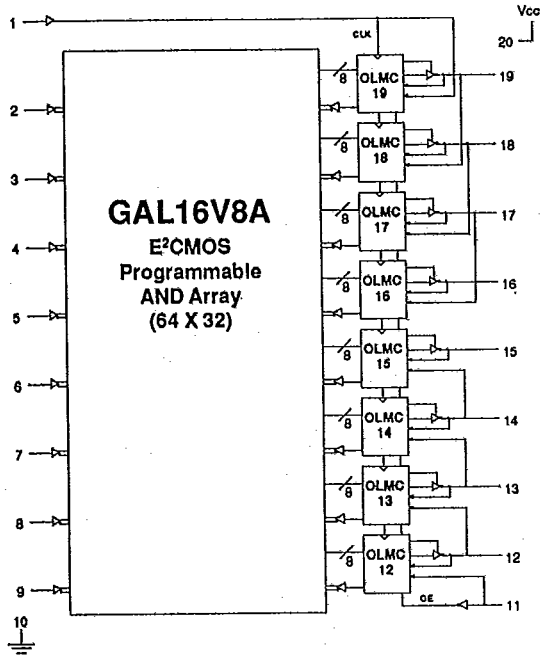
\*Guaranteed but not 100% tested.



T-46-13-27  
Specifications **GAL16V8A**  
**GAL20V8A**

**GAL16V8A BLOCK DIAGRAM**

**GAL20V8A BLOCK DIAGRAM**



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**GAL16V8A PIN DIAGRAM**

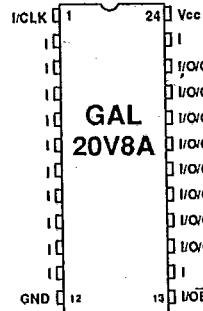
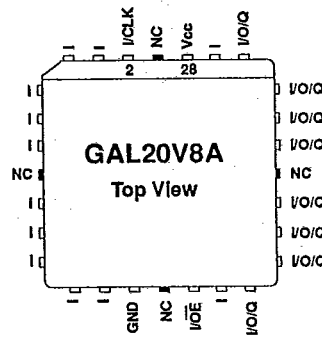
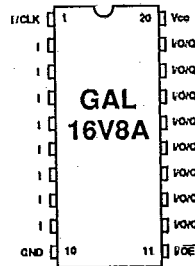
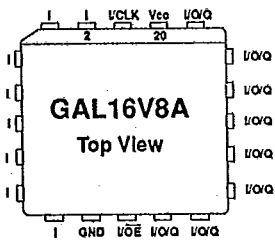
**GAL20V8A PIN DIAGRAM**

Chip Carrier

DIP

Chip Carrier

DIP

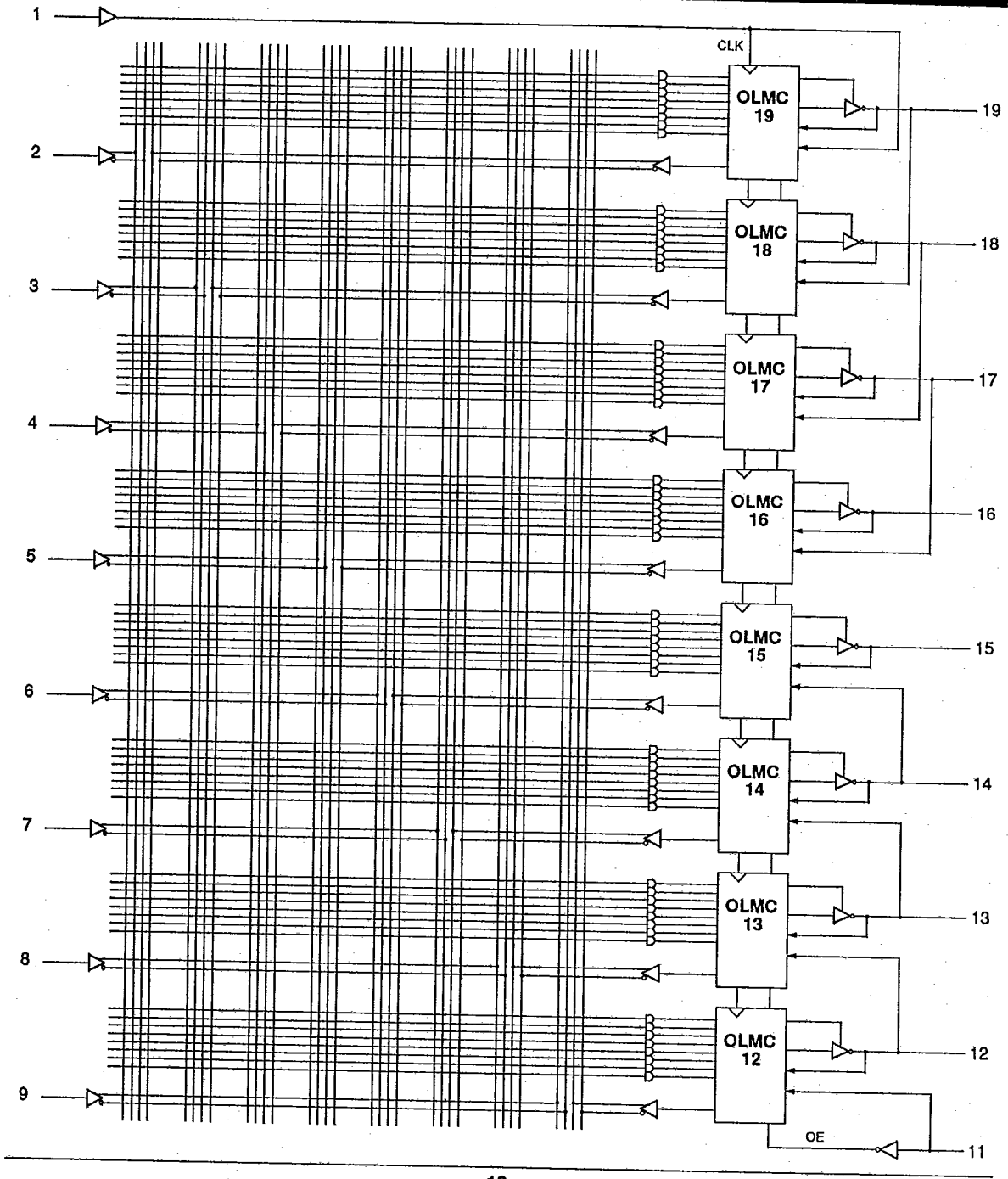


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Specifications GAL16V8A  
GAL20V8A

**GAL16V8A LOGIC DIAGRAM**



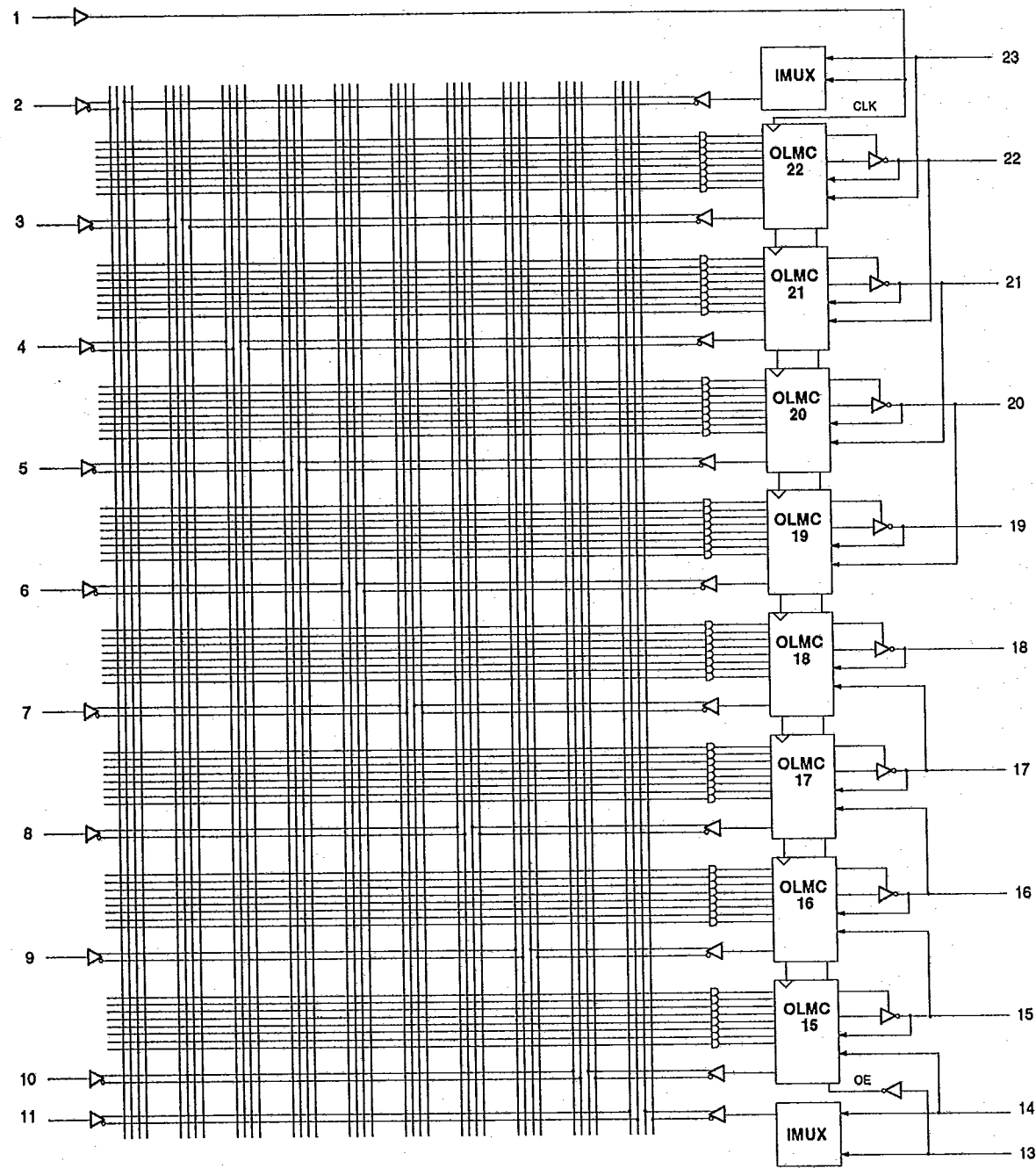


Specifications GAL16V8A

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GAL20V8A

GAL20V8A LOGIC DIAGRAM





T-46-13-27  
 Specifications **GAL16V8A**  
**GAL20V8A**

**ELECTRICAL CHARACTERISTICS****GAL16 / 20V8A-10L Commercial**

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
VOL	Output Low Voltage		—	—	0.5	V
VOH	Output High Voltage		2.4	—	—	V
IIL, IIH	Input Leakage Current		—	—	±10	μA
I/O/Q	Bidirectional Pin Leakage Current		—	—	±10	μA
IOS <sup>1</sup>	Output Short Circuit Current	V <sub>CC</sub> = 5V V <sub>OUT</sub> = 0.5V	-30	—	-150	mA
ICC	Operating Power Supply Current	V <sub>IL</sub> = 0.5V V <sub>IH</sub> = 3.0V f <sub>toggle</sub> = 25MHz	—	75	115	mA

1) One output at a time for a maximum duration of one second. V<sub>OUT</sub> = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.

**DC RECOMMENDED OPERATING CONDITIONS****GAL16 / 20V8A-10L Commercial**

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T <sub>A</sub>	Ambient Temperature	0	75	°C
V <sub>CC</sub>	Supply Voltage	4.75	5.25	V
V <sub>IL</sub>	Input Low Voltage	V <sub>SS</sub> - 0.5	0.8	V
V <sub>IH</sub>	Input High Voltage	2.0	V <sub>CC</sub> +1	V
I <sub>OL</sub>	Low Level Output Current	—	24	mA
I <sub>OH</sub>	High Level Output Current	—	-3.2	mA



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## Specifications GAL16V8A GAL20V8A

**SWITCHING CHARACTERISTICS****GAL16 / 20V8A-10L Commercial**

Over Recommended Operating Conditions

PARAMETER	#	FROM	TO	DESCRIPTION	TEST COND. <sup>1</sup>	MIN.	MAX.	UNITS
$t_{pd}$	1	I, I/O	O	Combinational Propagation Delay	1	3	10	ns
$t_{co}$	2	CLK	Q	Clock to Output Delay	1	2	7	ns
$t_{en}$	3	I, I/O	O	Output Enable, Z → O	2	—	10	ns
	4	$\overline{OE}$	Q	Output Register Enable, Z → Q	2	—	10	ns
$t_{dis}$	5	I, I/O	O	Output Disable, O → Z	3	—	10	ns
	6	$\overline{OE}$	Q	Output Register Disable, Q → Z	3	—	10	ns

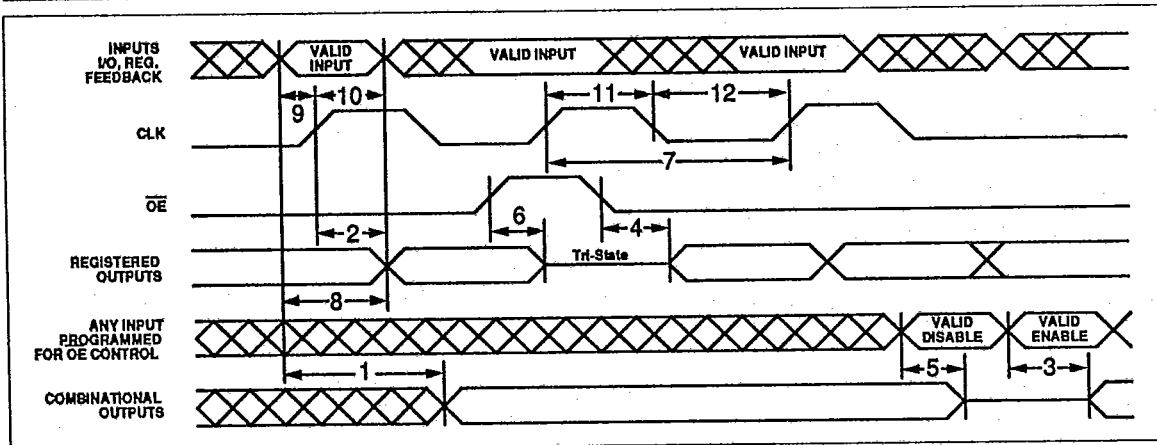
**2**

1) Refer to Switching Test Conditions section.

**AC RECOMMENDED OPERATING CONDITIONS****GAL16 / 20V8A-10L Commercial**

PARAMETER	#	DESCRIPTION	TEST COND.	MIN.	MAX.	UNITS
$f_{clk}$	7	Clock Frequency without Feedback <sup>1</sup> = $1 / (t_{wh} + t_{wl})$	1	0	62.5	MHz
	8	Clock Frequency with Feedback <sup>1</sup> = $1 / (t_{su} + t_{co})$	1	0	58.8	MHz
$t_{su}$	9	Setup Time, Input or Feedback, before CLK ↑	—	10	—	ns
$t_h$	10	Hold Time, Input or Feedback, after CLK ↑	—	0	—	ns
$t_w$	11	Clock Pulse Duration, High <sup>2</sup>	—	8	—	ns
	12	Clock Pulse Duration, Low <sup>2</sup>	—	8	—	ns

1)  $f_{clk}$  is for reference only and is not 100% tested. Various paths and architecture configurations will result in differing  $f_{clk}$  specifications.  
 2) Clock pulses of widths less than the specification may be detected as valid clock signals.

**SWITCHING WAVEFORMS**



T-46-13-27  
 Specifications **GAL16V8A**  
**GAL20V8A**

**ELECTRICAL CHARACTERISTICS****GAL16 / 20V8A-15L Commercial**

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
VOL	Output Low Voltage		—	—	0.5	V
VOH	Output High Voltage		2.4	—	—	V
IIL, IIH	Input Leakage Current		—	—	±10	μA
I/O/Q	Bidirectional Pin Leakage Current		—	—	±10	μA
IOS <sup>1</sup>	Output Short Circuit Current	V <sub>CC</sub> = 5V V <sub>OUT</sub> = 0.5V	-30	—	-150	mA
ICC	Operating Power Supply Current	V <sub>L</sub> = 0.5V V <sub>H</sub> = 3.0V f <sub>toggle</sub> = 25MHz	—	75	115	mA

1) One output at a time for a maximum duration of one second. V<sub>OUT</sub> = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.

**DC RECOMMENDED OPERATING CONDITIONS****GAL16 / 20V8A-15L Commercial**

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T <sub>A</sub>	Ambient Temperature	0	75	°C
V <sub>CC</sub>	Supply Voltage	4.75	5.25	V
V <sub>IL</sub>	Input Low Voltage	V <sub>SS</sub> - 0.5	0.8	V
V <sub>IH</sub>	Input High Voltage	2.0	V <sub>CC</sub> +1	V
I <sub>OL</sub>	Low Level Output Current	—	24	mA
I <sub>OH</sub>	High Level Output Current	—	-3.2	mA





T-46-13-27  
**Specifications GAL16V8A  
 GAL20V8A**

**SWITCHING CHARACTERISTICS**

GAL16 / 20V8A-15L Commercial

Over Recommended Operating Conditions

PARAMETER	#	FROM	TO	DESCRIPTION	TEST COND. <sup>1</sup>	MIN.	MAX.	UNITS
$t_{pd}$	1	I, I/O	O	Combinational Propagation Delay	1	3	15	ns
$t_{co}$	2	CLK	Q	Clock to Output Delay	1	2	10	ns
$t_{en}$	3	I, I/O	O	Output Enable, Z → O	2	—	15	ns
	4	$\overline{OE}$	Q	Output Register Enable, Z → Q	2	—	15	ns
$t_{ds}$	5	I, I/O	O	Output Disable, O → Z	3	—	15	ns
	6	$\overline{OE}$	Q	Output Register Disable, Q → Z	3	—	15	ns

**2**

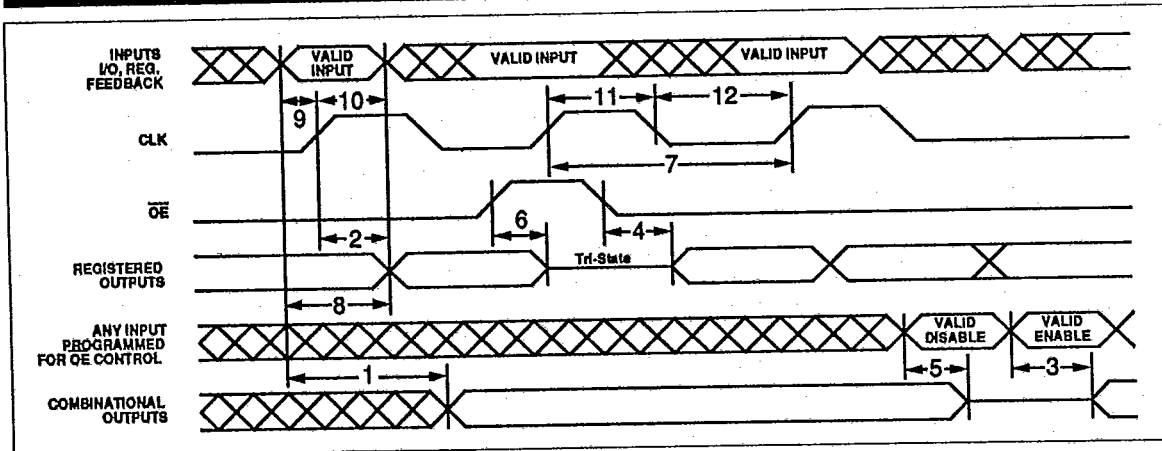
1) Refer to Switching Test Conditions section.

**AC RECOMMENDED OPERATING CONDITIONS**

GAL16 / 20V8A-15L Commercial

PARAMETER	#	DESCRIPTION	TEST COND.	MIN.	MAX.	UNITS
$f_{clk}$	7	Clock Frequency without Feedback <sup>1</sup> = $1 / (t_{wh} + t_{wl})$	1	0	62.5	MHz
	8	Clock Frequency with Feedback <sup>1</sup> = $1 / (t_{su} + t_{co})$	1	0	45.5	MHz
$t_{su}$	9	Setup Time, Input or Feedback, before CLK ↑	—	12	—	ns
$t_h$	10	Hold Time, Input or Feedback, after CLK ↑	—	0	—	ns
$t_w$	11	Clock Pulse Duration, High <sup>2</sup>	—	8	—	ns
	12	Clock Pulse Duration, Low <sup>2</sup>	—	8	—	ns

1)  $f_{clk}$  is for reference only and is not 100% tested. Various paths and architecture configurations will result in differing  $f_{clk}$  specifications.  
 2) Clock pulses of widths less than the specification may be detected as valid clock signals.

**SWITCHING WAVEFORMS**



T-46-13-27  
 Specifications GAL16V8A  
 GAL20V8A

**ELECTRICAL CHARACTERISTICS****GAL16 / 20V8A-15Q Commercial**

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
VOL	Output Low Voltage		—	—	0.5	V
VOH	Output High Voltage		2.4	—	—	V
IIL, IIH	Input Leakage Current		—	—	±10	μA
I/O/Q	Bidirectional Pin Leakage Current		—	—	±10	μA
IOS <sup>1</sup>	Output Short Circuit Current	V <sub>CC</sub> = 5V V <sub>OUT</sub> = 0.5V	-30	—	-150	mA
ICC	Operating Power Supply Current	V <sub>L</sub> = 0.5V V <sub>H</sub> = 3.0V f <sub>toggle</sub> = 15MHz	—	45	55	mA

1) One output at a time for a maximum duration of one second. V<sub>OUT</sub> = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.

**DC RECOMMENDED OPERATING CONDITIONS****GAL16 / 20V8A-15Q Commercial**

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T <sub>A</sub>	Ambient Temperature	0	75	°C
V <sub>CC</sub>	Supply Voltage	4.75	5.25	V
V <sub>IL</sub>	Input Low Voltage	V <sub>SS</sub> - 0.5	0.8	V
V <sub>IH</sub>	Input High Voltage	2.0	V <sub>CC</sub> +1	V
I <sub>OL</sub>	Low Level Output Current	—	24	mA
I <sub>OH</sub>	High Level Output Current	—	-3.2	mA



**SWITCHING CHARACTERISTICS**

**GAL16 / 20V8A-15Q Commercial**

Over Recommended Operating Conditions

PARAMETER	#	FROM	TO	DESCRIPTION	TEST COND. <sup>1</sup>	MIN.	MAX.	UNITS
$t_{pd}$	1	I, I/O	O	Combinational Propagation Delay	1	3	15	ns
$t_{co}$	2	CLK	Q	Clock to Output Delay	1	2	10	ns
$t_{en}$	3	I, I/O	O	Output Enable, Z → O	2	—	15	ns
	4	$\overline{OE}$	Q	Output Register Enable, Z → Q	2	—	15	ns
$t_{dis}$	5	I, I/O	O	Output Disable, O → Z	3	—	15	ns
	6	$\overline{OE}$	Q	Output Register Disable, Q → Z	3	—	15	ns

2

1) Refer to Switching Test Conditions section.

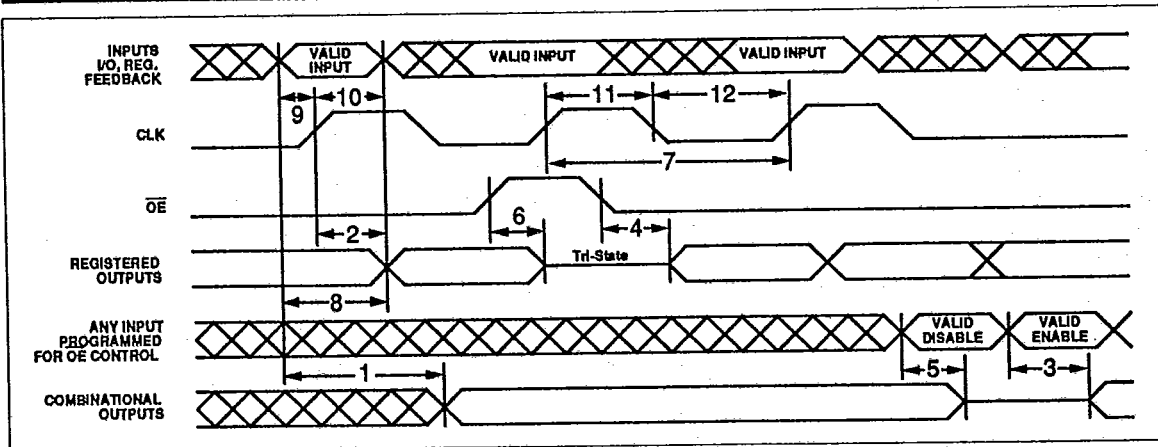
**AC RECOMMENDED OPERATING CONDITIONS**

**GAL16 / 20V8A-15Q Commercial**

PARAMETER	#	DESCRIPTION	TEST COND.	MIN.	MAX.	UNITS
$f_{clk}$	7	Clock Frequency without Feedback <sup>1</sup> = $1 / (t_{wh} + t_{wl})$	1	0	62.5	MHz
	8	Clock Frequency with Feedback <sup>1</sup> = $1 / (t_{su} + t_{co})$	1	0	45.5	MHz
$t_{su}$	9	Setup Time, Input or Feedback, before CLK ↑	—	12	—	ns
$t_h$	10	Hold Time, Input or Feedback, after CLK ↑	—	0	—	ns
$t_w$	11	Clock Pulse Duration, High <sup>2</sup>	—	8	—	ns
	12	Clock Pulse Duration, Low <sup>2</sup>	—	8	—	ns

1)  $f_{clk}$  is for reference only and is not 100% tested. Various paths and architecture configurations will result in differing  $f_{clk}$  specifications.  
2) Clock pulses of widths less than the specification may be detected as valid clock signals.

**SWITCHING WAVEFORMS**





T-46-13-27  
 Specifications GAL16V8A  
 GAL20V8A

**ELECTRICAL CHARACTERISTICS****GAL16 / 20V8A-25L Commercial**

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
VOL	Output Low Voltage		—	—	0.5	V
VOH	Output High Voltage		2.4	—	—	V
IIL, IIH	Input Leakage Current		—	—	±10	μA
I/OQ	Bidirectional Pin Leakage Current		—	—	±10	μA
I <sub>OS</sub> <sup>1</sup>	Output Short Circuit Current	V <sub>CC</sub> = 5V V <sub>OUT</sub> = 0.5V	-30	—	-150	mA
ICC	Operating Power Supply Current	V <sub>IL</sub> = 0.5V V <sub>IH</sub> = 3.0V f <sub>toggle</sub> = 15MHz	—	75	115	mA

1) One output at a time for a maximum duration of one second. V<sub>OUT</sub> = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.

**DC RECOMMENDED OPERATING CONDITIONS****GAL16 / 20V8A-25L Commercial**

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T <sub>A</sub>	Ambient Temperature	0	75	°C
V <sub>CC</sub>	Supply Voltage	4.75	5.25	V
V <sub>IL</sub>	Input Low Voltage	V <sub>SS</sub> - 0.5	0.8	V
V <sub>IH</sub>	Input High Voltage	2.0	V <sub>CC</sub> +1	V
I <sub>OL</sub>	Low Level Output Current	—	24	mA
I <sub>OH</sub>	High Level Output Current	—	-3.2	mA

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# Specifications GAL16V8A GAL20V8A

**SWITCHING CHARACTERISTICS****GAL16 / 20V8A-25L Commercial**

Over Recommended Operating Conditions

PARAMETER	#	FROM	TO	DESCRIPTION	TEST COND. <sup>1</sup>	MIN.	MAX.	UNITS
$t_{pd}$	1	I, I/O	O	Combinational Propagation Delay	1	3	25	ns
$t_{co}$	2	CLK	Q	Clock to Output Delay	1	2	12	ns
$t_{en}$	3	I, I/O	O	Output Enable, Z → O	2	—	25	ns
	4	OE	Q	Output Register Enable, Z → Q	2	—	20	ns
$t_{dis}$	5	I, I/O	O	Output Disable, O → Z	3	—	25	ns
	6	OE	Q	Output Register Disable, Q → Z	3	—	20	ns

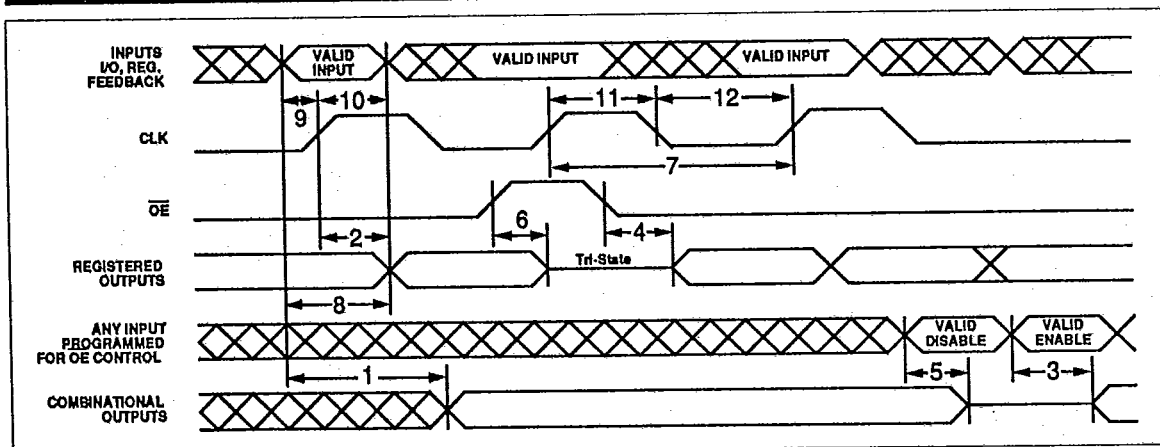
**2**

1) Refer to Switching Test Conditions section.

**AC RECOMMENDED OPERATING CONDITIONS****GAL16 / 20V8A-25L Commercial**

PARAMETER	#	DESCRIPTION	TEST COND.	MIN.	MAX.	UNITS
$f_{clk}$	7	Clock Frequency without Feedback <sup>1</sup> = $1 / (t_{wh} + t_{wl})$	1	0	41.7	MHz
	8	Clock Frequency with Feedback <sup>1</sup> = $1 / (t_{su} + t_{co})$	1	0	37	MHz
$t_{su}$	9	Setup Time, Input or Feedback, before CLK ↑	—	15	—	ns
$t_h$	10	Hold Time, Input or Feedback, after CLK ↑	—	0	—	ns
$t_w$	11	Clock Pulse Duration, High <sup>2</sup>	—	12	—	ns
	12	Clock Pulse Duration, Low <sup>2</sup>	—	12	—	ns

1)  $f_{clk}$  is for reference only and is not 100% tested. Various paths and architecture configurations will result in differing  $f_{clk}$  specifications.  
 2) Clock pulses of widths less than the specification may be detected as valid clock signals.

**SWITCHING WAVEFORMS**



T-46-13-27  
 Specifications **GAL16V8A**  
**GAL20V8A**

**ELECTRICAL CHARACTERISTICS****GAL16 / 20V8A-25Q Commercial**

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
V <sub>OL</sub>	Output Low Voltage		—	—	0.5	V
V <sub>OH</sub>	Output High Voltage		2.4	—	—	V
I <sub>IL</sub> , I <sub>IH</sub>	Input Leakage Current		—	—	±10	μA
I <sub>I/OQ</sub>	Bidirectional Pin Leakage Current		—	—	±10	μA
I <sub>OS</sub> <sup>1</sup>	Output Short Circuit Current	V <sub>CC</sub> = 5V V <sub>OUT</sub> = 0.5V	-30	—	-150	mA
I <sub>CC</sub>	Operating Power Supply Current	V <sub>L</sub> = 0.5V V <sub>H</sub> = 3.0V f <sub>toggle</sub> = 15MHz	—	45	55	mA

1) One output at a time for a maximum duration of one second. V<sub>OUT</sub> = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.

**DC RECOMMENDED OPERATING CONDITIONS****GAL16 / 20V8A-25Q Commercial**

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T <sub>A</sub>	Ambient Temperature	0	75	°C
V <sub>CC</sub>	Supply Voltage	4.75	5.25	V
V <sub>IL</sub>	Input Low Voltage	V <sub>SS</sub> - 0.5	0.8	V
V <sub>IH</sub>	Input High Voltage	2.0	V <sub>CC</sub> +1	V
I <sub>OL</sub>	Low Level Output Current	—	24	mA
I <sub>OH</sub>	High Level Output Current	—	-3.2	mA



**SWITCHING CHARACTERISTICS** GAL16 / 20V8A-25Q Commercial  
Over Recommended Operating Conditions

PARAMETER	#	FROM	TO	DESCRIPTION	TEST COND. <sup>1</sup>	MIN.	MAX.	UNITS
t <sub>pd</sub>	1	I, I/O	O	Combinational Propagation Delay	1	3	25	ns
t <sub>co</sub>	2	CLK	Q	Clock to Output Delay	1	2	12	ns
t <sub>en</sub>	3	I, I/O	O	Output Enable, Z → O	2	—	25	ns
	4	$\overline{OE}$	Q	Output Register Enable, Z → Q	2	—	20	ns
t <sub>dis</sub>	5	I, I/O	O	Output Disable, O → Z	3	—	25	ns
	6	$\overline{OE}$	Q	Output Register Disable, Q → Z	3	—	20	ns

2

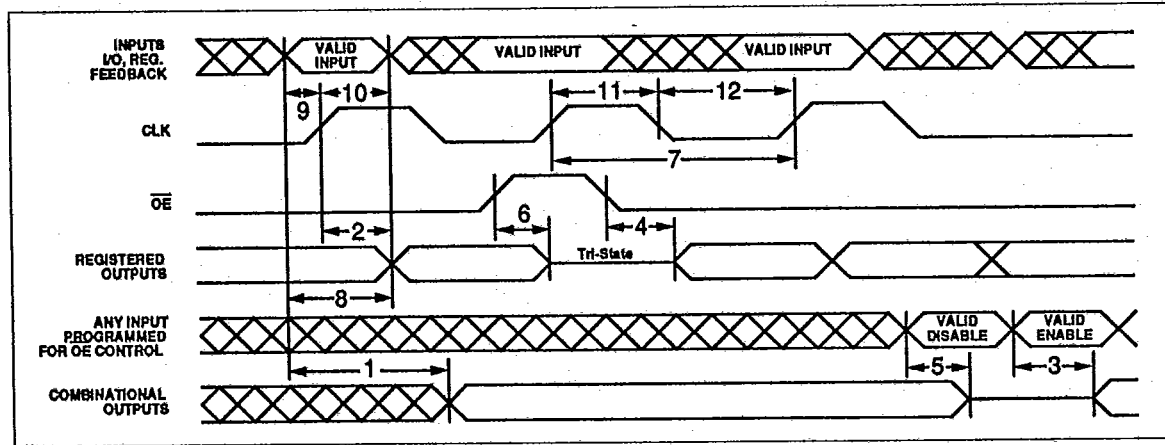
1) Refer to Switching Test Conditions section.

**AC RECOMMENDED OPERATING CONDITIONS** GAL16 / 20V8A-25Q Commercial

PARAMETER	#	DESCRIPTION	TEST COND.	MIN.	MAX.	UNITS
f <sub>clk</sub>	7	Clock Frequency without Feedback <sup>1</sup> = $1 / (t_{wh} + t_{wl})$	1	0	41.7	MHz
	8	Clock Frequency with Feedback <sup>1</sup> = $1 / (t_{su} + t_{co})$	1	0	37	MHz
t <sub>su</sub>	9	Setup Time, Input or Feedback, before CLK ↑	—	15	—	ns
t <sub>h</sub>	10	Hold Time, Input or Feedback, after CLK ↑	—	0	—	ns
t <sub>w</sub>	11	Clock Pulse Duration, High <sup>2</sup>	—	12	—	ns
	12	Clock Pulse Duration, Low <sup>2</sup>	—	12	—	ns

1) f<sub>clk</sub> is for reference only and is not 100% tested. Various paths and architecture configurations will result in differing f<sub>clk</sub> specifications.  
2) Clock pulses of widths less than the specification may be detected as valid clock signals.

**SWITCHING WAVEFORMS**





T-46-13-27  
 Specifications GAL16V8A  
 GAL20V8A

**ELECTRICAL CHARACTERISTICS**

GAL16 / 20V8A-15L Industrial

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
VOL	Output Low Voltage		—	—	0.5	V
VOH	Output High Voltage		2.4	—	—	V
IIL, IIH	Input Leakage Current		—	—	±10	μA
I/O/Q	Bidirectional Pin Leakage Current		—	—	±10	μA
IOS <sup>1</sup>	Output Short Circuit Current	V <sub>CC</sub> = 5V V <sub>OUT</sub> = 0.5V	-30	—	-150	mA
ICC	Operating Power Supply Current	V <sub>L</sub> = 0.5V V <sub>H</sub> = 3.0V f <sub>toggle</sub> = 25MHz	—	75	130	mA

1) One output at a time for a maximum duration of one second. V<sub>OUT</sub> = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.

**DC RECOMMENDED OPERATING CONDITIONS**

GAL16 / 20V8A-15L Industrial

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T <sub>A</sub>	Ambient Temperature	-40	85	°C
V <sub>CC</sub>	Supply Voltage	4.5	5.5	V
V <sub>IL</sub>	Input Low Voltage	V <sub>SS</sub> - 0.5	0.8	V
V <sub>IH</sub>	Input High Voltage	2.0	V <sub>CC</sub> +1	V
I <sub>OL</sub>	Low Level Output Current	—	24	mA
I <sub>OH</sub>	High Level Output Current	—	-3.2	mA





## Specifications GAL16V8A

## GAL20V8A

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## SWITCHING CHARACTERISTICS

GAL16 / 20V8A-15L Industrial

Over Recommended Operating Conditions

PARAMETER	#	FROM	TO	DESCRIPTION	TEST COND. <sup>1</sup>	MIN.	MAX.	UNITS
$t_{pd}$	1	I, I/O	O	Combinational Propagation Delay	1	3	15	ns
$t_{co}$	2	CLK	Q	Clock to Output Delay	1	2	12	ns
$t_{en}$	3	I, I/O	O	Output Enable, Z → O	2	—	15	ns
	4	$\overline{OE}$	Q	Output Register Enable, Z → Q	2	—	15	ns
$t_{dis}$	5	I, I/O	O	Output Disable, O → Z	3	—	15	ns
	6	$\overline{OE}$	Q	Output Register Disable, Q → Z	3	—	15	ns

2

1) Refer to Switching Test Conditions section.

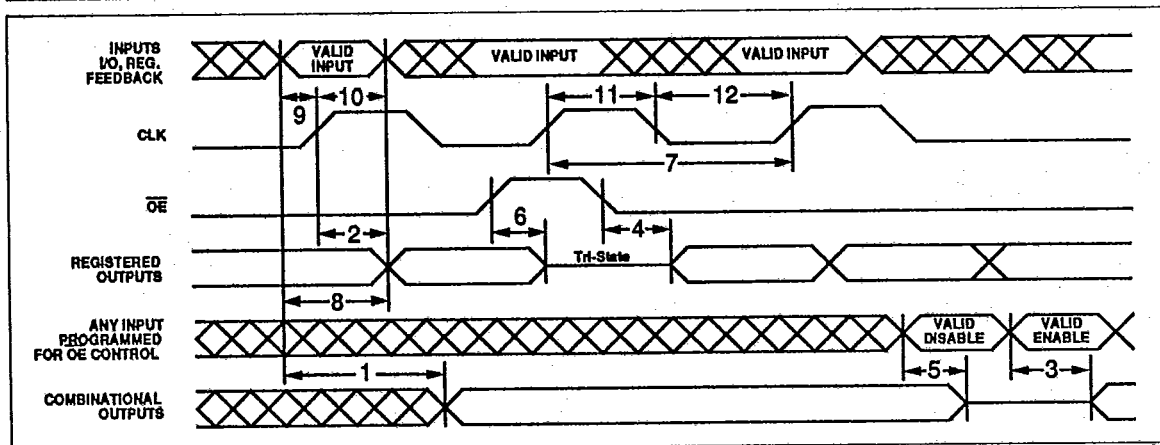
## AC RECOMMENDED OPERATING CONDITIONS

GAL16 / 20V8A-15L Industrial

PARAMETER	#	DESCRIPTION	TEST COND.	MIN.	MAX.	UNITS
$f_{clk}$	7	Clock Frequency without Feedback <sup>1</sup> = $1 / (t_{wh} + t_{wl})$	1	0	50	MHz
	8	Clock Frequency with Feedback <sup>1</sup> = $1 / (t_{su} + t_{co})$	1	0	41.6	MHz
$t_{su}$	9	Setup Time, Input or Feedback, before CLK ↑	—	12	—	ns
$t_h$	10	Hold Time, Input or Feedback, after CLK ↑	—	0	—	ns
$t_w$	11	Clock Pulse Duration, High <sup>2</sup>	—	10	—	ns
	12	Clock Pulse Duration, Low <sup>2</sup>	—	10	—	ns

1)  $f_{clk}$  is for reference only and is not 100% tested. Various paths and architecture configurations will result in differing  $f_{clk}$  specifications.  
 2) Clock pulses of widths less than the specification may be detected as valid clock signals.

## SWITCHING WAVEFORMS



Specifications **GAL16V8A****GAL20V8A**

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**ELECTRICAL CHARACTERISTICS**

GAL16 / 20V8A-20L Industrial

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
VOL	Output Low Voltage		—	—	0.5	V
VOH	Output High Voltage		2.4	—	—	V
IIL, IIH	Input Leakage Current		—	—	±10	μA
I/OQ	Bidirectional Pin Leakage Current		—	—	±10	μA
IOS <sup>1</sup>	Output Short Circuit Current	V <sub>CC</sub> = 5V V <sub>OUT</sub> = 0.5V	-30	—	-150	mA
ICC	Operating Power Supply Current	V <sub>IL</sub> = 0.5V V <sub>IH</sub> = 3.0V f <sub>toggle</sub> = 25MHz	—	75	130	mA

1) One output at a time for a maximum duration of one second. V<sub>OUT</sub> = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.

**DC RECOMMENDED OPERATING CONDITIONS**

GAL16 / 20V8A-20L Industrial

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T <sub>A</sub>	Ambient Temperature	-40	85	°C
V <sub>CC</sub>	Supply Voltage	4.5	5.5	V
V <sub>IL</sub>	Input Low Voltage	V <sub>SS</sub> - 0.5	0.8	V
V <sub>IH</sub>	Input High Voltage	2.0	V <sub>CC</sub> +1	V
I <sub>OL</sub>	Low Level Output Current	—	24	mA
I <sub>OH</sub>	High Level Output Current	—	-3.2	mA



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**Specifications GAL16V8A  
 GAL20V8A**

**SWITCHING CHARACTERISTICS**

**GAL16 / 20V8A-20L Industrial**

Over Recommended Operating Conditions

PARAMETER	#	FROM	TO	DESCRIPTION	TEST COND. <sup>1</sup>	MIN.	MAX.	UNITS
$t_{pd}$	1	I, I/O	O	Combinational Propagation Delay	1	3	20	ns
$t_{co}$	2	CLK	Q	Clock to Output Delay	1	2	15	ns
$t_{en}$	3	I, I/O	O	Output Enable, Z → O	2	—	20	ns
	4	$\overline{OE}$	Q	Output Register Enable, Z → Q	2	—	18	ns
$t_{dis}$	5	I, I/O	O	Output Disable, O → Z	3	—	20	ns
	6	$\overline{OE}$	Q	Output Register Disable, Q → Z	3	—	18	ns

**2**

1) Refer to Switching Test Conditions section.

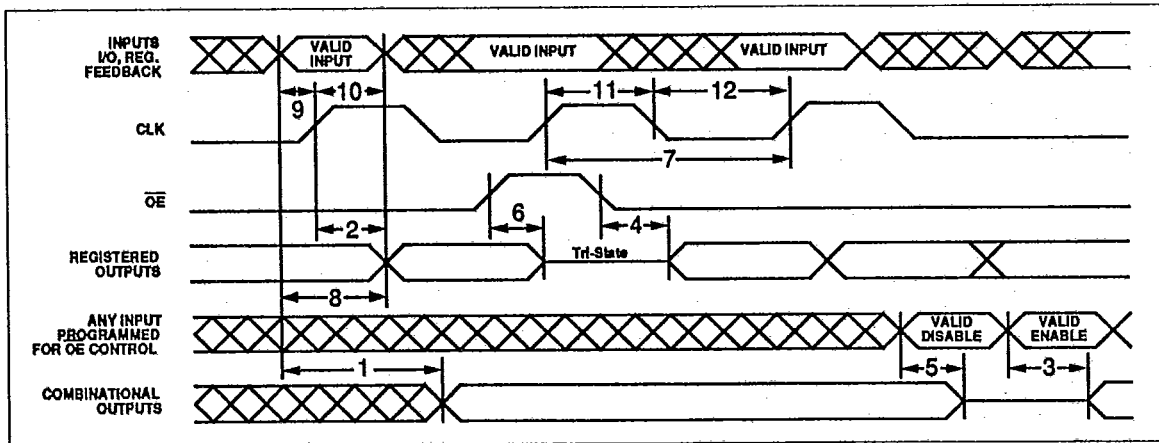
**AC RECOMMENDED OPERATING CONDITIONS**

**GAL16 / 20V8A-20L Industrial**

PARAMETER	#	DESCRIPTION	TEST COND.	MIN.	MAX.	UNITS
$f_{clk}$	7	Clock Frequency without Feedback <sup>1</sup> = $1 / (t_{wh} + t_{wl})$	1	0	41.7	MHz
	8	Clock Frequency with Feedback <sup>1</sup> = $1 / (t_{su} + t_{co})$	1	0	33.3	MHz
$t_{su}$	9	Setup Time, Input or Feedback, before CLK ↑	—	15	—	ns
$t_h$	10	Hold Time, Input or Feedback, after CLK ↑	—	0	—	ns
$t_w$	11	Clock Pulse Duration, High <sup>2</sup>	—	12	—	ns
	12	Clock Pulse Duration, Low <sup>2</sup>	—	12	—	ns

1)  $f_{clk}$  is for reference only and is not 100% tested. Various paths and architecture configurations will result in differing  $f_{clk}$  specifications.  
 2) Clock pulses of widths less than the specification may be detected as valid clock signals.

**SWITCHING WAVEFORMS**





# Specifications GAL16V8A GAL20V8A

## ELECTRICAL CHARACTERISTICS

### GAL16 / 20V8A-20Q Industrial

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
VOL	Output Low Voltage		—	—	0.5	V
VOH	Output High Voltage		2.4	—	—	V
IIL, IIH	Input Leakage Current		—	—	±10	μA
I/O/Q	Bidirectional Pin Leakage Current		—	—	±10	μA
IOS <sup>1</sup>	Output Short Circuit Current	V <sub>CC</sub> = 5V V <sub>OUT</sub> = 0.5V	-30	—	-150	mA
ICC	Operating Power Supply Current	V <sub>IL</sub> = 0.5V V <sub>IH</sub> = 3.0V f <sub>toggle</sub> = 15MHz	—	45	65	mA

1) One output at a time for a maximum duration of one second. V<sub>OUT</sub> = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.

## DC RECOMMENDED OPERATING CONDITIONS

### GAL16 / 20V8A-20Q Industrial

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T <sub>A</sub>	Ambient Temperature	-40	85	°C
V <sub>CC</sub>	Supply Voltage	4.5	5.5	V
V <sub>IL</sub>	Input Low Voltage	V <sub>SS</sub> - 0.5	0.8	V
V <sub>IH</sub>	Input High Voltage	2.0	V <sub>CC</sub> +1	V
I <sub>OL</sub>	Low Level Output Current	—	24	mA
I <sub>OH</sub>	High Level Output Current	—	-3.2	mA



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 Specifications GAL16V8A  
 GAL20V8A

## SWITCHING CHARACTERISTICS

## GAL16 / 20V8A-20Q Industrial

Over Recommended Operating Conditions

PARAMETER	#	FROM	TO	DESCRIPTION	TEST COND. <sup>1</sup>	MIN.	MAX.	UNITS
$t_{pd}$	1	I, I/O	O	Combinational Propagation Delay	1	3	20	ns
$t_{co}$	2	CLK	Q	Clock to Output Delay	1	2	15	ns
$t_{en}$	3	I, I/O	O	Output Enable, Z → O	2	—	20	ns
	4	$\overline{OE}$	Q	Output Register Enable, Z → Q	2	—	18	ns
$t_{dis}$	5	I, I/O	O	Output Disable, O → Z	3	—	20	ns
	6	$\overline{OE}$	Q	Output Register Disable, Q → Z	3	—	18	ns

2

1) Refer to Switching Test Conditions section.

## AC RECOMMENDED OPERATING CONDITIONS

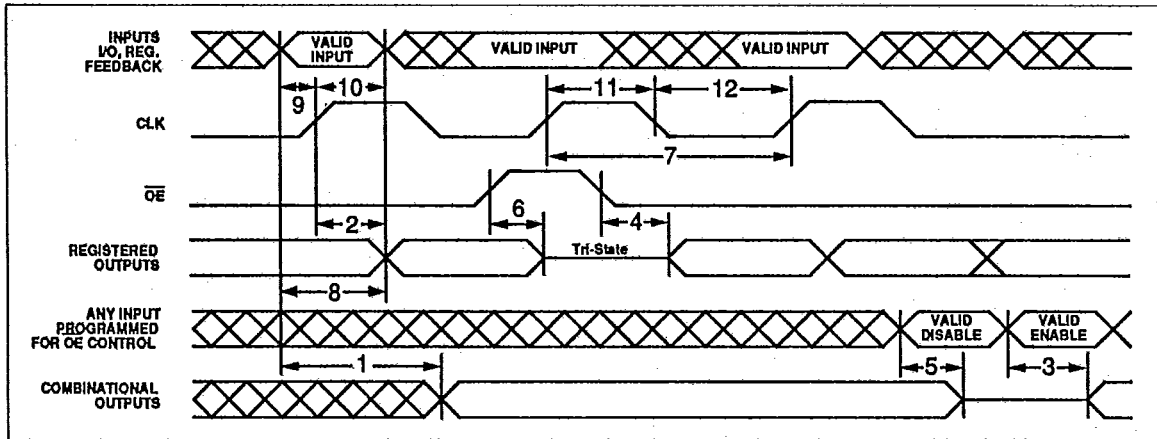
## GAL16 / 20V8A-20Q Industrial

PARAMETER	#	DESCRIPTION	TEST COND.	MIN.	MAX.	UNITS
$f_{clk}$	7	Clock Frequency without Feedback <sup>1</sup> = $1 / (t_{wh} + t_{wl})$	1	0	41.7	MHz
	8	Clock Frequency with Feedback <sup>1</sup> = $1 / (t_{su} + t_{co})$	1	0	33.3	MHz
$t_{su}$	9	Setup Time, Input or Feedback, before CLK ↑	—	15	—	ns
$t_h$	10	Hold Time, Input or Feedback, after CLK ↑	—	0	—	ns
$t_w$	11	Clock Pulse Duration, High <sup>2</sup>	—	12	—	ns
	12	Clock Pulse Duration, Low <sup>2</sup>	—	12	—	ns

1)  $f_{clk}$  is for reference only and is not 100% tested. Various paths and architecture configurations will result in differing  $f_{clk}$  specifications.

2) Clock pulses of widths less than the specification may be detected as valid clock signals.

## SWITCHING WAVEFORMS



**ELECTRICAL CHARACTERISTICS**

GAL16 / 20V8A-25L Industrial

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
VOL	Output Low Voltage		—	—	0.5	V
VOH	Output High Voltage		2.4	—	—	V
IIL, IIH	Input Leakage Current		—	—	±10	μA
I/OQ	Bidirectional Pin Leakage Current		—	—	±10	μA
I <sub>OS</sub> <sup>1</sup>	Output Short Circuit Current	V <sub>CC</sub> = 5V V <sub>OUT</sub> = 0.5V	-30	—	-150	mA
I <sub>CC</sub>	Operating Power Supply Current	V <sub>IL</sub> = 0.5V V <sub>IH</sub> = 3.0V f <sub>toggle</sub> = 25MHz	—	75	130	mA

1) One output at a time for a maximum duration of one second. V<sub>OUT</sub> = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.

**DC RECOMMENDED OPERATING CONDITIONS**

GAL16 / 20V8A-25L Industrial

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T <sub>A</sub>	Ambient Temperature	-40	85	°C
V <sub>CC</sub>	Supply Voltage	4.5	5.5	V
V <sub>IL</sub>	Input Low Voltage	V <sub>SS</sub> - 0.5	0.8	V
V <sub>IH</sub>	Input High Voltage	2.0	V <sub>CC</sub> +1	V
I <sub>OL</sub>	Low Level Output Current	—	24	mA
I <sub>OH</sub>	High Level Output Current	—	-3.2	mA



Specifications **GAL16V8A**  
**GAL20V8A**

**SWITCHING CHARACTERISTICS**

**GAL16 / 20V8A-25L Industrial**

Over Recommended Operating Conditions

PARAMETER	#	FROM	TO	DESCRIPTION	TEST COND. <sup>1</sup>	MIN.	MAX.	UNITS
$t_{pd}$	1	I, I/O	O	Combinational Propagation Delay	1	3	25	ns
$t_{co}$	2	CLK	Q	Clock to Output Delay	1	2	15	ns
$t_{en}$	3	I, I/O	O	Output Enable, Z → O	2	—	25	ns
	4	$\overline{OE}$	Q	Output Register Enable, Z → Q	2	—	20	ns
$t_{dis}$	5	I, I/O	O	Output Disable, O → Z	3	—	25	ns
	6	$\overline{OE}$	Q	Output Register Disable, Q → Z	3	—	20	ns

**2**

1) Refer to Switching Test Conditions section.

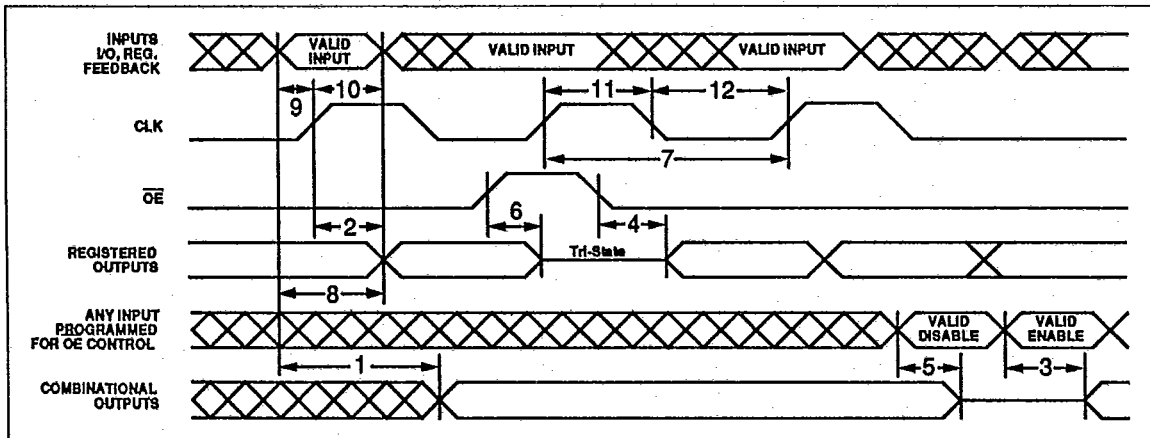
**AC RECOMMENDED OPERATING CONDITIONS**

**GAL16 / 20V8A-25L Industrial**

PARAMETER	#	DESCRIPTION	TEST COND.	MIN.	MAX.	UNITS
$f_{clk}$	7	Clock Frequency without Feedback <sup>1</sup> = $1 / (t_{wh} + t_{wl})$	1	0	33.3	MHz
	8	Clock Frequency with Feedback <sup>1</sup> = $1 / (t_{su} + t_{co})$	1	0	28.5	MHz
$t_{su}$	9	Setup Time, Input or Feedback, before CLK ↑	—	20	—	ns
$t_h$	10	Hold Time, Input or Feedback, after CLK ↑	—	0	—	ns
$t_w$	11	Clock Pulse Duration, High <sup>2</sup>	—	15	—	ns
	12	Clock Pulse Duration, Low <sup>2</sup>	—	15	—	ns

1)  $f_{clk}$  is for reference only and is not 100% tested. Various paths and architecture configurations will result in differing  $f_{clk}$  specifications.  
2) Clock pulses of widths less than the specification may be detected as valid clock signals.

**SWITCHING WAVEFORMS**





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**Specifications GAL16V8A  
 GAL20V8A**

**ELECTRICAL CHARACTERISTICS****GAL16 / 20V8A-15L Military**

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
VOL	Output Low Voltage		—	—	0.5	V
VOH	Output High Voltage		2.4	—	—	V
IIL, IIH	Input Leakage Current		—	—	±10	μA
I/O/Q	Bidirectional Pin Leakage Current		—	—	±10	μA
IOS <sup>1</sup>	Output Short Circuit Current	V <sub>CC</sub> = 5V V <sub>OUT</sub> = 0.5V	-30	—	-150	mA
ICC	Operating Power Supply Current	V <sub>IL</sub> = 0.5V V <sub>IH</sub> = 3.0V f <sub>toggle</sub> = 25MHz	—	75	130	mA

1) One output at a time for a maximum duration of one second. V<sub>OUT</sub> = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.

**DC RECOMMENDED OPERATING CONDITIONS****GAL16 / 20V8A-15L Military**

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T <sub>C</sub>	Case Temperature	-55	125	°C
V <sub>CC</sub>	Supply Voltage	4.5	5.5	V
V <sub>IL</sub>	Input Low Voltage	V <sub>SS</sub> - 0.5	0.8	V
V <sub>IH</sub>	Input High Voltage	2.0	V <sub>CC</sub> +1	V
I <sub>OL</sub>	Low Level Output Current	—	12	mA
I <sub>OH</sub>	High Level Output Current	—	-2.0	mA





Specifications **GAL16V8A**  
**GAL20V8A**

**SWITCHING CHARACTERISTICS**

**GAL16 / 20V8A-15L Military**

Over Recommended Operating Conditions

PARAMETER	#	FROM	TO	DESCRIPTION	TEST COND. <sup>1</sup>	MIN.	MAX.	UNITS
$t_{pd}$	1	I, I/O	O	Combinational Propagation Delay	1	3	15	ns
$t_{co}$	2	CLK	Q	Clock to Output Delay	1	2	12	ns
$t_{en}$	3	I, I/O	O	Output Enable, Z → O	2	—	15	ns
	4	$\overline{OE}$	Q	Output Register Enable, Z → Q	2	—	15	ns
$t_{dis}$	5	I, I/O	O	Output Disable, O → Z	3	—	15	ns
	6	$\overline{OE}$	Q	Output Register Disable, Q → Z	3	—	15	ns

2

1) Refer to Switching Test Conditions section.

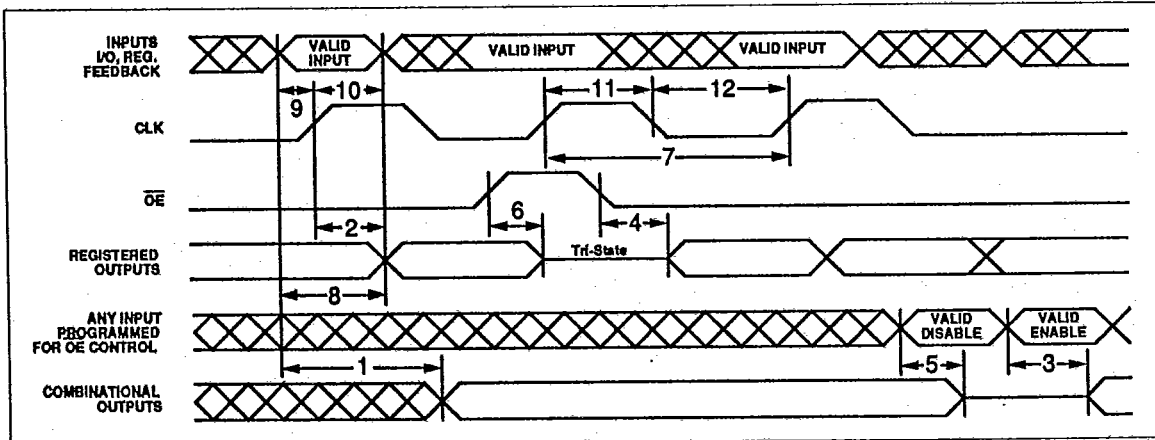
**AC RECOMMENDED OPERATING CONDITIONS**

**GAL16 / 20V8A-15L Military**

PARAMETER	#	DESCRIPTION	TEST COND.	MIN.	MAX.	UNITS
$f_{clk}$	7	Clock Frequency without Feedback <sup>1</sup> = $1 / (t_{wh} + t_{wl})$	1	0	50	MHz
	8	Clock Frequency with Feedback <sup>1</sup> = $1 / (t_{su} + t_{co})$	1	0	41.6	MHz
$t_{su}$	9	Setup Time, Input or Feedback, before CLK ↑	—	12	—	ns
$t_h$	10	Hold Time, Input or Feedback, after CLK ↑	—	0	—	ns
$t_w$	11	Clock Pulse Duration, High <sup>2</sup>	—	10	—	ns
	12	Clock Pulse Duration, Low <sup>2</sup>	—	10	—	ns

1)  $f_{clk}$  is for reference only and is not 100% tested. Various paths and architecture configurations will result in differing  $f_{clk}$  specifications.  
2) Clock pulses of widths less than the specification may be detected as valid clock signals.

**SWITCHING WAVEFORMS**





T-46-13-27  
**Specifications GAL16V8A  
 GAL20V8A**

**ELECTRICAL CHARACTERISTICS****GAL16 / 20V8A-20L Military**

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
VOL	Output Low Voltage		—	—	0.5	V
VOH	Output High Voltage		2.4	—	—	V
IIL, IIH	Input Leakage Current		—	—	±10	μA
I/O/Q	Bidirectional Pin Leakage Current		—	—	±10	μA
IOS <sup>1</sup>	Output Short Circuit Current	V <sub>CC</sub> = 5V V <sub>OUT</sub> = 0.5V	-30	—	-150	mA
ICC	Operating Power Supply Current	V <sub>IL</sub> = 0.5V V <sub>IH</sub> = 3.0V f <sub>toggle</sub> = 25MHz	—	75	130	mA

1) One output at a time for a maximum duration of one second. V<sub>OUT</sub> = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.

**DC RECOMMENDED OPERATING CONDITIONS****GAL16 / 20V8A-20L Military**

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T <sub>C</sub>	Case Temperature	-55	125	°C
V <sub>CC</sub>	Supply Voltage	4.5	5.5	V
V <sub>IL</sub>	Input Low Voltage	V <sub>SS</sub> - 0.5	0.8	V
V <sub>IH</sub>	Input High Voltage	2.0	V <sub>CC</sub> +1	V
I <sub>OL</sub>	Low Level Output Current	—	12	mA
I <sub>OH</sub>	High Level Output Current	—	-2.0	mA



Specifications **GAL16V8A**  
**GAL20V8A**

**SWITCHING CHARACTERISTICS**

**GAL16 / 20V8A-20L Military**

Over Recommended Operating Conditions

PARAMETER	#	FROM	TO	DESCRIPTION	TEST COND. <sup>1</sup>	MIN.	MAX.	UNITS
$t_{pd}$	1	I, I/O	O	Combinational Propagation Delay	1	3	20	ns
$t_{co}$	2	CLK	Q	Clock to Output Delay	1	2	15	ns
$t_{en}$	3	I, I/O	O	Output Enable, Z → O	2	—	20	ns
	4	$\overline{OE}$	Q	Output Register Enable, Z → Q	2	—	18	ns
$t_{dis}$	5	I, I/O	O	Output Disable, O → Z	3	—	20	ns
	6	$\overline{OE}$	Q	Output Register Disable, Q → Z	3	—	18	ns

**2**

1) Refer to Switching Test Conditions section.

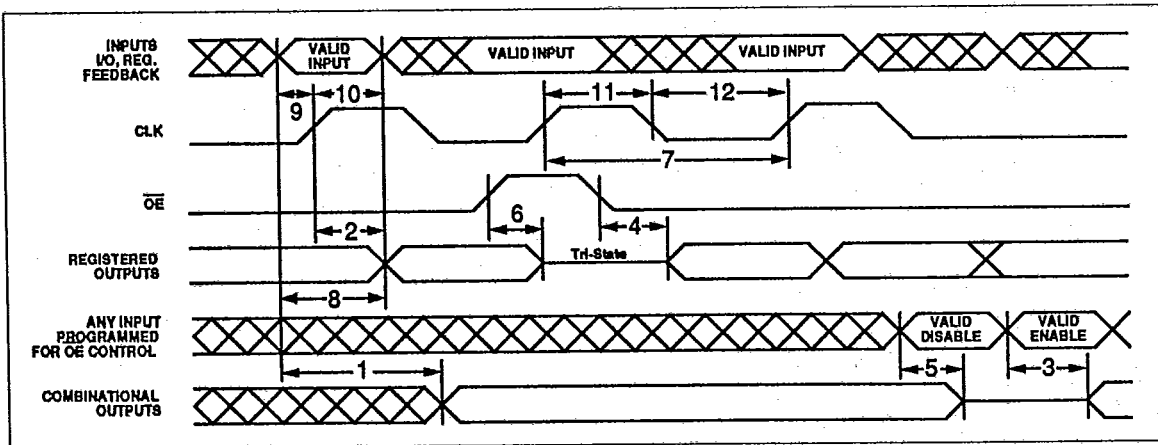
**AC RECOMMENDED OPERATING CONDITIONS**

**GAL16 / 20V8A-20L Military**

PARAMETER	#	DESCRIPTION	TEST COND.	MIN.	MAX.	UNITS
$f_{clk}$	7	Clock Frequency without Feedback <sup>1</sup> = $1 / (t_{wh} + t_{wl})$	1	0	41.7	MHz
	8	Clock Frequency with Feedback <sup>1</sup> = $1 / (t_{su} + t_{co})$	1	0	33.3	MHz
$t_{su}$	9	Setup Time, Input or Feedback, before CLK ↑	—	15	—	ns
$t_h$	10	Hold Time, Input or Feedback, after CLK ↑	—	0	—	ns
$t_w$	11	Clock Pulse Duration, High <sup>2</sup>	—	12	—	ns
	12	Clock Pulse Duration, Low <sup>2</sup>	—	12	—	ns

- 1)  $f_{clk}$  is for reference only and is not 100% tested. Various paths and architecture configurations will result in differing  $f_{clk}$  specifications.
- 2) Clock pulses of widths less than the specification may be detected as valid clock signals.

**SWITCHING WAVEFORMS**





# Specifications GAL16V8A GAL20V8A

## ELECTRICAL CHARACTERISTICS

**GAL16 / 20V8A-20Q Military**

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
VOL	Output Low Voltage		—	—	0.5	V
VOH	Output High Voltage		2.4	—	—	V
IIL, IIH	Input Leakage Current		—	—	±10	μA
I/O/Q	Bidirectional Pin Leakage Current		—	—	±10	μA
IOS <sup>1</sup>	Output Short Circuit Current	V <sub>CC</sub> = 5V V <sub>OUT</sub> = 0.5V	-30	—	-150	mA
ICC	Operating Power Supply Current	V <sub>L</sub> = 0.5V V <sub>H</sub> = 3.0V f <sub>toggle</sub> = 15MHz	—	45	65	mA

1) One output at a time for a maximum duration of one second. V<sub>OUT</sub> = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.

## DC RECOMMENDED OPERATING CONDITIONS

**GAL16 / 20V8A-20Q Military**

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T <sub>C</sub>	Case Temperature	-55	125	°C
V <sub>CC</sub>	Supply Voltage	4.5	5.5	V
V <sub>IL</sub>	Input Low Voltage	V <sub>SS</sub> - 0.5	0.8	V
V <sub>IH</sub>	Input High Voltage	2.0	V <sub>CC</sub> +1	V
I <sub>OL</sub>	Low Level Output Current	—	12	mA
I <sub>OH</sub>	High Level Output Current	—	-2.0	mA



Specifications **GAL16V8A**  
**GAL20V8A**

**SWITCHING CHARACTERISTICS**

**GAL16 / 20V8A-20Q Military**

Over Recommended Operating Conditions

2

PARAMETER	#	FROM	TO	DESCRIPTION	TEST COND. <sup>1</sup>	MIN.	MAX.	UNITS
$t_{pd}$	1	I, I/O	O	Combinational Propagation Delay	1	3	20	ns
$t_{co}$	2	CLK	Q	Clock to Output Delay	1	2	15	ns
$t_{en}$	3	I, I/O	O	Output Enable, Z → O	2	—	20	ns
	4	$\overline{OE}$	Q	Output Register Enable, Z → Q	2	—	18	ns
$t_{dis}$	5	I, I/O	O	Output Disable, O → Z	3	—	20	ns
	6	$\overline{OE}$	Q	Output Register Disable, Q → Z	3	—	18	ns

1) Refer to Switching Test Conditions section.

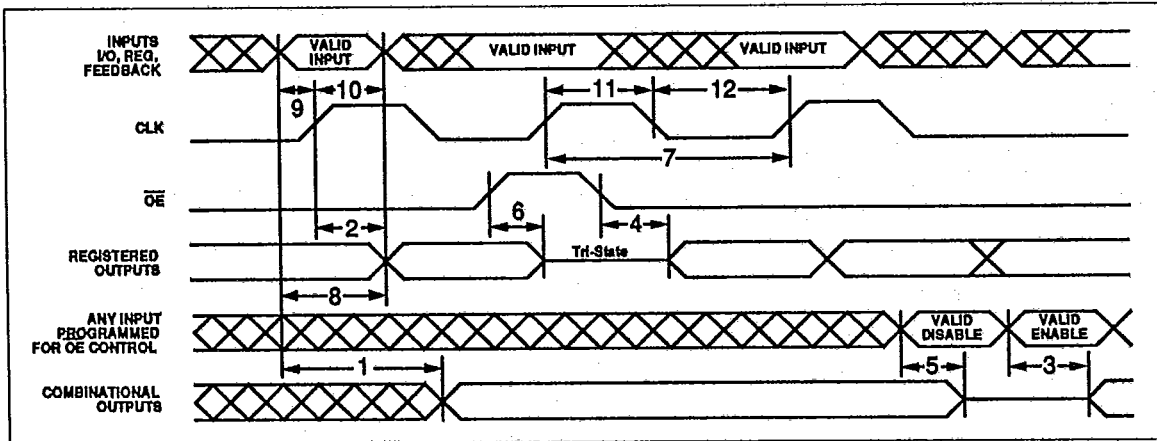
**AC RECOMMENDED OPERATING CONDITIONS**

**GAL16 / 20V8A-20Q Military**

PARAMETER	#	DESCRIPTION	TEST COND.	MIN.	MAX.	UNITS
$f_{clk}$	7	Clock Frequency without Feedback <sup>1</sup> = $1 / (t_{wh} + t_{wl})$	1	0	41.7	MHz
	8	Clock Frequency with Feedback <sup>1</sup> = $1 / (t_{su} + t_{co})$	1	0	33.3	MHz
$t_{su}$	9	Setup Time, Input or Feedback, before CLK ↑	—	15	—	ns
$t_h$	10	Hold Time, Input or Feedback, after CLK ↑	—	0	—	ns
$t_w$	11	Clock Pulse Duration, High <sup>2</sup>	—	12	—	ns
	12	Clock Pulse Duration, Low <sup>2</sup>	—	12	—	ns

1)  $f_{clk}$  is for reference only and is not 100% tested. Various paths and architecture configurations will result in differing  $f_{clk}$  specifications.  
2) Clock pulses of widths less than the specification may be detected as valid clock signals.

**SWITCHING WAVEFORMS**





T-46-13-27  
**Specifications GAL16V8A  
 GAL20V8A**

### OUTPUT LOGIC MACROCELL (OLMC)

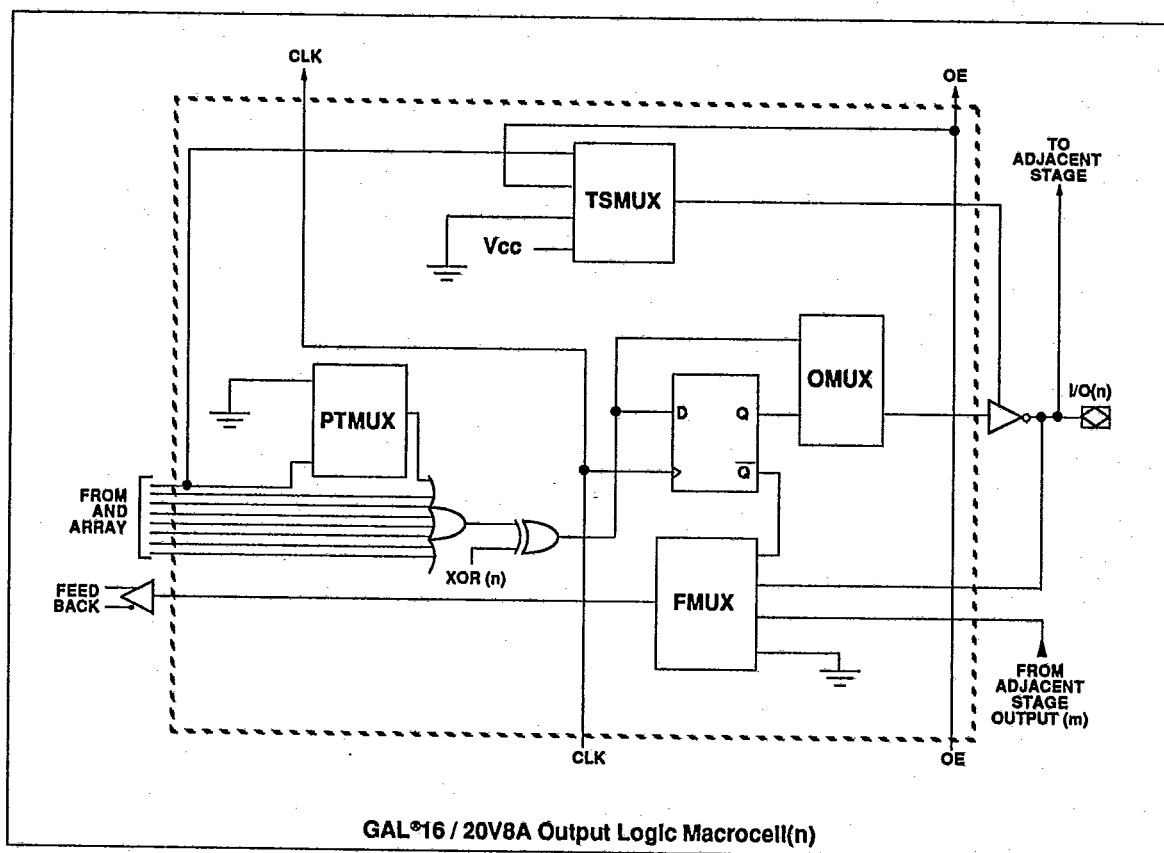
The following discussion pertains to configuring the output logic macrocell. It should be noted that actual implementation is accomplished by development software/hardware and is completely transparent to the user.

There are three OLMC configuration modes possible: registered, complex, and simple. These are illustrated in the diagrams on the following pages. You cannot mix modes, either all OLMCs are simple, complex, or registered (in registered mode the output can be combinational or registered).

The outputs of the AND array are fed into an OLMC, where each output can be individually set to active high or active low, with either combinational (asynchronous) or registered (synchronous)

configurations. A common output enable is connected to all registered outputs; or a product term can be used to provide individual output enable control for combinational outputs in the registered mode or combinational outputs in the complex mode. There is no output enable control in the simple mode. The output logic macrocell provides the designer with maximum output flexibility in matching signal requirements, thus providing more functionality than possible with existing 20 and 24-pin PAL® devices.

The six valid macrocell configurations, two configurations per mode, are shown in each of the macrocell equivalent diagrams. Pin and macrocell functions are detailed in the following diagrams.





# Specifications GAL16V8A GAL20V8A

## REGISTERED MODE

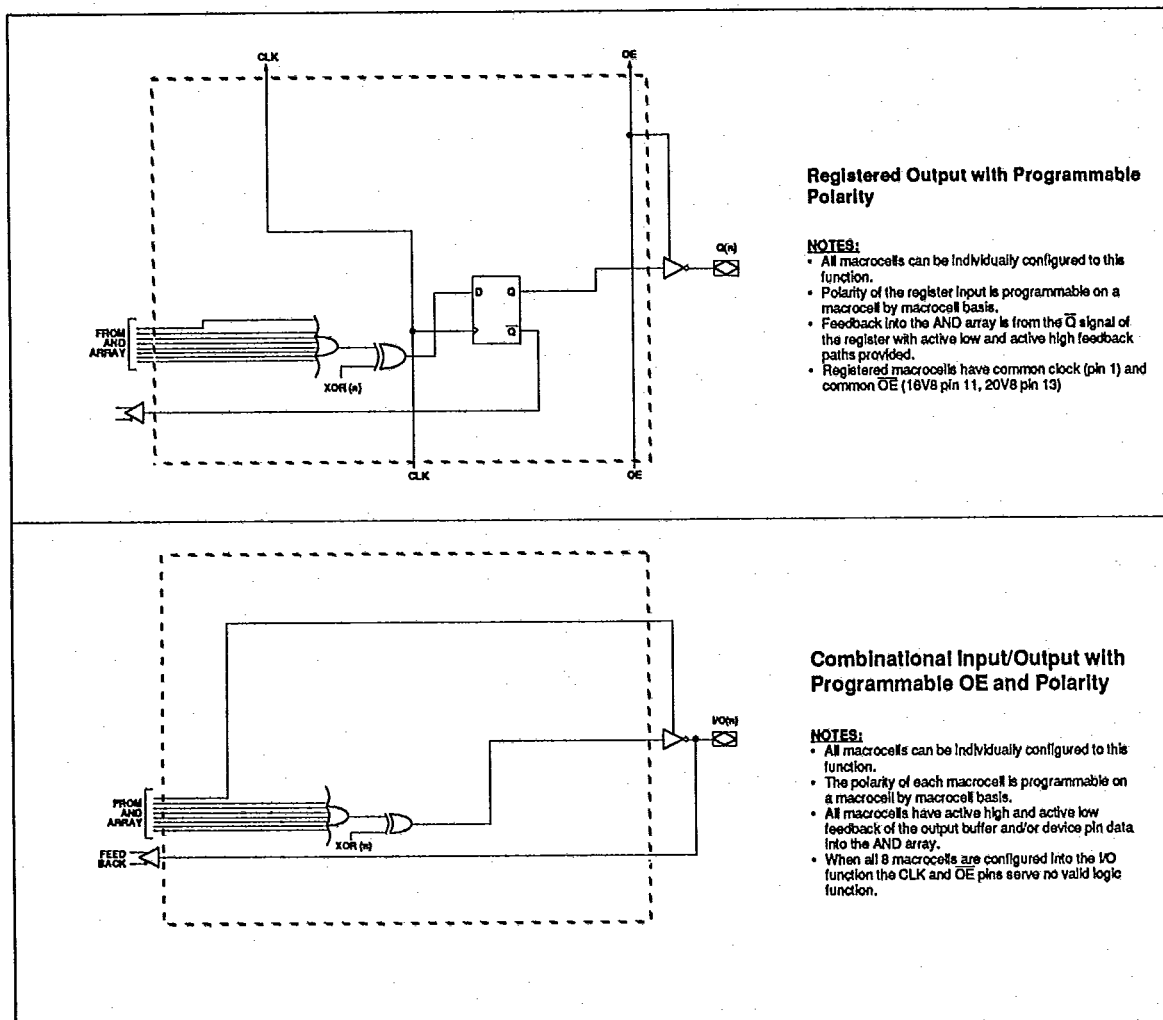
In the Registered architecture mode macrocells are configured as dedicated, registered outputs or as I/O functions.

Architecture configurations available in this mode are similar to the common 16R8, 20R6 and 16RP4 devices with various permutations of polarity, I/O and register placement.

All registered macrocells share common clock and  $\overline{OE}$  control pins. Any macrocell can be configured as registered or I/O. Up to 8 registers or up to 8 I/O's are possible in this mode. Dedicated input or output functions can be implemented as sub-sets of the I/O function.

Registered outputs have 8 data product terms per output. I/O's have 7 data product terms per output.

2



Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.



# Specifications GAL16V8A GAL20V8A

## COMPLEX MODE

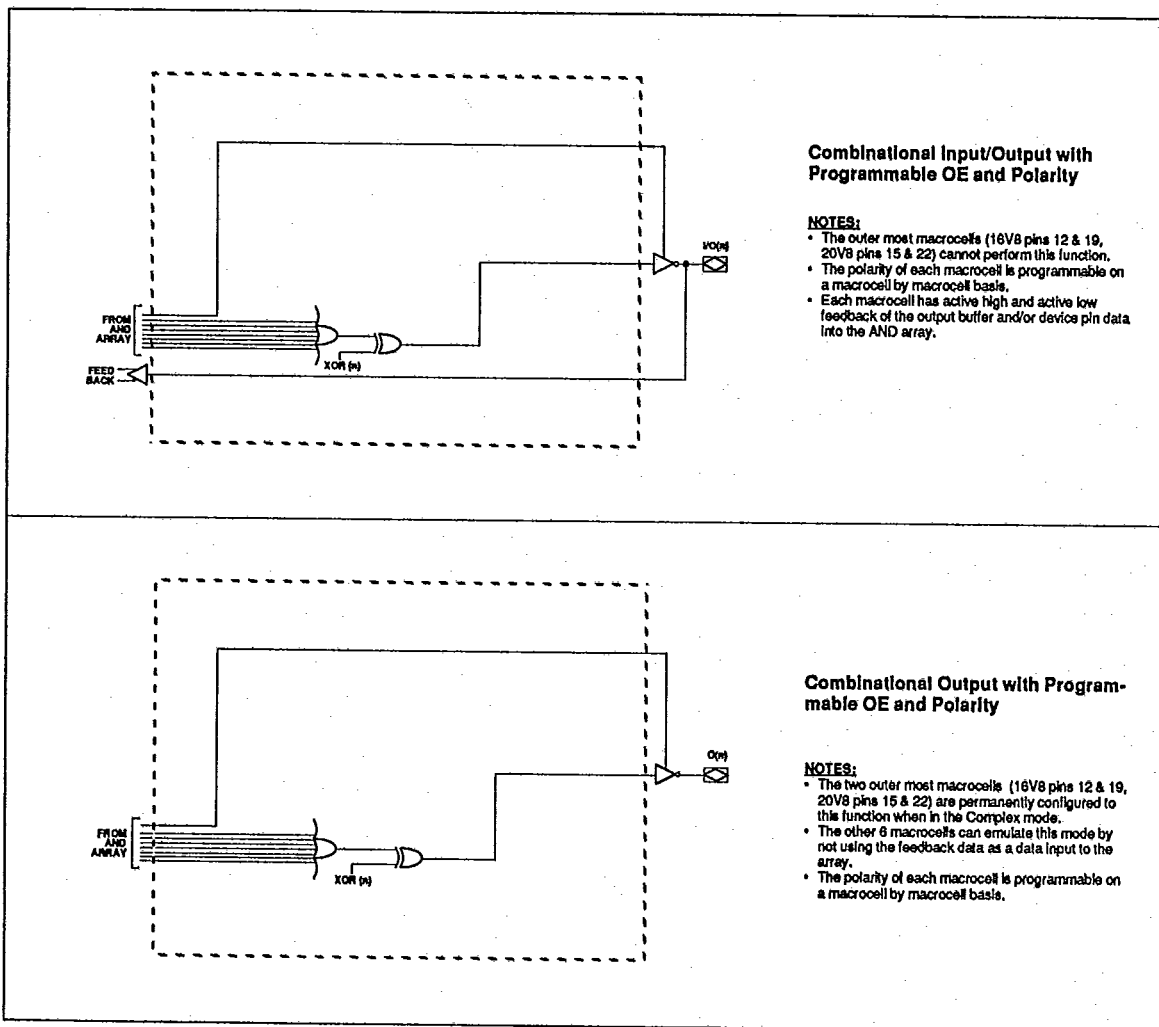
In the Complex architecture mode macrocells are configured as output only or I/O functions.

Architecture configurations available in this mode are similar to the common 16L8, 20L8 and 16P8 devices with programmable polarity in each macrocell.

Up to 6 I/O's are possible in this mode. Dedicated inputs or out-

puts can be implemented as sub-sets of the I/O function. The two "outboard" macrocells do not have input capability. Designs requiring 8 I/O's can be implemented in the Registered mode.

All macrocells have 7 data product terms per output. One product term is used for programmable OE control. Pins 1 and 11 on a GAL16V8A, and pins 1 and 13 on a GAL20V8A, are always available as data inputs into the AND array.



Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.





# Specifications GAL16V8A GAL20V8A

## SIMPLE MODE

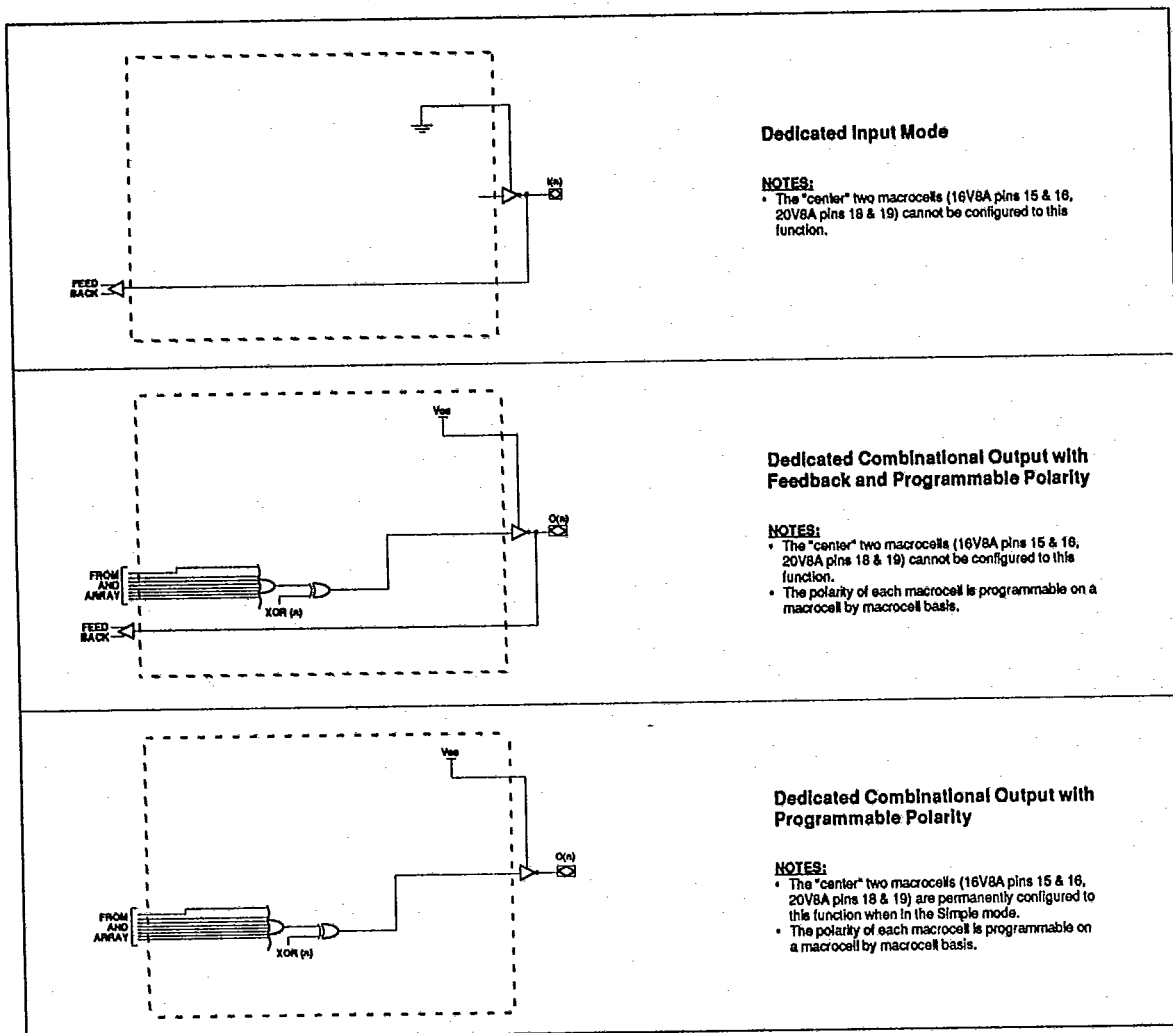
In the Simple architecture mode pins are configured as dedicated inputs or as dedicated, always active, combinational outputs.

Architecture configurations available in this mode are similar to the common 10L8, 18H4 and 16P6 devices with many permutations of generic polarity output or input choices.

All outputs are associated with 8 data product terms. In addition, each output has programmable polarity.

Pins 1 and 11 on a GAL16V8A, and pins 1 and 13 on a GAL20V8, are always available as data inputs into the AND array. The "center" two macrocells (GAL16V8A pins 15 & 16, GAL20V8A pins 18 & 19) cannot be used in the input configuration.

2



### Dedicated Input Mode

#### NOTES:

- The "center" two macrocells (16V8A pins 15 & 16, 20V8A pins 18 & 19) cannot be configured to this function.

### Dedicated Combinational Output with Feedback and Programmable Polarity

#### NOTES:

- The "center" two macrocells (16V8A pins 15 & 16, 20V8A pins 18 & 19) cannot be configured to this function.
- The polarity of each macrocell is programmable on a macrocell by macrocell basis.

### Dedicated Combinational Output with Programmable Polarity

#### NOTES:

- The "center" two macrocells (16V8A pins 15 & 16, 20V8A pins 18 & 19) are permanently configured to this function when in the Simple mode.
- The polarity of each macrocell is programmable on a macrocell by macrocell basis.

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.



## Specifications GAL16V8A GAL20V8A

### ELECTRONIC SIGNATURE

An electronic signature (ES) is provided with every GAL16V8A and GAL20V8A device. It contains 64 bits of reprogrammable memory that can contain user defined data. Some uses include user ID codes, revision numbers, or inventory control. The signature data is always available to the user independent of the state of the security cell.

**NOTE:** The ES is included in checksum calculations. Changing the ES will alter the checksum.

### SECURITY CELL

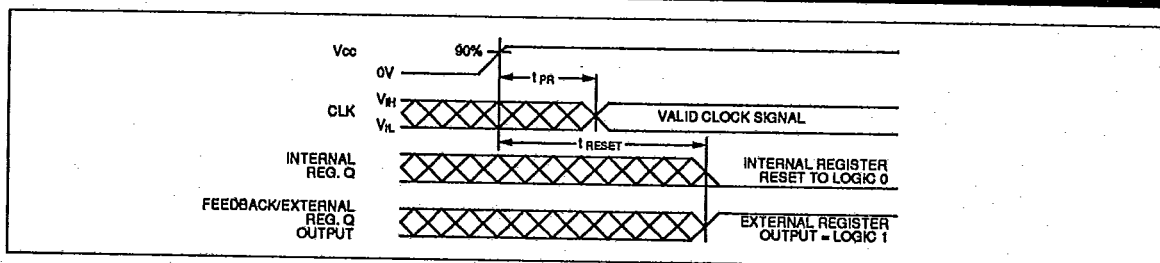
A security cell is provided with every GAL16V8A and GAL20V8A device as a deterrent to unauthorized copying of the array patterns. Once programmed, this cell prevents further read access to the AND array. This cell can be erased only during a bulk erase cycle, so the original configuration can never be examined once this cell is programmed. The Electronic Signature is always available to the user, regardless of the state of this control cell.

### INPUT BUFFERS

GAL16V8A and GAL20V8A devices are designed with TTL level compatible input buffers. These buffers, with their characteristically high impedance, load driving logic much less than traditional bipolar devices. This allows for a greater fan out from the driving logic.

GAL16V8A and GAL20V8A devices do not possess active pull-ups within their input structures. As a result, Lattice recommends that all unused inputs and tri-stated I/O pins be connected to another active input,  $V_{CC}$ , or GND. Doing this will tend to improve noise immunity and reduce  $I_{CC}$  for the device.

### POWER-UP RESET



Circuitry within the GAL16V8A and GAL20V8A provides a reset signal to all registers during power-up. All internal registers will have their Q outputs set low after a specified time ( $t_{RESET}$ , 45 $\mu$ s MAX). As a result, the state on the registered output pins (if they are enabled through OE) will always be high on power-up, regardless of the programmed polarity of the output pins. This feature can greatly simplify state machine design by providing a known state on power-up.

### OUTPUT REGISTER PRELOAD

When testing state machine designs, all possible states and state transitions must be verified in the design, not just those required in the normal machine operations. This is because in system operation, certain events occur that may throw the logic into an illegal state (power-up, line voltage glitches, brown-outs, etc.). To test a design for proper treatment of these conditions, a way must be provided to break the feedback paths, and force any desired (i.e., illegal) state into the registers. Then the machine can be sequenced and the outputs tested for correct next state conditions.

GAL16V8A and GAL20V8A devices include circuitry that allows each registered output to be synchronously set either high or low. Thus, any present state condition can be forced for test sequencing. If necessary, approved GAL programmers capable of executing test vectors perform output register preload automatically.

### LATCH-UP PROTECTION

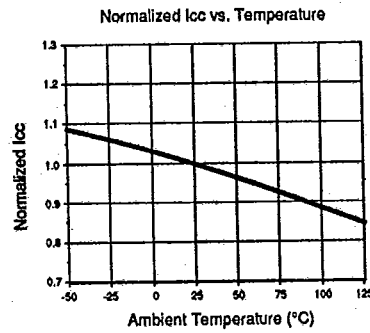
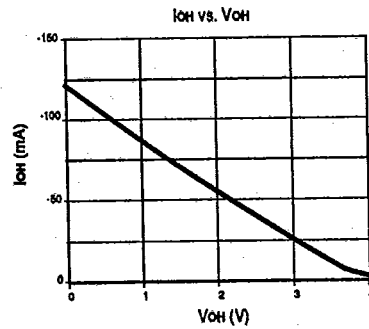
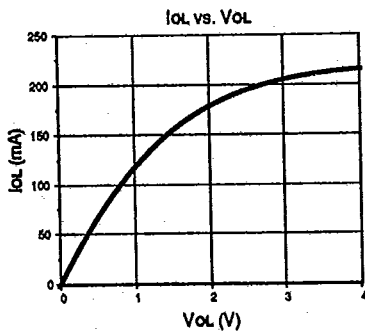
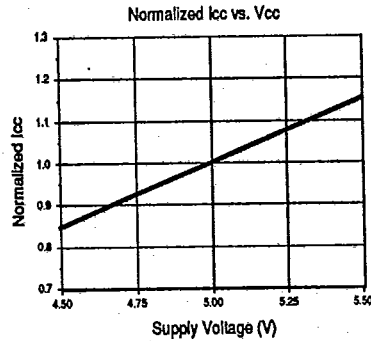
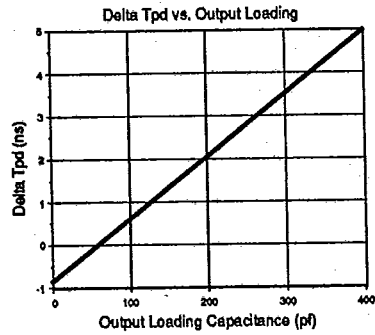
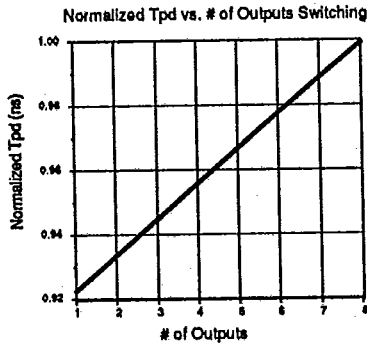
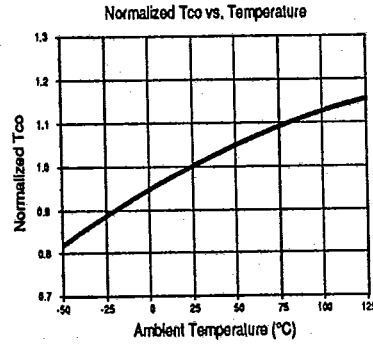
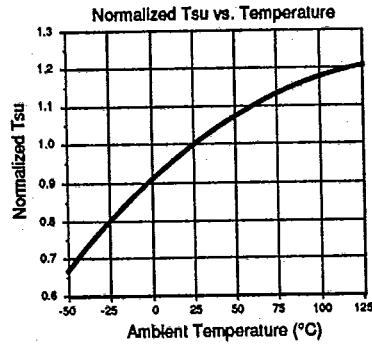
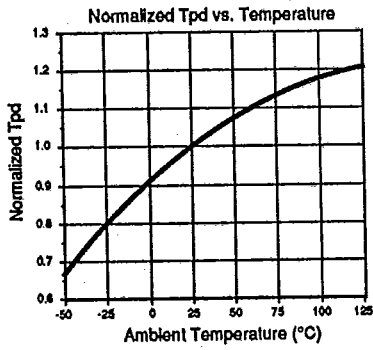
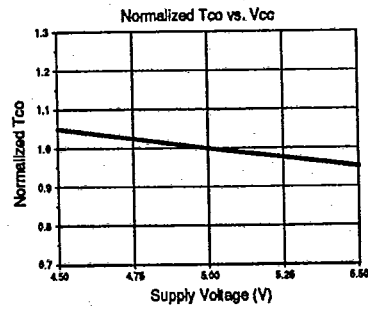
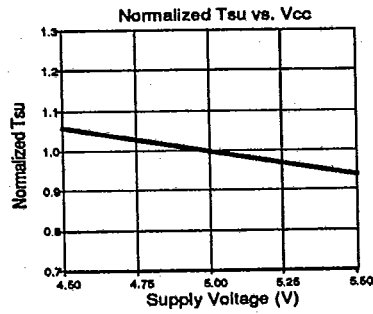
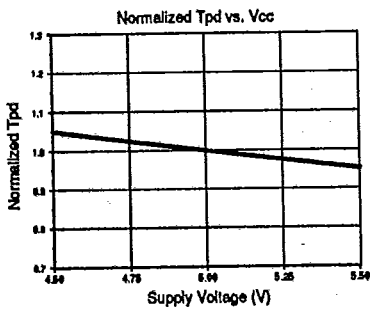
GAL16V8A and GAL20V8A devices are designed with an on-board charge pump to negatively bias the substrate. The negative bias is of sufficient magnitude to prevent input undershoots from causing the circuitry to latch. Additionally, outputs are designed with n-channel pull-up instead of the traditional p-channel pullups to eliminate any possibility of SCR induced latching.

### BULK ERASE MODE

Before writing a new pattern into a previously programmed part, the old pattern must first be erased. This erasure is done automatically by the programming hardware as part of the programming cycle and takes only 50 milliseconds.



2

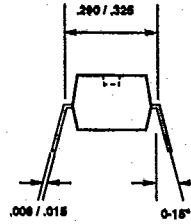
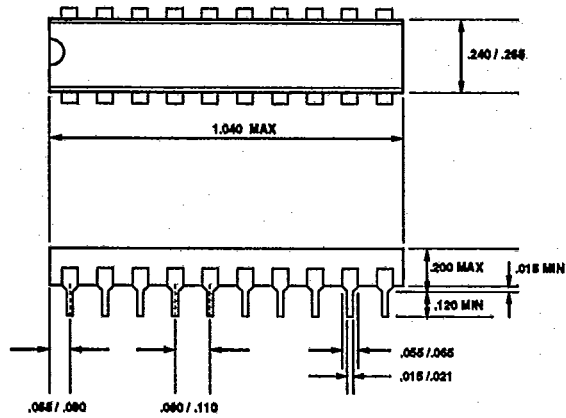


# PACKAGE DIAGRAMS

T-90-20

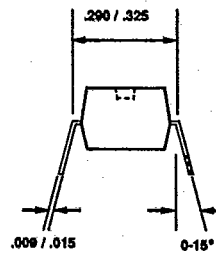
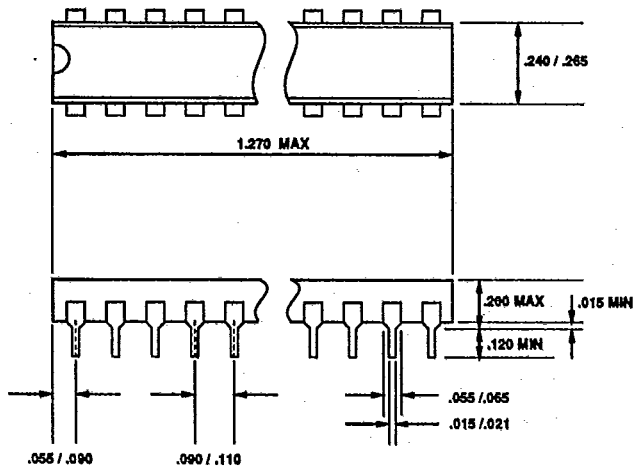
## 20-Pin Plastic DIP

Dimensions in Inches MIN. / MAX.



## 24-Pin Plastic DIP

Dimensions in Inches MIN. / MAX.



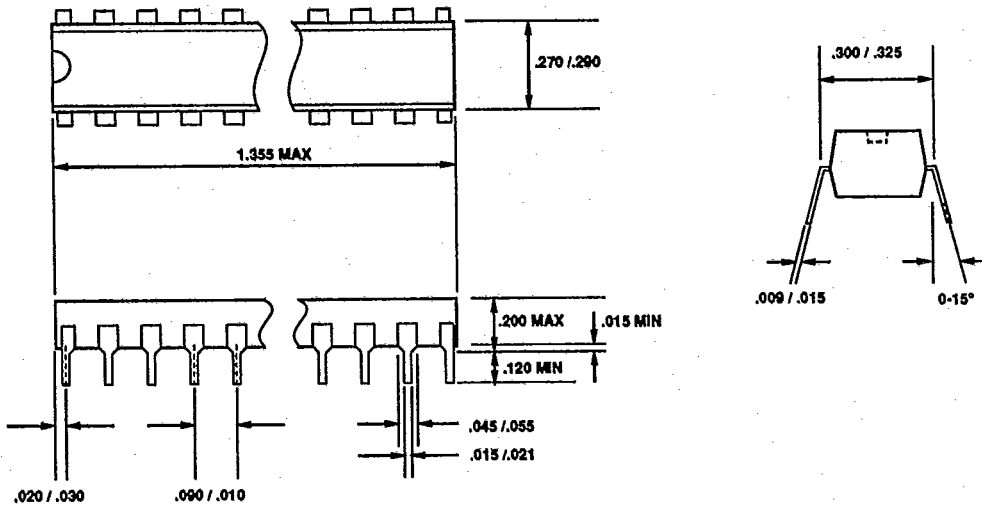


# Package Diagrams

T-90-20

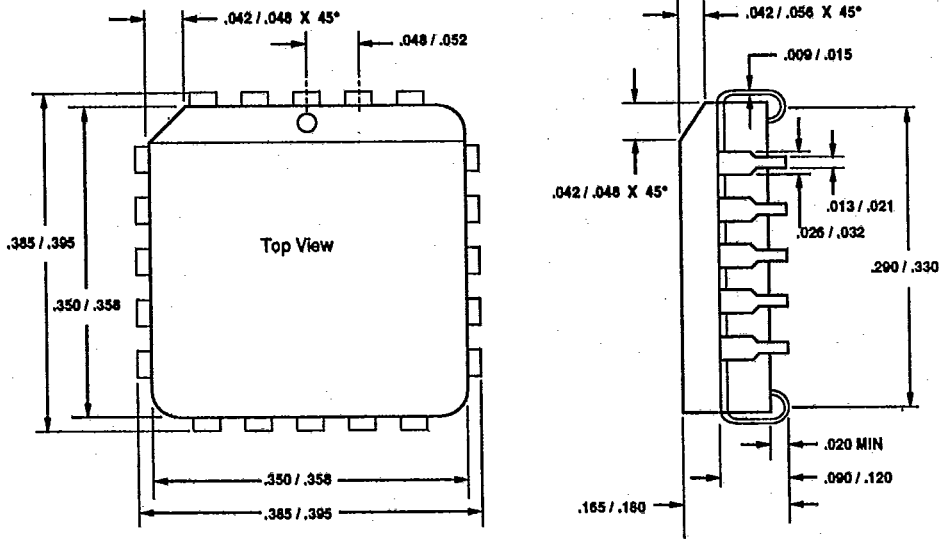
## 28-Pin Plastic DIP

Dimensions in Inches MIN. / MAX.



## 20-Pin PLCC Package

Dimensions in Inches MIN. / MAX.

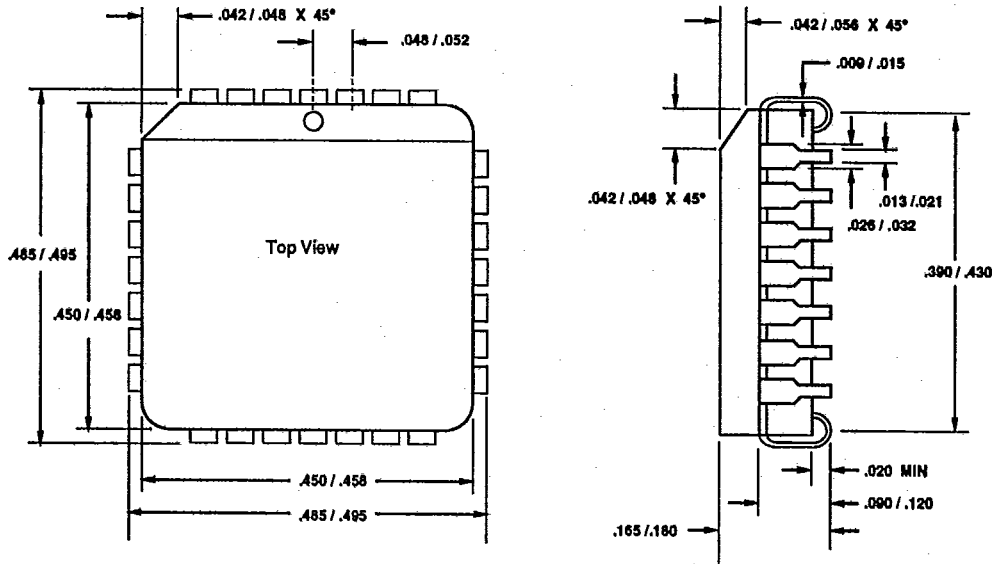


6



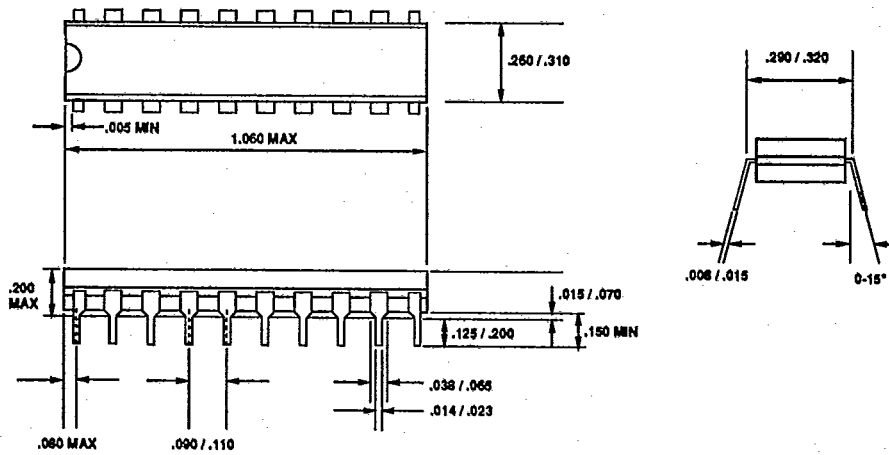
**28-Pin PLCC Package**

Dimensions in Inches MIN. / MAX.



**20-Pin (300 MIL) Cerdip**

Dimensions in Inches MIN. / MAX.





**24-Pin (300 MIL) CERDIP**

Dimensions in Inches MIN. / MAX.

