

MC74AC373, MC74ACT373

Octal Transparent Latch with 3-State Outputs

The MC74AC373/74ACT373 consists of eight latches with 3-state outputs for bus organized system applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup time is latched. Data appears on the bus when the Output Enable (\overline{OE}) is LOW. When \overline{OE} is HIGH, the bus output is in the high impedance state.

- Eight Latches in a Single Package
- 3-State Outputs for Bus Interfacing
- Outputs Source/Sink 24 mA
- 'ACT373 Has TTL Compatible Inputs

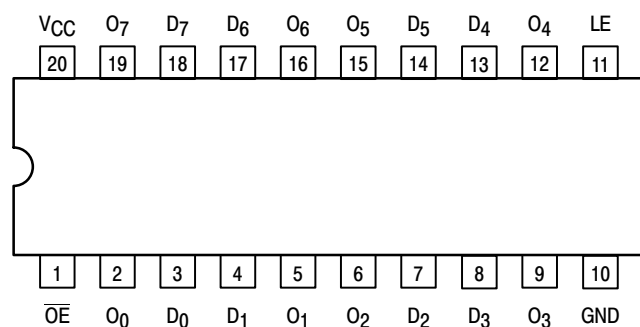


Figure 1. Pinout: 20-Lead Packages Conductors (Top View)

PIN ASSIGNMENT

PIN	FUNCTION
D ₀ –D ₇	Data Inputs
LE	Latch Enable Input
\overline{OE}	Output Enable Input
O ₀ –O ₇	3-State Latch Outputs

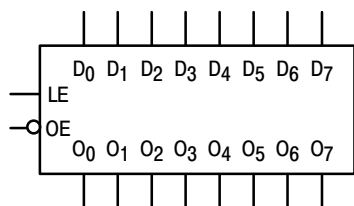
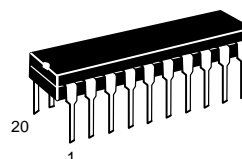


Figure 2. Logic Symbol

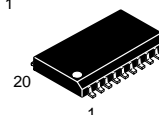


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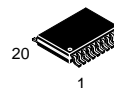
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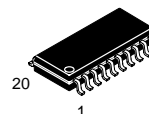
PDIP-20
N SUFFIX
CASE 738



SO-20
DW SUFFIX
CASE 751



TSSOP-20
DT SUFFIX
CASE 948E



EIAJ-20
M SUFFIX
CASE 967

ORDERING INFORMATION

Device	Package	Shipping
MC74AC373N	PDIP-20	18 Units/Rail
MC74ACT373N	PDIP-20	18 Units/Rail
MC74AC373DW	SOIC-20	38 Units/Rail
MC74AC373DWR2	SOIC-20	1000 Tape & Reel
MC74ACT373DW	SOIC-20	38 Units/Rail
MC74ACT373DWR2	SOIC-20	1000 Tape & Reel
MC74AC373DT	TSSOP-20	75 Units/Rail
MC74AC373DTR2	TSSOP-20	2500 Tape & Reel
MC74ACT373DT	TSSOP-20	75 Units/Rail
MC74ACT373DTR2	TSSOP-20	2500 Tape & Reel
MC74AC373M	EIAJ-20	40 Units/Rail
MC74AC373MEL	EIAJ-20	2000 Tape & Reel
MC74ACT373M	EIAJ-20	40 Units/Rail
MC74ACT373MEL	EIAJ-20	2000 Tape & Reel

DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 238 of this data sheet.

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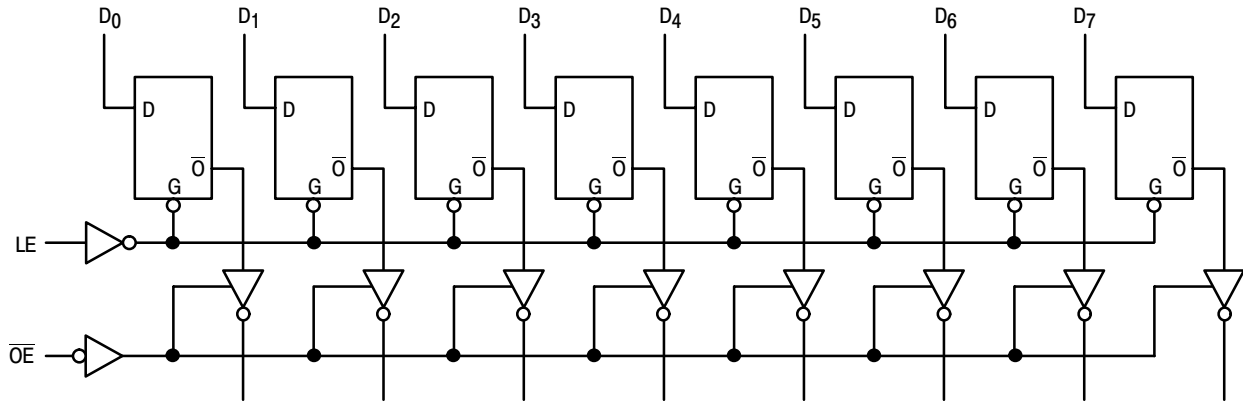
TRUTH TABLE

Inputs			Outputs
\overline{OE}	LE	D_n	O_n
H	X	X	Z
L	H	L	L
L	H	H	H
L	L	X	O_0

H = HIGH Voltage Level
 L = LOW Voltage Level
 Z = High Impedance
 X = Immaterial
 O_0 = Previous O_0 before LOW-to-HIGH Transition of Clock

FUNCTIONAL DESCRIPTION

The MC74AC373/74ACT373 contains eight D-type latches with 3-state standard outputs. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW, the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The 3-state standard outputs are controlled by the Output Enable (\overline{OE}) input. When \overline{OE} is LOW, the standard outputs are in the 2-state mode. When \overline{OE} is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.



NOTE: This diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Figure 3. Logic Diagram

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MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V _{IN}	DC Input Voltage (Referenced to GND)	-0.5 to V _{CC} +0.5	V
V _{OUT}	DC Output Voltage (Referenced to GND)	-0.5 to V _{CC} +0.5	V
I _{IN}	DC Input Current, per Pin	±20	mA
I _{OUT}	DC Output Sink/Source Current, per Pin	±50	mA
I _{CC}	DC V _{CC} or GND Current per Output Pin	±50	mA
T _{stg}	Storage Temperature	-65 to +150	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit	
V _{CC}	Supply Voltage	'AC	2.0	5.0	6.0	V
		'ACT	4.5	5.0	5.5	
V _{IN} , V _{OUT}	DC Input Voltage, Output Voltage (Ref. to GND)	0	-	V _{CC}	V	
t _r , t _f	Input Rise and Fall Time (Note 1) 'AC Devices except Schmitt Inputs	V _{CC} @ 3.0 V	-	150	-	ns/V
		V _{CC} @ 4.5 V	-	40	-	
		V _{CC} @ 5.5 V	-	25	-	
t _r , t _f	Input Rise and Fall Time (Note 2) 'ACT Devices except Schmitt Inputs	V _{CC} @ 4.5 V	-	10	-	ns/V
		V _{CC} @ 5.5 V	-	8.0	-	
T _J	Junction Temperature (PDIP)	-	-	140	°C	
T _A	Operating Ambient Temperature Range	-40	25	85	°C	
I _{OH}	Output Current – High	-	-	-24	mA	
I _{OL}	Output Current – Low	-	-	24	mA	

1. V_{IN} from 30% to 70% V_{CC}; see individual Data Sheets for devices that differ from the typical input rise and fall times.
2. V_{IN} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

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DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74AC		74AC		Unit	Conditions
			T _A = +25°C		T _A = -40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1		V	V _{OUT} = 0.1 V or V _{CC} - 0.1 V
		4.5	2.25	3.15	3.15			
		5.5	2.75	3.85	3.85			
V _{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9		V	V _{OUT} = 0.1 V or V _{CC} - 0.1 V
		4.5	2.25	1.35	1.35			
		5.5	2.75	1.65	1.65			
V _{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9		V	I _{OUT} = -50 μA
		4.5	4.49	4.4	4.4			
		5.5	5.49	5.4	5.4			
		3.0	-	2.56	2.46		V	*V _{IN} = V _{IL} or V _{IH} -12 mA I _{OH} -24 mA -24 mA
		4.5	-	3.86	3.76			
		5.5	-	4.86	4.76			
V _{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1		V	I _{OUT} = 50 μA
		4.5	0.001	0.1	0.1			
		5.5	0.001	0.1	0.1			
		3.0	-	0.36	0.44		V	*V _{IN} = V _{IL} or V _{IH} 12 mA I _{OL} 24 mA 24 mA
		4.5	-	0.36	0.44			
		5.5	-	0.36	0.44			
I _{IN}	Maximum Input Leakage Current	5.5	-	±0.1	±1.0		μA	V _I = V _{CC} , GND
I _{OZ}	Maximum 3-State Current	5.5	-	±0.5	±5.0		μA	V _I (OE) = V _{IL} , V _{IH} V _I = V _{CC} , GND V _O = V _{CC} , GND
I _{OLD}	†Minimum Dynamic Output Current	5.5	-	-	75		mA	V _{OLD} = 1.65 V Max
I _{OHD}		5.5	-	-	-75		mA	V _{OHD} = 3.85 V Min
I _{CC}	Maximum Quiescent Supply Current	5.5	-	8.0	80		μA	V _{IN} = V _{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

NOTE: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}.

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AC CHARACTERISTICS (For Figures and Waveforms – See Section 3 of the ON Semiconductor FACT Data Book, DL138/D)

Symbol	Parameter	V _{CC} * (V)	74AC			74AC		Unit	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
t _{PLH}	Propagation Delay D _n to O _n	3.3 5.0	1.5 1.5	10 7.0	13.5 9.5	1.5 1.5	15 10.5	ns	3-5
t _{PHL}	Propagation Delay D _n to O _n	3.3 5.0	1.5 1.5	9.5 7.0	13 9.5	1.5 1.5	14.5 10.5	ns	3-5
t _{PLH}	Propagation Delay LE to O _n	3.3 5.0	1.5 1.5	10 7.5	13.5 9.5	1.5 1.5	15 10.5	ns	3-6
t _{PHL}	Propagation Delay LE to O _n	3.3 5.0	1.5 1.5	9.5 7.0	12.5 9.5	1.5 1.5	14 10.5	ns	3-6
t _{PZH}	Output Enable Time	3.3 5.0	1.5 1.5	9.0 7.0	11.5 8.5	1.0 1.0	13 9.5	ns	3-7
t _{PZL}	Output Enable Time	3.3 5.0	1.5 1.5	8.5 6.5	11.5 8.5	1.0 1.0	13 9.5	ns	3-8
t _{PHZ}	Output Disable Time	3.3 5.0	1.5 1.5	10 8.0	12.5 11	1.0 1.0	14.5 12.5	ns	3-7
t _{PLZ}	Output Disable Time	3.3 5.0	1.5 1.5	8.0 6.5	11.5 8.5	1.0 1.0	12.5 10	ns	3-8

*Voltage Range 3.3 V is 3.3 V ±0.3 V.
Voltage Range 5.0 V is 5.0 V ±0.5 V.

AC OPERATING REQUIREMENTS

Symbol	Parameter	V _{CC} * (V)	74AC		74AC		Unit	Fig. No.
			T _A = +25°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF			
			Typ	Guaranteed Minimum				
t _s	Setup Time, HIGH or LOW D _n to LE	3.3 5.0	3.5 2.0	5.5 4.0	6.0 4.5	ns	3-9	
t _h	Hold Time, HIGH or LOW D _n to LE	3.3 5.0	-3.0 -1.5	1.0 1.0	1.0 1.0	ns	3-9	
t _w	LE Pulse Width, HIGH	3.3 5.0	4.0 2.0	5.5 4.0	6.0 4.5	ns	3-6	

*Voltage Range 3.3 V is 3.3 V ±0.3 V.
Voltage Range 5.0 V is 5.0 V ±0.5 V.

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DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74ACT		74ACT		Unit	Conditions
			T _A = +25°C		T _A = -40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	4.5	1.5	2.0	2.0		V	V _{OUT} = 0.1 V or V _{CC} - 0.1 V
		5.5	1.5	2.0	2.0			
V _{IL}	Maximum Low Level Input Voltage	4.5	1.5	0.8	0.8		V	V _{OUT} = 0.1 V or V _{CC} - 0.1 V
		5.5	1.5	0.8	0.8			
V _{OH}	Minimum High Level Output Voltage	4.5	4.49	4.4	4.4		V	I _{OUT} = -50 μA
		5.5	5.49	5.4	5.4			
		4.5	-	3.86	3.76		V	*V _{IN} = V _{IL} or V _{IH} -24 mA I _{OH} -24 mA
		5.5	-	4.86	4.76			
V _{OL}	Maximum Low Level Output Voltage	4.5	0.001	0.1	0.1		V	I _{OUT} = 50 μA
		5.5	0.001	0.1	0.1			
		4.5	-	0.36	0.44		V	*V _{IN} = V _{IL} or V _{IH} 24 mA I _{OL} 24 mA
		5.5	-	0.36	0.44			
I _{IN}	Maximum Input Leakage Current	5.5	-	±0.1	±1.0		μA	V _I = V _{CC} , GND
ΔI _{CCCT}	Additional Max. I _{CC} /Input	5.5	0.6	-	1.5		mA	V _I = V _{CC} - 2.1 V
I _{OZ}	Maximum 3-State Current	5.5	-	±0.5	±5.0		μA	V _I (OE) = V _{IL} , V _{IH} V _I = V _{CC} , GND V _O = V _{CC} , GND
I _{OLD}	†Minimum Dynamic Output Current	5.5	-	-	75		mA	V _{OLD} = 1.65 V Max
I _{OHD}		5.5	-	-	-75		mA	V _{OHD} = 3.85 V Min
I _{CC}	Maximum Quiescent Supply Current	5.5	-	8.0	80		μA	V _{IN} = V _{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

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AC CHARACTERISTICS (For Figures and Waveforms – See Section 3 of the ON Semiconductor FACT Data Book, DL138/D)

Symbol	Parameter	V _{CC} * (V)	74ACT			74ACT		Unit	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
t _{PLH}	Propagation Delay D _n to O _n	5.0	2.5	8.5	10	1.5	11.5	ns	3-5
t _{PHL}	Propagation Delay D _n to O _n	5.0	2.0	8.0	10	1.5	11.5	ns	3-5
t _{PLH}	Propagation Delay LE to O _n	5.0	2.5	8.5	11	2.0	11.5	ns	3-6
t _{PHL}	Propagation Delay LE to O _n	5.0	2.0	8.0	10	1.5	11.5	ns	3-6
t _{PZH}	Output Enable Time	5.0	2.0	8.0	9.5	1.5	10.5	ns	3-7
t _{PZL}	Output Enable Time	5.0	2.0	7.5	9.0	1.5	10.5	ns	3-8
t _{PHZ}	Output Disable Time	5.0	2.5	9.0	11	2.5	12.5	ns	3-7
t _{PLZ}	Output Disable Time	5.0	1.5	7.5	8.5	1.0	10	ns	3-8

*Voltage Range 5.0 V is 5.0 V ±0.5 V.

AC OPERATING REQUIREMENTS

Symbol	Parameter	V _{CC} * (V)	74ACT		74ACT		Unit	Fig. No.
			T _A = +25°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF			
			Typ	Guaranteed Minimum				
t _s	Setup Time, HIGH or LOW D _n to LE	5.0	3.0	7.0	8.0	ns	3-9	
t _h	Hold Time, HIGH or LOW D _n to LE	5.0	0	0	1.0	ns	3-9	
t _w	LE Pulse Width, HIGH	5.0	2.0	7.0	8.0	ns	3-6	

*Voltage Range 5.0 V is 5.0 V ±0.5 V.

CAPACITANCE

Symbol	Parameter	Value Typ	Unit	Test Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = 5.0 V
C _{PD}	Power Dissipation Capacitance	40	pF	V _{CC} = 5.0 V

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MARKING DIAGRAMS

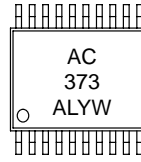
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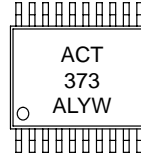
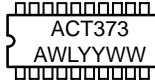
SO-20



TSSOP-20



EIAJ-20



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week