

## 74VCX16838

### Low Voltage 16-Bit Selectable Register/Buffer with 3.6V Tolerant Inputs and Outputs

#### General Description

The VCX16838 contains sixteen non-inverting selectable buffered or registered paths. The device can be configured to operate in a registered, or flow through buffer mode by utilizing the register enable (REGE) and Clock (CLK) signals. The device operates in a 16-bit word wide mode. All outputs can be placed into 3-State through use of the  $\overline{OE}$  Pin. These devices are ideally suited for buffered or registered 168 pin and 200 pin SDRAM DIMM memory modules.

The 74VCX16838 is designed for low voltage (1.65V to 3.6V)  $V_{CC}$  applications with I/O compatibility up to 3.6V.

The 74VCX16838 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining low CMOS power dissipation.

#### Features

- Compatible with PC100 and PC133 DIMM module specifications
- 1.65V–3.6V  $V_{CC}$  supply operation
- 3.6V tolerant inputs and outputs
- $t_{PD}$  (CLK to  $O_n$ )
  - 3.0 ns max for 3.0V to 3.6V  $V_{CC}$
  - 4.0 ns max for 2.3V to 2.7V  $V_{CC}$
  - 8.0 ns max for 1.65V to 1.95V  $V_{CC}$
- Power-off high impedance inputs and outputs
- Supports live insertion and withdrawal (Note 1)
- Static Drive ( $I_{OH}/I_{OL}$ )
  - ±24 mA @ 3.0V  $V_{CC}$
  - ±18 mA @ 2.3V  $V_{CC}$
  - ±6 mA @ 1.65V  $V_{CC}$
- Uses patented noise/EMI reduction circuitry
- Ideal for SDRAM DIMM modules
- Latch-up performance exceeds 300 mA
- ESD performance:
  - Human body model > 2000V
  - Machine model > 200V

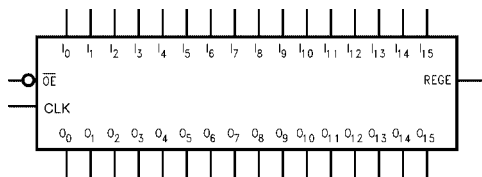
**Note 1:** To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pull-up resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

#### Ordering Code:

Order Number	Package Number	Package Description
74VCX16838MTD	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

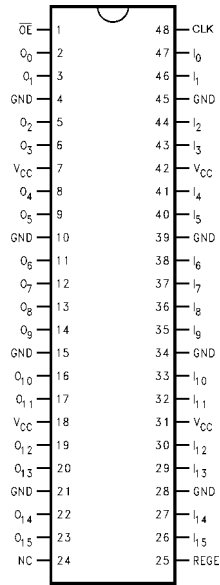
#### Logic Symbol



#### Pin Descriptions

Pin Names	Description
$\overline{OE}$	Output Enable Input (Active LOW)
$I_0$ – $I_{15}$	Inputs
$O_0$ – $O_{15}$	Outputs
CLK	Clock Input
REGE	Register Enable Input

**Connection Diagram**



**Truth Table**

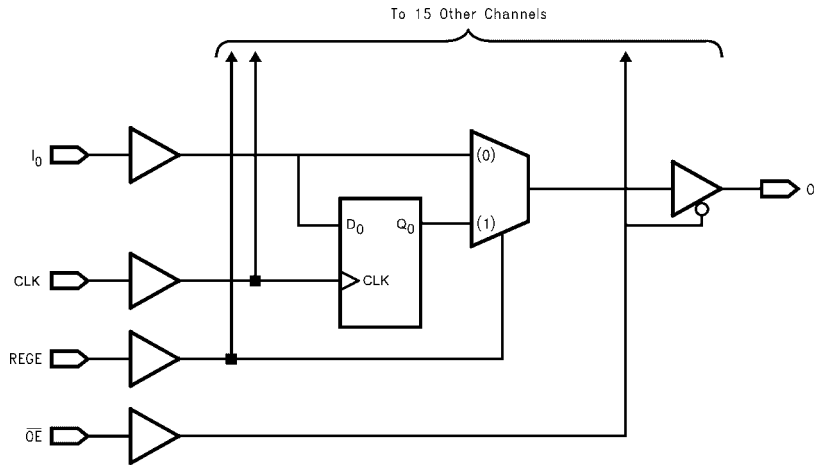
Inputs				Outputs
CLK	REGE	I <sub>n</sub>	$\overline{OE}$	O <sub>n</sub>
↑	H	H	L	H
↑	H	L	L	L
X	L	H	L	H
X	L	L	L	L
X	X	X	H	Z

H = Logic HIGH  
 L = Logic LOW  
 X = Don't Care, but not floating  
 Z = High Impedance  
 ↑ = LOW-to-HIGH Clock Transition

**Functional Description**

The 74VCX16838 consists of sixteen selectable non-inverting buffers or registers with word wide modes. Mode functionality is selected through operation of the CLK and REGE pin as shown by the truth table. When REGE is held at a logic HIGH the device operates as a 16-bit register. Data is transferred from I<sub>n</sub> to O<sub>n</sub> on the rising edge of the CLK input. When the REGE pin is held at a logic LOW the device operates in a flow through mode and data propagates directly from the I to the O outputs. All outputs can be 3-STATE by holding the OE pin at a logic HIGH.

**Logic Diagram**



**Absolute Maximum Ratings** (Note 2)

Supply Voltage ( $V_{CC}$ )	-0.5V to +4.6V
DC Input Voltage ( $V_I$ )	-0.5V to +4.6V
Output Voltage ( $V_O$ )	
Outputs 3-STATE	-0.5V to +4.6V
Outputs Active (Note 3)	-0.5V to $V_{CC}$ +0.5V
DC Input Diode Current ( $I_{IK}$ ) $V_I < 0V$	-50 mA
DC Output Diode Current ( $I_{OK}$ )	
$V_O < 0V$	-50 mA
$V_O > V_{CC}$	+50 mA
DC Output Source/Sink Current ( $I_{OH}/I_{OL}$ )	$\pm 50$ mA
DC $V_{CC}$ or GND Current per Supply Pin ( $I_{CC}$ or GND)	$\pm 100$ mA
Storage Temperature Range ( $T_{STG}$ )	-65°C to +150°C

**Recommended Operating Conditions** (Note 4)

Power Supply	
Operating	1.65V to 3.6V
Data Retention Only	1.2V to 3.6V
Input Voltage	-0.3V to +3.6V
Output Voltage ( $V_O$ )	
Output in Active States	0V to $V_{CC}$
Output in "OFF" State	0V to 3.6V
Output Current in $I_{OH}/I_{OL}$	
$V_{CC} = 3.0V$ to 3.6V	$\pm 24$ mA
$V_{CC} = 2.3V$ to 2.7V	$\pm 18$ mA
$V_{CC} = 1.65V$ to 2.3V	$\pm 6$ mA
Free Air Operating Temperature ( $T_A$ )	-40°C to +85°C
Minimum Input Edge Rate ( $\Delta t/\Delta V$ )	
$V_{IN} = 0.8V$ to 2.0V, $V_{CC} = 3.0V$	10 ns/V

**Note 2:** The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Note 3:**  $I_O$  Absolute Maximum Rating must be observed.

**Note 4:** Floating or unused inputs must be held HIGH or LOW.

**DC Electrical Characteristics (2.7V <  $V_{CC}$  ≤ 3.6V)**

Symbol	Parameter	Conditions	$V_{CC}$ (V)	Min	Max	Units
$V_{IH}$	HIGH Level Input Voltage		2.7-3.6	2.0		V
$V_{IL}$	LOW Level Input Voltage		2.7-3.6		0.8	V
$V_{OH}$	HIGH Level Output Voltage	$I_{OH} = -100 \mu A$	2.7-3.6	$V_{CC} - 0.2$		V
		$I_{OH} = -12 \text{ mA}$	2.7	2.2		
		$I_{OH} = -18 \text{ mA}$	3.0	2.4		
		$I_{OH} = -24 \text{ mA}$	3.0	2.2		
$V_{OL}$	LOW Level Output Voltage	$I_{OL} = 100 \mu A$	2.7-3.6		0.2	V
		$I_{OL} = 12 \text{ mA}$	2.7		0.4	
		$I_{OL} = 18 \text{ mA}$	3.0		0.4	
		$I_{OL} = 24 \text{ mA}$	3.0		0.55	
$I_I$	Input Leakage Current	$0V \leq V_I \leq 3.6V$	2.7-3.6		$\pm 5.0$	$\mu A$
$I_{OZ}$	3-STATE Output Leakage	$0V \leq V_O \leq 3.6V$ $V_I = V_{IH}$ or $V_{IL}$	2.7-3.6		$\pm 10$	$\mu A$
$I_{OFF}$	Power-OFF Leakage Current	$0V \leq (V_I, V_O) \leq 3.6V$	0		10	$\mu A$
$I_{CC}$	Quiescent Supply Current	$V_I = V_{CC}$ or GND	2.7-3.6		20	$\mu A$
		$V_{CC} \leq (V_I, V_O) \leq 3.6V$ (Note 5)		$\pm 20$		
$\Delta I_{CC}$	Increase in $I_{CC}$ per Input	$V_{IH} = V_{CC} - 0.6V$	2.7-3.6		750	$\mu A$

**Note 5:** Outputs disabled or 3-STATE only.

### DC Electrical Characteristics ( $2.3V \leq V_{CC} \leq 2.7V$ )

Symbol	Parameter	Conditions	V <sub>CC</sub> (V)	Min	Max	Units
V <sub>IH</sub>	HIGH Level Input Voltage		2.3-2.7	1.6		V
V <sub>IL</sub>	LOW Level Input Voltage		2.3-2.7		0.7	V
V <sub>OH</sub>	HIGH Level Output Voltage	I <sub>OH</sub> = -100 μA	2.3-2.7	V <sub>CC</sub> - 0.2		V
		I <sub>OH</sub> = -6 mA	2.3	2.0		
		I <sub>OH</sub> = -12 mA	2.3	1.8		
		I <sub>OH</sub> = -18 mA	2.3	1.7		
V <sub>OL</sub>	LOW Level Output Voltage	I <sub>OL</sub> = 100 μA	2.3-2.7		0.2	V
		I <sub>OL</sub> = 12 mA	2.3		0.4	
		I <sub>OL</sub> = 18 mA	2.3		0.6	
I <sub>I</sub>	Input Leakage Current	0V ≤ V <sub>I</sub> ≤ 3.6V	2.3-2.7		±5.0	μA
I <sub>OZ</sub>	3-STATE Output Leakage	0V ≤ V <sub>O</sub> ≤ 3.6V V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	2.3-2.7		±10	μA
I <sub>OFF</sub>	Power-OFF Leakage Current	0V ≤ (V <sub>I</sub> , V <sub>O</sub> ) ≤ 3.6V	0		10	μA
I <sub>CC</sub>	Quiescent Supply Current	V <sub>I</sub> = V <sub>CC</sub> or GND	2.3-2.7		20	μA
		V <sub>CC</sub> ≤ (V <sub>I</sub> , V <sub>O</sub> ) ≤ 3.6V (Note 6)			±20	

Note 6: Outputs disabled or 3-STATE only.

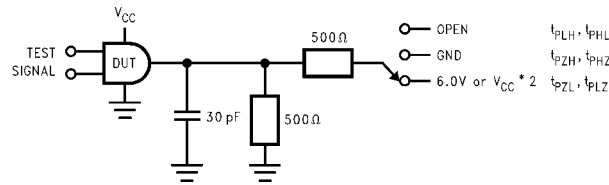
### DC Electrical Characteristics ( $1.65V \leq V_{CC} < 2.3V$ )

Symbol	Parameter	Conditions	V <sub>CC</sub> (V)	Min	Max	Units
V <sub>IH</sub>	HIGH Level Input Voltage		1.65 - 2.3	0.65 × V <sub>CC</sub>		V
V <sub>IL</sub>	LOW Level Input Voltage		1.65 - 2.3		0.35 × V <sub>CC</sub>	V
V <sub>OH</sub>	HIGH Level Output Voltage	I <sub>OH</sub> = -100 μA	1.65 - 2.3	V <sub>CC</sub> - 0.2		V
		I <sub>OH</sub> = -6 mA	1.65	1.25		
V <sub>OL</sub>	LOW Level Output Voltage	I <sub>OL</sub> = 100 μA	1.65 - 2.3		0.2	V
		I <sub>OL</sub> = 6 mA	1.65		0.3	
I <sub>I</sub>	Input Leakage Current	0V ≤ V <sub>I</sub> ≤ 3.6V	1.65 - 2.3		±5.0	μA
I <sub>OZ</sub>	3-STATE Output Leakage	0V ≤ V <sub>O</sub> ≤ 3.6V V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	1.65 - 2.3		±10	μA
I <sub>OFF</sub>	Power-OFF Leakage Current	0V ≤ (V <sub>I</sub> , V <sub>O</sub> ) ≤ 3.6V	0		10	μA
I <sub>CC</sub>	Quiescent Supply Current	V <sub>I</sub> = V <sub>CC</sub> or GND	1.65 - 2.3		20	μA
		V <sub>CC</sub> ≤ (V <sub>I</sub> , V <sub>O</sub> ) ≤ 3.6V (Note 7)			±20	

Note 7: Outputs disabled or 3-STATE only.

AC Electrical Characteristics (Note 8)								
Symbol	Parameter	$T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}, C_L = 30\text{ pF}, R_L = 500\Omega$						Units
		$V_{CC} = 3.3\text{V} \pm 0.3\text{V}$		$V_{CC} = 2.5\text{V} \pm 0.2\text{V}$		$V_{CC} = 1.8\text{V} \pm 0.15\text{V}$		
		Min	Max	Min	Max	Min	Max	
$f_{\text{MAX}}$	Maximum Clock Frequency	250		200		100		MHz
$t_{\text{PHL}}, t_{\text{PLH}}$	Propagation Delay $I_n$ to $O_n$ (REGE = 0)	0.8	2.5	1.0	3.5	1.5	7.0	ns
$t_{\text{PHL}}, t_{\text{PLH}}$	Propagation Delay CLK to $O_n$ (REGE = 1)	0.8	3.0	1.0	4.0	1.5	8.0	ns
$t_{\text{PHL}}, t_{\text{PLH}}$	Propagation Delay REGE to $O_n$	0.8	3.0	1.0	4.0	1.5	8.0	ns
$t_{\text{PZL}}, t_{\text{PZH}}$	Output Enable Time	0.8	3.5	1.0	4.7	1.5	9.4	ns
$t_{\text{PLZ}}, t_{\text{PHZ}}$	Output Disable Time	0.8	3.5	1.0	3.9	1.5	7.0	ns
$t_S$	Setup Time	1.0		1.0		2.5		ns
$t_H$	Hold Time	0.7		0.7		1.0		ns
$t_W$	Pulse Width	1.5		1.5		4.0		ns
$t_{\text{OSHL}}$	Output to Output Skew (Note 9)		0.5		0.5		0.75	ns
$t_{\text{OSLH}}$	(Note 9)							
<p><b>Note 8:</b> For <math>C_L = 50\text{pF}</math>, add approximately 300 ps to the AC maximum specification.</p> <p><b>Note 9:</b> Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (<math>t_{\text{OSHL}}</math>) or LOW-to-HIGH (<math>t_{\text{OSLH}}</math>).</p>								
Extended AC Electrical Characteristics (Note 10)								
Symbol	Parameter	$T_A = -0^{\circ}\text{C to } +85^{\circ}\text{C}, R_L = 500\Omega, V_{CC} = 3.3\text{V} \pm 0.3\text{V}$				Units		
		$C_L = 50\text{ pF}$						
		Min		Max				
$t_{\text{PHL}}, t_{\text{PLH}}$	Propagation Delay $I_n$ to $O_n$ (REGE = 0)	1.0		2.8		ns		
$t_{\text{PHL}}, t_{\text{PLH}}$	Propagation Delay CLK to $O_n$ (REGE = 1)	1.4		3.3		ns		
$t_{\text{PHL}}, t_{\text{PLH}}$	Propagation Delay REGE to $O_n$	1.0		3.3		ns		
$t_{\text{PZL}}, t_{\text{PZH}}$	Output Enable Time	1.0		3.8		ns		
$t_{\text{PLZ}}, t_{\text{PHZ}}$	Output Disable Time	1.0		3.8		ns		
$t_S$	Setup Time	1.0				ns		
$t_H$	Hold Time	0.7				ns		
<p><b>Note 10:</b> This parameter is guaranteed by characterization but not tested.</p>								
Dynamic Switching Characteristics								
Symbol	Parameter	Conditions	$V_{CC}$ (V)	$T_A = +25^{\circ}\text{C}$	Units			
				Typical				
$V_{\text{OLP}}$	Quiet Output Dynamic Peak $V_{\text{OL}}$	$C_L = 30\text{ pF}, V_{\text{IH}} = V_{\text{CC}}, V_{\text{IL}} = 0\text{V}$	1.8 2.5 3.3	0.25 0.6 0.8	V			
$V_{\text{OLV}}$	Quiet Output Dynamic Valley $V_{\text{OL}}$	$C_L = 30\text{ pF}, V_{\text{IH}} = V_{\text{CC}}, V_{\text{IL}} = 0\text{V}$	1.8 2.5 3.3	-0.25 -0.6 -0.8	V			
$V_{\text{OHV}}$	Quiet Output Dynamic Valley $V_{\text{OH}}$	$C_L = 30\text{ pF}, V_{\text{IH}} = V_{\text{CC}}, V_{\text{IL}} = 0\text{V}$	1.8 2.5 3.3	1.5 1.9 2.2	V			
Capacitance								
Symbol	Parameter	Conditions	$T_A = +25^{\circ}\text{C}$	Units				
			Typical					
$C_{\text{IN}}$	Input Capacitance	$V_{\text{CC}} = 1.8\text{V}, 2.5\text{V or } 3.3\text{V}, V_{\text{I}} = 0\text{V or } V_{\text{CC}}$	6	pF				
$C_{\text{OUT}}$	Output Capacitance	$V_{\text{I}} = 0\text{V or } V_{\text{CC}}, V_{\text{CC}} = 1.8\text{V}, 2.5\text{V or } 3.3\text{V}$	7	pF				
$C_{\text{PD}}$	Power Dissipation Capacitance	$V_{\text{I}} = 0\text{V or } V_{\text{CC}}, f = 10\text{ MHz}, V_{\text{CC}} = 1.8\text{V}, 2.5\text{V or } 3.3\text{V}$	20	pF				

AC Loading and Waveforms



TEST	SWITCH
$t_{PLH}, t_{PHL}$	Open
$t_{PZL}, t_{PLZ}$	6V at $V_{CC} = 3.3 \pm 0.3V$ ; $V_{CC} \times 2$ at $V_{CC} = 2.5 \pm 0.2V$ ; $1.8V \pm 0.15V$
$t_{PZH}, t_{PHZ}$	GND

FIGURE 1. AC Test Circuit

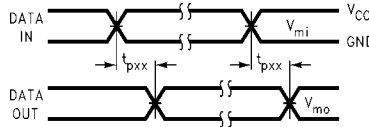


FIGURE 2. Waveform for Inverting and Non-Inverting Functions

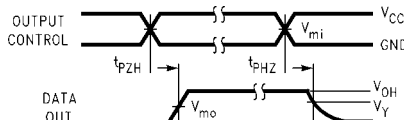


FIGURE 3. 3-STATE Output High Enable and Disable Times for Low Voltage Logic

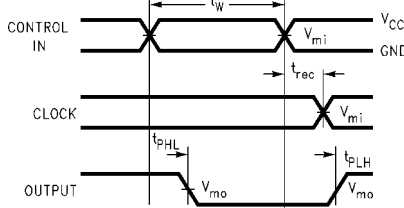


FIGURE 4. Propagation Delay, Pulse Width and  $t_{rec}$  Waveforms

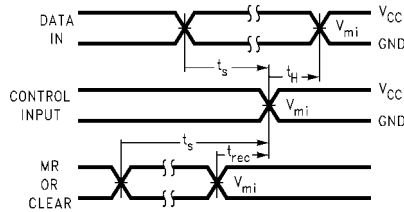
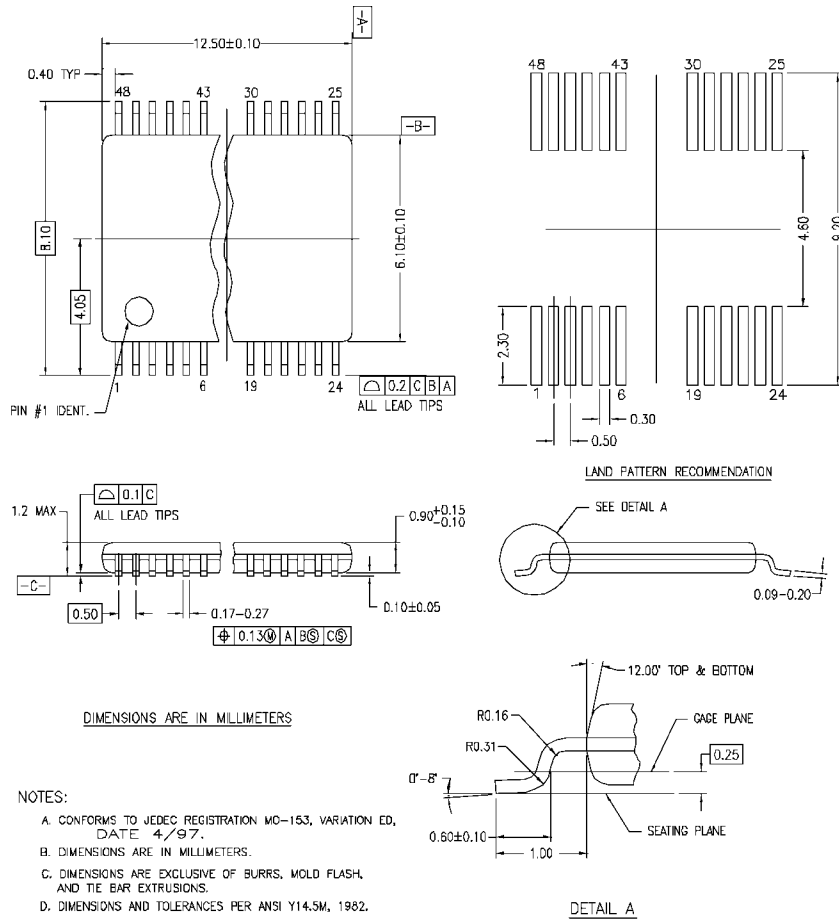


FIGURE 5. Setup Time, Hold Time and Recovery Time for Low Voltage Logic

Symbol	$V_{CC}$		
	$3.3V \pm 0.3V$	$2.5V \pm 0.2V$	$1.8V \pm 0.15V$
$V_{mi}$	1.5V	$V_{CC}/2$	$V_{CC}/2$
$V_{mo}$	1.5V	$V_{CC}/2$	$V_{CC}/2$
$V_X$	$V_{OL} + 0.3V$	$V_{OL} + 0.15V$	$V_{OL} + 0.15V$
$V_Y$	$V_{OH} - 0.3V$	$V_{OH} - 0.15V$	$V_{OH} - 0.15V$

**Physical Dimensions** inches (millimeters) unless otherwise noted



MTD48REVC

**48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide Package Number MTD48**

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

**LIFE SUPPORT POLICY**

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

[www.fairchildsemi.com](http://www.fairchildsemi.com)