

74LVC1G34

Single buffer

Rev. 5 — 2 July 2012

Product data sheet

1. General description

The 74LVC1G34 provides a low-power, low-voltage single buffer.

The input can be driven from either 3.3 V or 5 V devices. This feature allows the use of this device in a mixed 3.3 V and 5 V environment.

This device is fully specified for partial power-down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

Schmitt trigger action at all inputs makes the circuit highly tolerant of slower input rise and fall times.

2. Features and benefits

- Wide supply voltage range from 1.65 V to 5.5 V
- 5 V tolerant inputs for interfacing with 5 V logic
- High noise immunity
- Complies with JEDEC standard:
 - ◆ JESD8-7 (1.65 V to 1.95 V)
 - ◆ JESD8-5 (2.3 V to 2.7 V)
 - ◆ JESD8-B/JESD36 (2.7 V to 3.6 V).
- ESD protection:
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V
- ± 24 mA output drive ($V_{CC} = 3.0$ V)
- CMOS low power consumption
- Latch-up performance exceeds 250 mA
- Direct interface with TTL levels
- Inputs accept voltages up to 5 V
- Multiple package options
- Specified from -40 °C to $+85$ °C and -40 °C to $+125$ °C



3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74LVC1G34GW	-40 °C to +125 °C	TSSOP5	plastic thin shrink small outline package; 5 leads; body width 1.25 mm	SOT353-1
74LVC1G34GV	-40 °C to +125 °C	SC-74A	plastic surface-mounted package; 5 leads	SOT753
74LVC1G34GM	-40 °C to +125 °C	XSON6	plastic extremely thin small outline package; no leads; 6 terminals; body 1 × 1.45 × 0.5 mm	SOT886
74LVC1G34GF	-40 °C to +125 °C	XSON6	plastic extremely thin small outline package; no leads; 6 terminals; body 1 × 1 × 0.5 mm	SOT891
74LVC1G34GN	-40 °C to +125 °C	XSON6	extremely thin small outline package; no leads; 6 terminals; body 0.9 × 1.0 × 0.35 mm	SOT1115
74LVC1G34GS	-40 °C to +125 °C	XSON6	extremely thin small outline package; no leads; 6 terminals; body 1.0 × 1.0 × 0.35 mm	SOT1202
74LVC1G34GX	-40 °C to +125 °C	X2SON5	X2SON5: plastic thermal enhanced extremely thin small outline package; no leads; 5 terminals; body 0.8 × 0.8 × 0.35 mm	SOT1226

4. Marking

Table 2. Marking

Type number	Marking code ^[1]
74LVC1G34GW	YN
74LVC1G34GV	YN
74LVC1G34GM	YN
74LVC1G34GF	YN
74LVC1G34GN	YN
74LVC1G34GS	YN
74LVC1G34GX	YN

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram

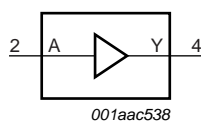


Fig 1. Logic symbol

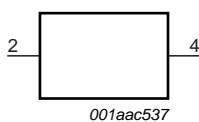


Fig 2. IEC logic symbol

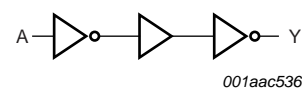


Fig 3. Logic diagram

6. Pinning information

6.1 Pinning

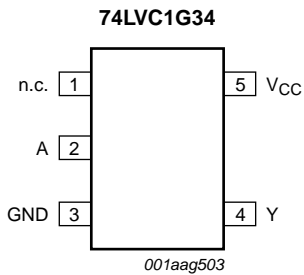


Fig 4. Pin configuration SOT353-1 and SOT753

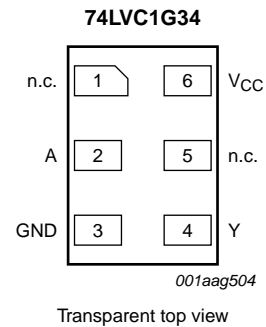


Fig 5. Pin configuration SOT886

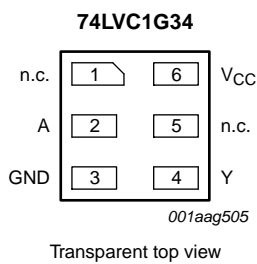


Fig 6. Pin configuration SOT891, SOT1115 and SOT1202

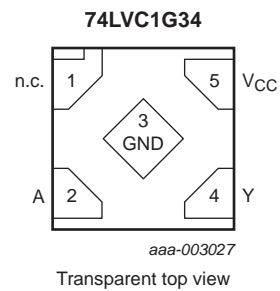


Fig 7. Pin configuration SOT1226 (X2SON5)

6.2 Pin description

Table 3. Pin description

Symbol	Pin		Description
	TSSOP5 and X2SON5	XSON6	
n.c.	1	1	not connected
A	2	2	data input
GND	3	3	ground (0 V)
Y	4	4	data output
n.c.	-	5	not connected
V _{CC}	5	6	supply voltage

7. Functional description

Table 4. Function table^[1]

Input	Output
A	Y
L	L
H	H

- [1] H = HIGH voltage level;
L = LOW voltage level.

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+6.5	V
I_{IK}	input clamping current	$V_I < 0$ V	-50	-	mA
V_I	input voltage		^[1] -0.5	+6.5	V
I_{OK}	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V	-	±50	mA
V_O	output voltage	Active mode	^{[1][2]} -0.5	$V_{CC} + 0.5$	V
		Power-down mode	^{[1][2]} -0.5	+6.5	V
I_O	output current	$V_O = 0$ V to V_{CC}	-	±50	mA
I_{CC}	supply current		-	100	mA
I_{GND}	ground current		-100	-	mA
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to +125 °C	^[3] -	250	mW
T_{stg}	storage temperature		-65	+150	°C

- [1] The minimum input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 [2] When $V_{CC} = 0$ V (Power-down mode), the output voltage can be 5.5 V in normal operation.
 [3] For TSSOP5 and SC-74A packages: above 87.5 °C the value of P_{tot} derates linearly with 4.0 mW/K.
 For XSON6 and X2SON5 package: above 118 °C the value of P_{tot} derates linearly with 7.8 mW/K.

9. Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		1.65	-	5.5	V
V_I	input voltage		0	-	5.5	V
V_O	output voltage	Active mode	0	-	V_{CC}	V_O
		$V_{CC} = 0$ V; Power-down mode	0	-	5.5	V_O
T_{amb}	ambient temperature		-40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.65$ V to 2.7 V	-	-	20	ns/V
		$V_{CC} = 2.7$ V to 5.5 V	-	-	10	ns/V

10. Static characteristics

Table 7. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{amb} = -40\text{ °C to }+85\text{ °C}$ [1]						
V_{IH}	HIGH-level input voltage	$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	$0.65 \times V_{CC}$	-	-	V
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.7	-	-	V
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	2.0	-	-	V
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	$0.7 \times V_{CC}$	-	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	-	-	$0.35 \times V_{CC}$	V
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	-	-	0.7	V
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	-	-	0.8	V
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	-	-	$0.3 \times V_{CC}$	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = -100\text{ }\mu\text{A}$; $V_{CC} = 1.65\text{ V to }5.5\text{ V}$	$V_{CC} - 0.1$	-	-	V
		$I_O = -4\text{ mA}$; $V_{CC} = 1.65\text{ V}$	1.2	1.54	-	V
		$I_O = -8\text{ mA}$; $V_{CC} = 2.3\text{ V}$	1.9	2.15	-	V
		$I_O = -12\text{ mA}$; $V_{CC} = 2.7\text{ V}$	2.2	2.50	-	V
		$I_O = -24\text{ mA}$; $V_{CC} = 3.0\text{ V}$	2.3	2.62	-	V
		$I_O = -32\text{ mA}$; $V_{CC} = 4.5\text{ V}$	3.8	4.11	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = 100\text{ }\mu\text{A}$; $V_{CC} = 1.65\text{ V to }5.5\text{ V}$	-	-	0.10	V
		$I_O = 4\text{ mA}$; $V_{CC} = 1.65\text{ V}$	-	0.07	0.45	V
		$I_O = 8\text{ mA}$; $V_{CC} = 2.3\text{ V}$	-	0.12	0.30	V
		$I_O = 12\text{ mA}$; $V_{CC} = 2.7\text{ V}$	-	0.17	0.40	V
		$I_O = 24\text{ mA}$; $V_{CC} = 3.0\text{ V}$	-	0.33	0.55	V
		$I_O = 32\text{ mA}$; $V_{CC} = 4.5\text{ V}$	-	0.39	0.55	V
I_I	input leakage current	$V_{CC} = 0\text{ V to }5.5\text{ V}$; $V_I = 5.5\text{ V}$ or GND [2]	-	± 0.1	± 5	μA
I_{OFF}	power-off leakage current	$V_{CC} = 0\text{ V}$; V_I or $V_O = 5.5\text{ V}$	-	± 0.1	± 10	μA
I_{CC}	supply current	$V_{CC} = 1.65\text{ V to }5.5\text{ V}$; $I_O = 0\text{ A}$; $V_I = 5.5\text{ V}$ or GND	-	0.1	10	μA
ΔI_{CC}	additional supply current	$V_{CC} = 2.3\text{ V to }5.5\text{ V}$; $V_I = V_{CC} - 0.6\text{ V}$; $I_O = 0\text{ A}$ [2]	-	5	500	μA
C_I	input capacitance	$V_{CC} = 3.3\text{ V}$; $V_I = \text{GND to }V_{CC}$	-	4	-	pF
$T_{amb} = -40\text{ °C to }+125\text{ °C}$						
V_{IH}	HIGH-level input voltage	$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	$0.65 \times V_{CC}$	-	-	V
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.7	-	-	V
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	2.0	-	-	V
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	$0.7 \times V_{CC}$	-	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	-	-	$0.35 \times V_{CC}$	V
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	-	-	0.7	V
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	-	-	0.8	V
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	-	-	$0.3 \times V_{CC}$	V

Table 7. Static characteristics ...continued

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = -100 μA; V _{CC} = 1.65 V to 5.5 V	V _{CC} - 0.1	-	-	V
		I _O = -4 mA; V _{CC} = 1.65 V	0.95	-	-	V
		I _O = -8 mA; V _{CC} = 2.3 V	1.7	-	-	V
		I _O = -12 mA; V _{CC} = 2.7 V	1.9	-	-	V
		I _O = -24 mA; V _{CC} = 3.0 V	2.0	-	-	V
		I _O = -32 mA; V _{CC} = 4.5 V	3.4	-	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = 100 μA; V _{CC} = 1.65 V to 5.5 V	-	-	0.10	V
		I _O = 4 mA; V _{CC} = 1.65 V	-	-	0.70	V
		I _O = 8 mA; V _{CC} = 2.3 V	-	-	0.45	V
		I _O = 12 mA; V _{CC} = 2.7 V	-	-	0.60	V
		I _O = 24 mA; V _{CC} = 3.0 V	-	-	0.80	V
		I _O = 32 mA; V _{CC} = 4.5 V	-	-	0.80	V
I _I	input leakage current	V _{CC} = 0 V to 5.5 V; V _I = 5.5 V or GND	-	-	±100	μA
I _{OFF}	power-off leakage current	V _{CC} = 0 V; V _I or V _O = 5.5 V	-	-	±200	μA
I _{CC}	supply current	V _{CC} = 1.65 V to 5.5 V; I _O = 0 A; V _I = 5.5 V or GND	-	-	200	μA
ΔI _{CC}	additional supply current	V _{CC} = 2.3 V to 5.5 V; V _I = V _{CC} - 0.6 V; I _O = 0 A	-	-	5000	μA

[1] All typical values are measured at T_{amb} = 25 °C.[2] These typical values are measured at V_{CC} = 3.3 V.

11. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see [Figure 9](#).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
t _{pd}	propagation delay	A to Y; see Figure 8 ^[2]						
		V _{CC} = 1.65 V to 1.95 V	1.0	4.0	8.6	1.0	11.0	ns
		V _{CC} = 2.3 V to 2.7 V	0.5	2.6	4.4	0.5	5.6	ns
		V _{CC} = 2.7 V	0.5	2.3	4.5	0.5	5.6	ns
		V _{CC} = 3.0 V to 3.6 V	0.5	2.0	4.1	0.5	5.2	ns
		V _{CC} = 4.5 V to 5.5 V	0.5	1.6	3.2	0.5	4.1	ns
C _{PD}	power dissipation capacitance	V _I = GND to V _{CC} ; V _{CC} = 3.3 V ^[3]	-	15	-	-	-	pF

[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.8 V, 2.5 V, 2.7 V, 3.3 V, and 5.0 V respectively.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

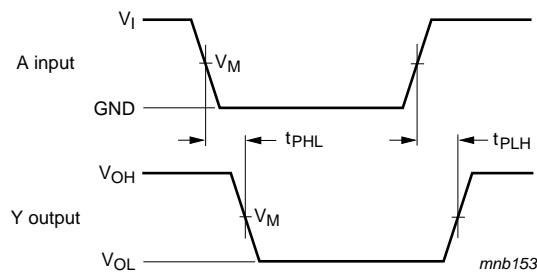
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

∑(C_L × V_{CC}² × f_o) = sum of outputs.

12. Waveforms



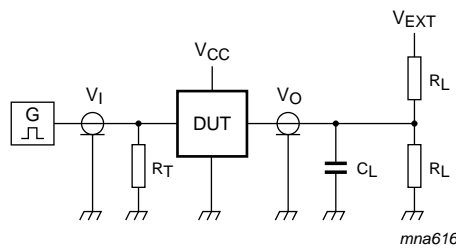
Measurement points are given in [Table 9](#).

V_{OL} and V_{OH} are typical output voltage drops that occur with the output load.

Fig 8. The data input (A) to output (Y) propagation delays

Table 9. Measurement points

Supply voltage	Input	Output
V_{CC}	V_M	V_M
1.65 V to 1.95 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
2.3 V to 2.7 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
2.7 V	1.5 V	1.5 V
3.0 V to 3.6 V	1.5 V	1.5 V
4.5 V to 5.5 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$



Test data is given in [Table 10](#).

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

Fig 9. Test circuit for measuring switching times

Table 10. Test data

Supply voltage	Input	Load			V_{EXT}
V_{CC}	V_I	$t_r = t_f$	C_L	R_L	t_{PLH}, t_{PHL}
1.65 V to 1.95 V	V_{CC}	≤ 2.0 ns	30 pF	1 k Ω	open
2.3 V to 2.7 V	V_{CC}	≤ 2.0 ns	30 pF	500 Ω	open
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open
4.5 V to 5.5 V	V_{CC}	≤ 2.5 ns	50 pF	500 Ω	open

13. Package outline

TSSOP5: plastic thin shrink small outline package; 5 leads; body width 1.25 mm

SOT353-1

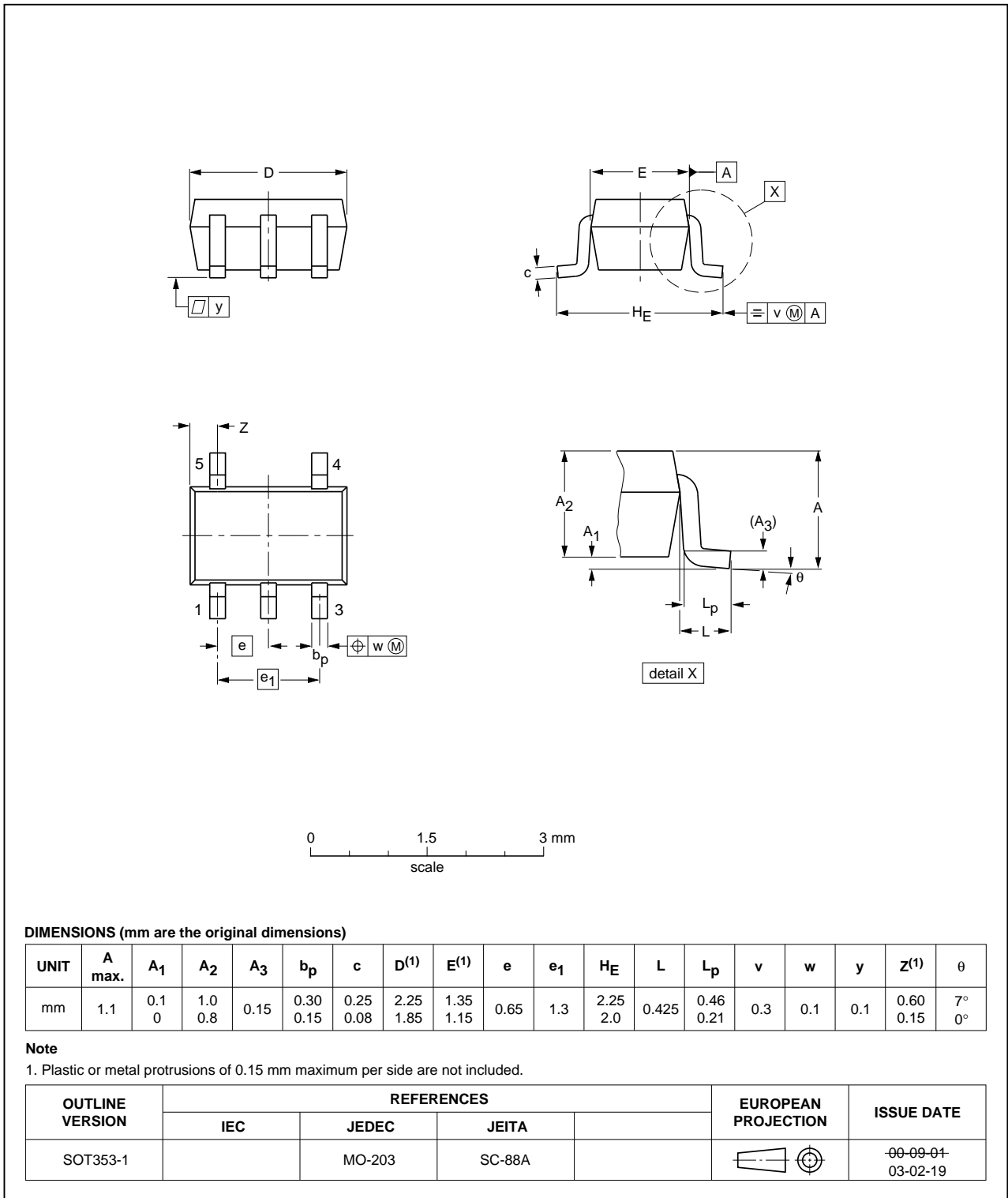


Fig 10. Package outline SOT353-1 (TSSOP5)

Plastic surface-mounted package; 5 leads

SOT753

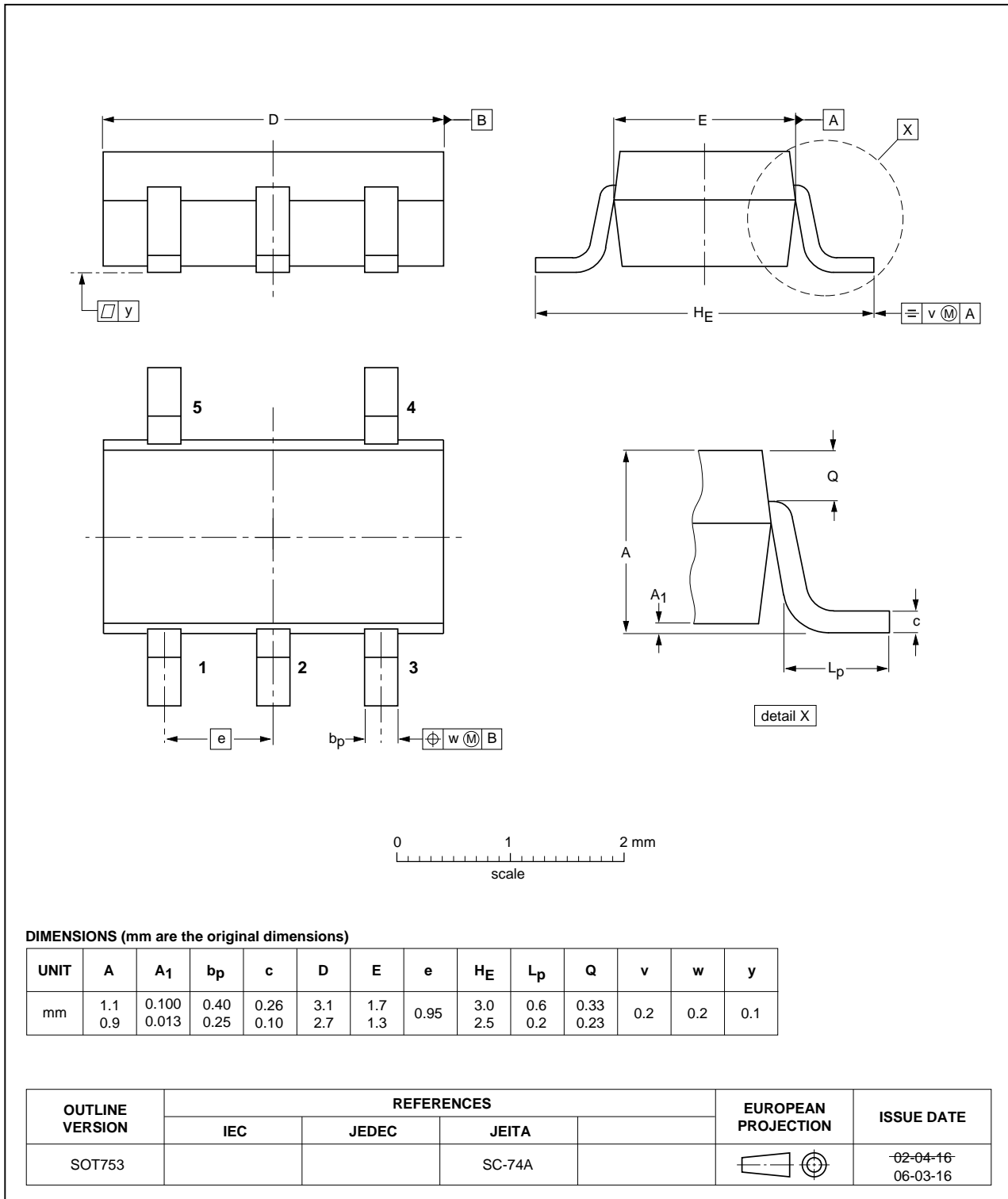


Fig 11. Package outline SOT753 (SC-74A)

XSON6: plastic extremely thin small outline package; no leads; 6 terminals; body 1 x 1.45 x 0.5 mm

SOT886

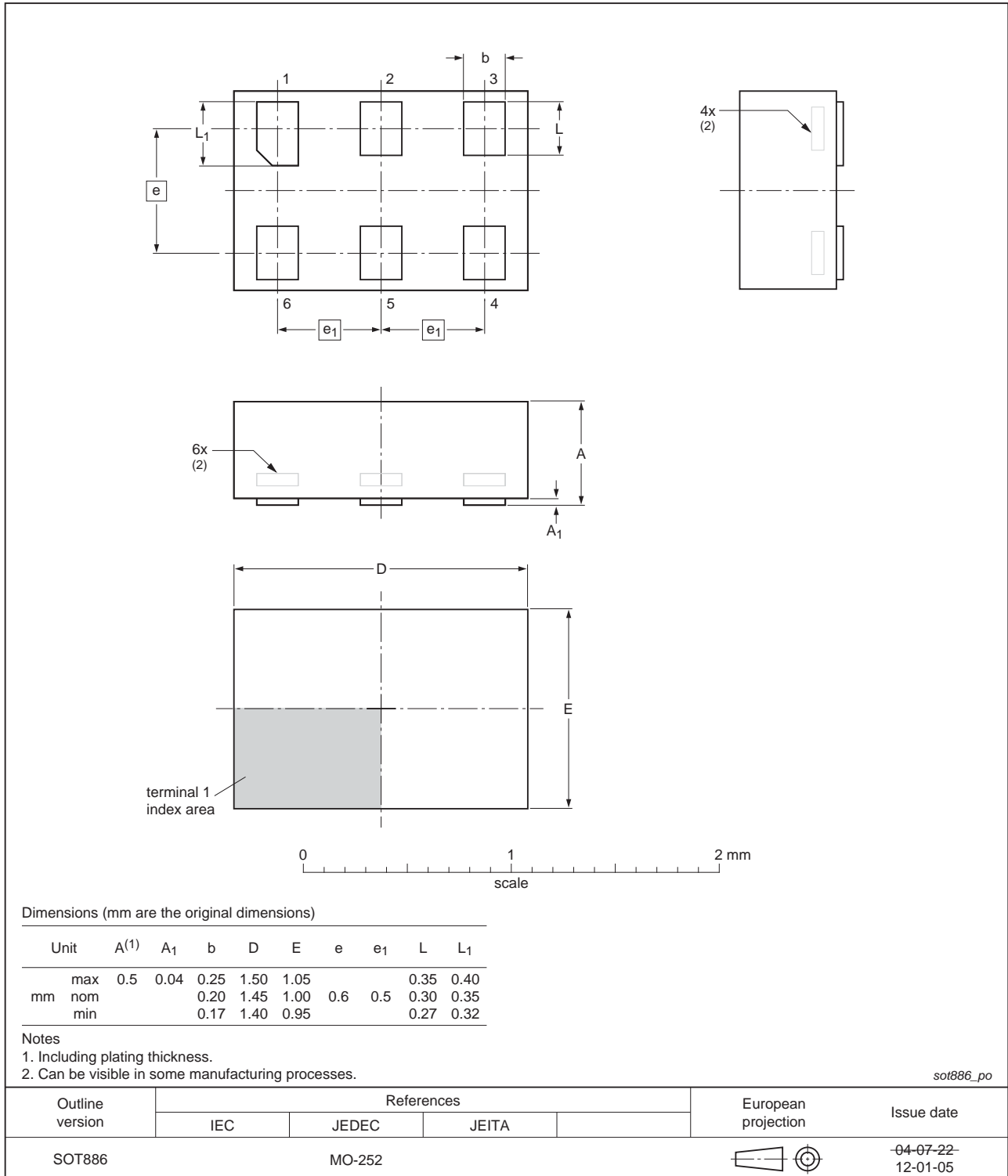


Fig 12. Package outline SOT886 (XSON6)

XSON6: plastic extremely thin small outline package; no leads; 6 terminals; body 1 x 1 x 0.5 mm

SOT891

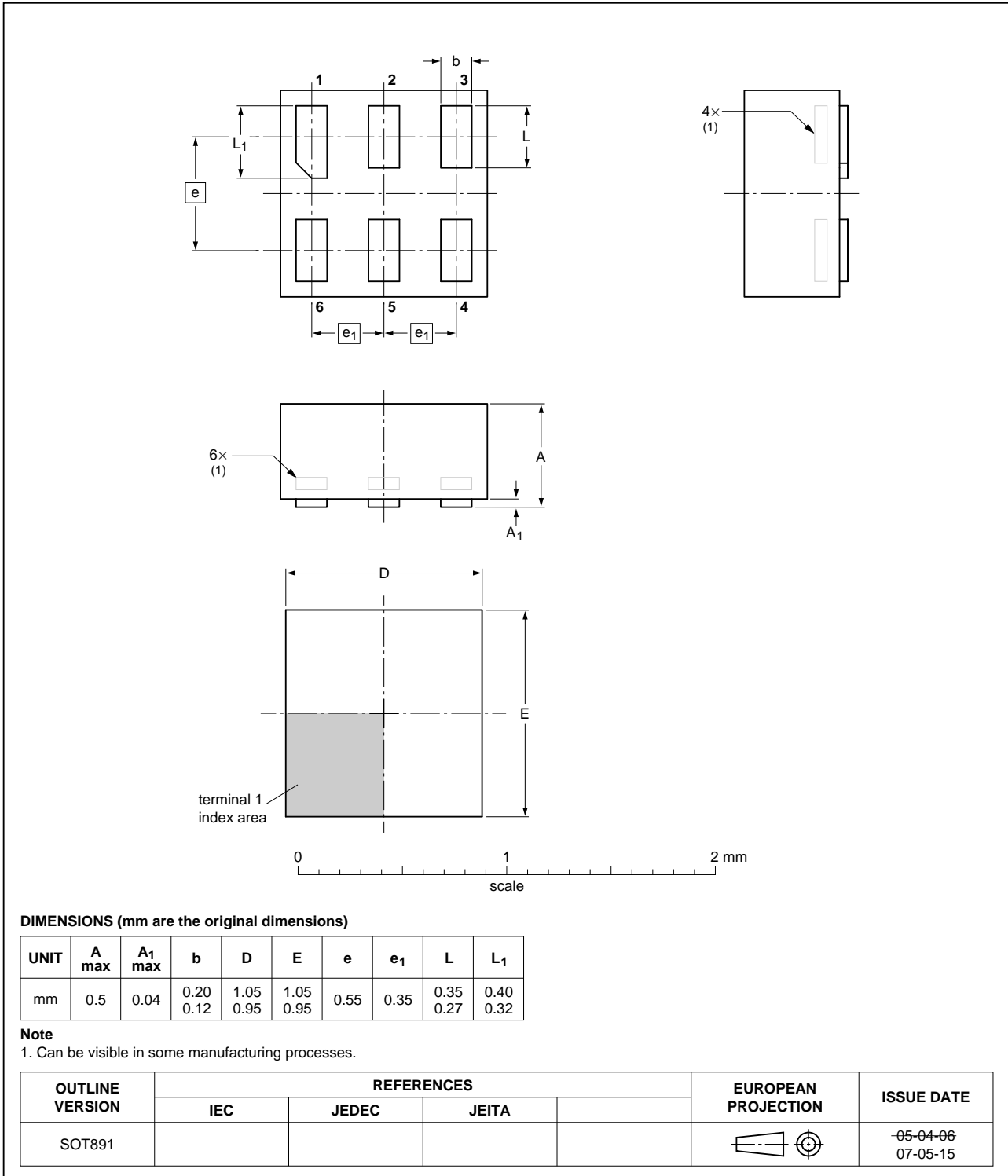


Fig 13. Package outline SOT891 (XSON6)

**XSON6: extremely thin small outline package; no leads;
6 terminals; body 0.9 x 1.0 x 0.35 mm**

SOT1115

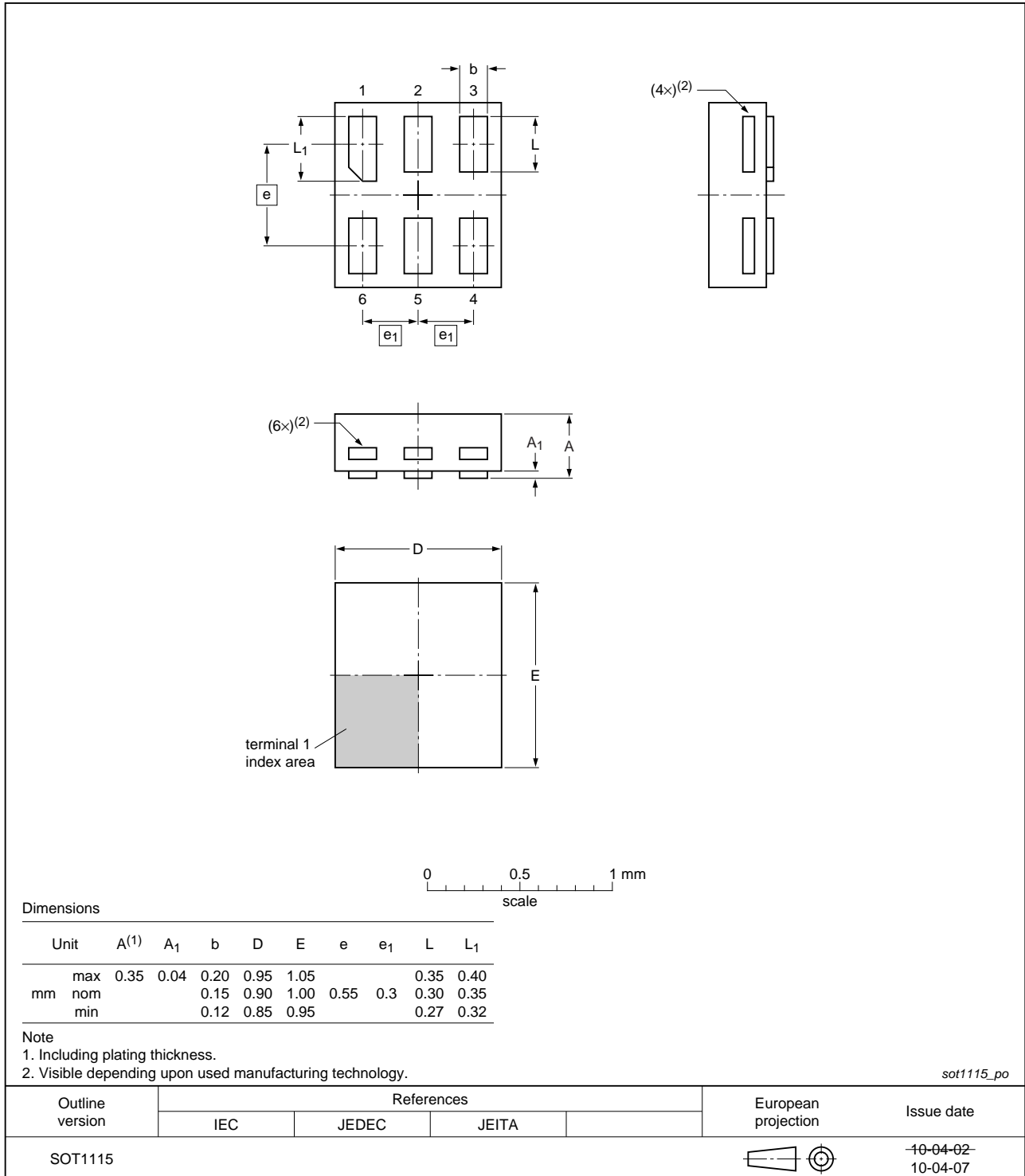


Fig 14. Package outline SOT1115 (XSON6)

XSON6: extremely thin small outline package; no leads;
6 terminals; body 1.0 x 1.0 x 0.35 mm

SOT1202

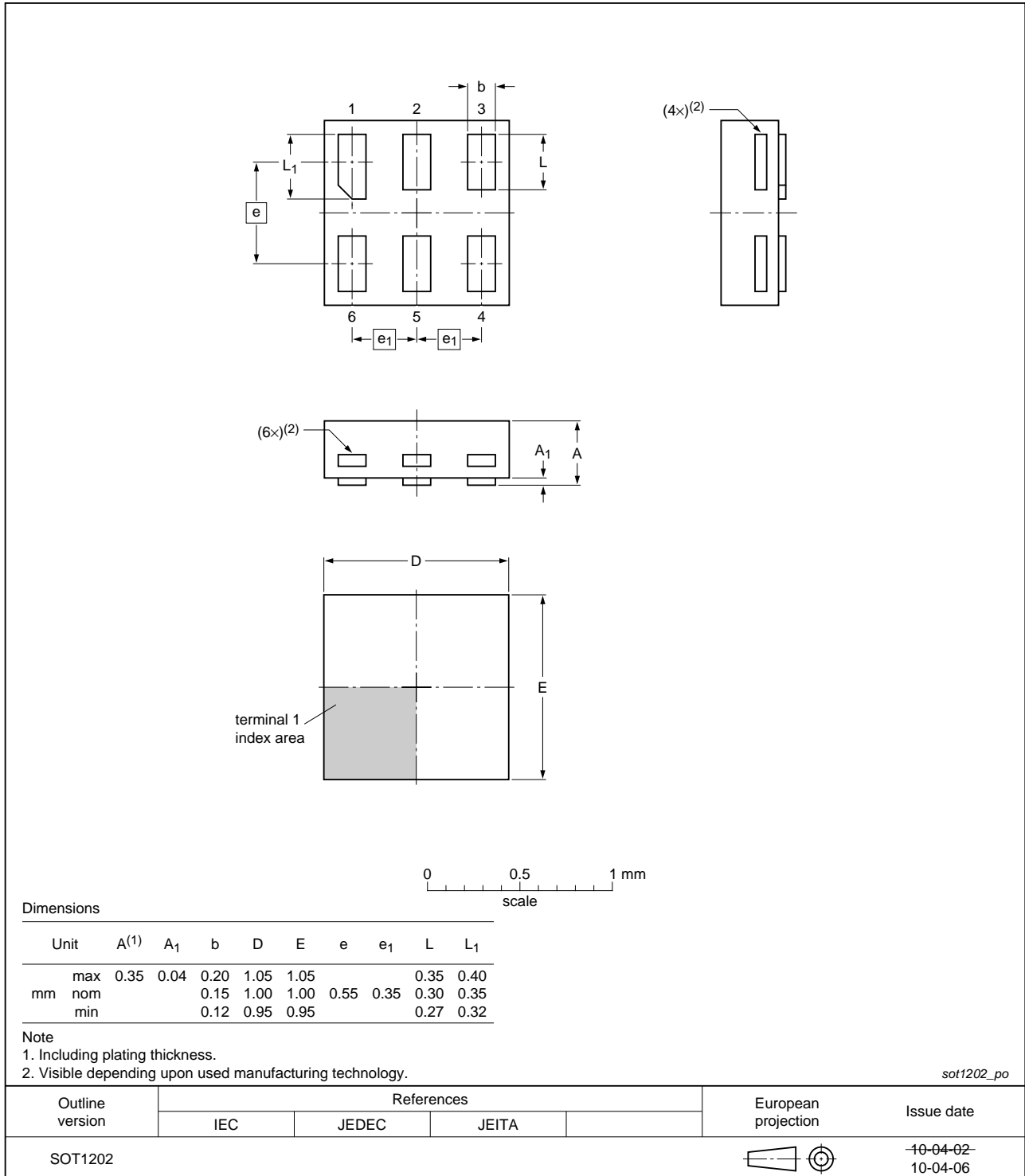


Fig 15. Package outline SOT1202 (XSON6)

X2SON5: plastic thermal enhanced extremely thin small outline package; no leads;
5 terminals; body 0.8 x 0.8 x 0.35 mm

SOT1226

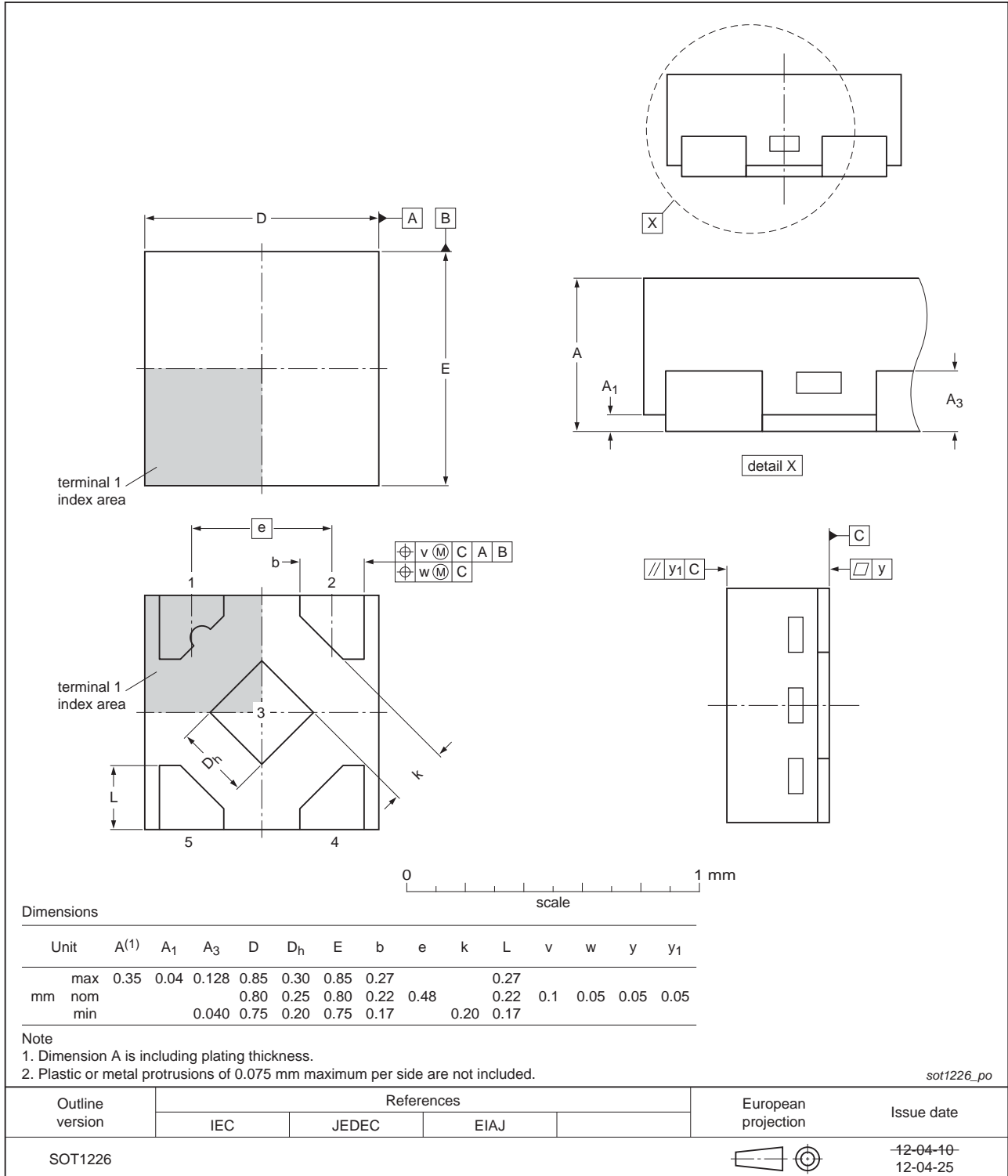


Fig 16. Package outline SOT1226 (X2SON5)

14. Abbreviations

Table 11. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

15. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC1G34 v.5	20120702	Product data sheet	-	74LVC1G34 v.4
Modifications:	<ul style="list-style-type: none"> Added type number 74LVC1G34GX (SOT1226) Package outline drawing of SOT886 (Figure 12) modified. 			
74LVC1G34 v.4	20111206	Product data sheet	-	74LVC1G34 v.3
Modifications:	<ul style="list-style-type: none"> Legal pages updated. 			
74LVC1G34 v.3	20100902	Product data sheet	-	74LVC1G34 v.2
74LVC1G34 v.2	20070521	Product data sheet	-	74LVC1G34 v.1
74LVC1G34 v.1	20050907	Product data sheet	-	-

16. Legal information

16.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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