Low Power Universal SLIC Family

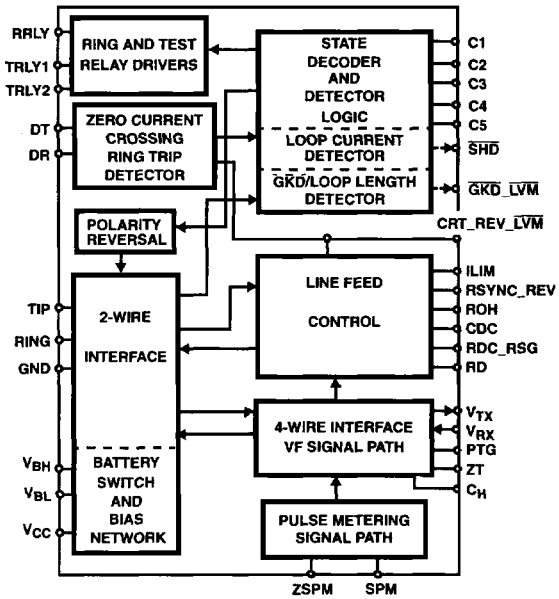
The UniSLIC14 is a family of Ultra Low Power SLICs. The feature set and common pinouts of the UniSLIC14 family positions it as a universal solution for: Plain Old Telephone Service (POTS), PBX, Central Office, Loop Carrier, Fiber in the Loop, ISDN-TA and NT1+, Pairgain and Wireless Local Loop.

The UniSLIC14 family achieves it's ultra low power operation through: It's automatic single and dual battery operation (based on line length), low power standby state and battery tracking saturation guard to ensure the maximum loop coverage on the lowest battery voltage. This architecture is ideal for power critical applications such as ISDN NT1+, Pairgain and Wireless local loop products.

The UniSLIC14 family has many user programmable features. This family of SLICs delivers a low noise, low component count solution for Central Office and Loop Carrier universal voice grade designs. The product family integrates advanced pulse metering, test and signaling capabilities, and zero crossing ring control.

The UniSLIC14 family is designed in the Harris "Latch" free Bonded Wafer process. This process dielectrically isolates the active circuitry to eliminate any leakage paths as found in our competition's JI process. This makes the UniSLIC14 family compliant with "hot plug" requirements and operation in harsh outdoor environments.

Block Diagram



Features

- Ultra Low Active Power (OHT) < 60mW
- Low Standby Power < 25mW
- Single/Dual Battery Operation
- Automatic Silent Battery Switching
- Thermal Management/Shutdown
- Battery Tracking Saturation Guard
- Single 5V Supply
- Zero Crossing Ring Control
  - Zero Voltage On/Zero Current Off
- Tip/Ring Disconnect
- Pulse Metering Capability
- 4 Wire Loopback
- Programmable Constant Current Feed
- Programmable Resistive Feed
- Programmable Loop Detect Threshold
- Programmable On-Hook and Off-Hook Overheads
- Programmable Overhead for Pulse Metering
- Programmable Polarity Reversal Time
- Selectable Transmit Gain 0dB/-6dB
- 2 Wire Impedance Set by Single Network
- Loop and Ground Key Detectors
- On-Hook Transmission
- Common Pinout
- HC55121
  - Polarity Reversal
- HC55130
  - -63dB Longitudinal Balance
- HC55140
  - Polarity Reversal
  - Ground Start
  - Line Voltage Measurement
  - 2 Wire Loopback
  - -63dB Longitudinal Balance
- HC55142
  - Polarity Reversal
  - Ground Start
  - Line Voltage Measurement
  - 2.2V_{RMS} Pulse Metering
  - 2 Wire Loopback
- HC55150
  - Polarity Reversal
  - Line Voltage Measurement
  - 2.2V_{RMS} Pulse Metering
  - 2 Wire Loopback

Related Literature

- AN9832, User's Guide for Development Board

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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Ordering Information (PLCC Package Only)

PART NUMBER	MAX LOOP CURRENT (mA)	POLARITY REVERSAL	GROUND START	GROUND KEY	LINE VOLTAGE MEASUREMENT †	PULSE METERING	2 TEST RELAY DRIVERS	2 WIRE LOOPBACK †	LONGITUDINAL BALANCE	TEMP RANGE (°C)	PKG. NO.
HC55120CM	30			•					53dB	0 to 70	M28.3 N28.45
HC55121IM	30	•		•		•		•	53dB	-40 to 85	M28.3 N28.45
HC55130IM	45						HC55131IM		63dB	-40 to 85	M28.3 N28.45
HC55140IM	45	•	•	•	•		HC5514IM	•	63dB	-40 to 85	M28.3 N28.45
HC55142IM	45	•	•	•	•	•	HC55143IM	•	53dB	-40 to 85	M28.3 N28.45
HC55150CM	45	•			•	•	HC5515ICM	•	55dB	0 to 70	M28.3 N28.45
HC5514XEVAL1	Evaluation board										

† Available by placing SLIC in Test mode.

Device Operating Modes

C3	C2	C1	DESCRIPTION	HC55120	HC55121	HC55130/1	HC55140/1	HC55142/3	HC55150/1
0	0	0	Disconnect Tip and Ring.	•	•	•	•	•	•
0	0	1	Ringing	•	•	•	•	•	•
0	1	0	Forward Active	•	•	•	•	•	•
0	1	1	Test Forward Active 2 Wire Loopback and Line Voltage Measurement		•		•	•	•
1	0	0	Tip Open Ground Start				•	•	
1	0	1	Low Power Standby	•	•	•	•	•	•
1	1	0	Reverse Active		•		•	•	•
1	1	1	Test Reverse Active Line Voltage Measurement				•	•	•

Absolute Maximum Ratings $T_A = 25^oC$

Temperature, Humidity
- Storage Temperature Range ..... -65°C to 150°C
- Operating Temperature Range..... -40°C to 110°C
- Operating Junction Temperature Range..... -40°C to 150°C

Power Supply (-40°C ≤ T_A ≤ +85°C)
- Supply Voltage V_{CC} to GND ..... -.04V to 7V
- Supply Voltage V_{BL} to GND..... $-V_{BL}$ to 0.4V
- Supply Voltage V_{BH} to GND, Continuous..... -75V to 0.4V
- Supply Voltage V_{BH} to GND, 10ms ..... -80V to 0.4V

Relay Driver
- Ring Relay Supply Voltage ..... 0V to 14V
- Ring Relay Current..... 50mA

Digital Inputs, Outputs (C1, C2, C3, C4, C5, $\overline{SHD}$, $\overline{GKD_LVM}$)
- Input Voltage ..... -0.4V to V_{CC}
- Output Voltage ($\overline{SHD}$, $\overline{GKD_LVM}$ Not Active)..... -0.4V to V_{CC}
- Output Current ($\overline{SHD}$, $\overline{GKD}$_LVM) 5mA

ESD Rating 500V

Gate Count..... 543 Transistors, 51 Diodes

Tipx and Ringx Terminals (-40°C ≤ T_A ≤ 85°C)
- Tipx or Ringx Current..... -100mA to 100mA

Tip and Ring Terminals

- Tipx or Ringx, Current, Pulse < 10ms, T_{REP} > 10s 2A
- Tipx or Ringx, Current, Pulse < 1ms, T_{REP} > 10s 5A
- Tipx or Ringx, Current, Pulse < 10µs, T_{REP} > 10s 15A
- Tipx or Ringx, Current, Pulse < 1µs, T_{REP} > 10s 20A
- Tipx or Ringx, Pulse < 250ns, T_{REP} > 10s 20A

Thermal Information

Thermal Resistance θ_{JA}
- 28 Lead PLCC Package..... 53°C/W
- 28 Lead SOIC Package..... TBD°C/W
- 32 Lead PLCC Package..... TBD°C/W

Continuous Power Dissipation at +85°C
- 28 Lead PLCC Package..... 1.5W
- 28 Lead SOIC Package..... TBDW
- 32 Lead PLCC Package..... TBDW

Peak Power Dissipation at 70°C, t<100ms, t_{Rep}>1 sec
- 28 Lead PLCC Package..... TBDW
- 28 Lead SOIC Package..... TBDW
- 32 Lead PLCC Package..... TBDW

Lead Temperature (Soldering 10s, PLCC Lead Tips Only) .... 300°C

Derate above 70°C

PLCC..... 15.4mW/°C

SOIC ..... TBDW/°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Typical Operating Conditions

These represent the conditions under which the part was developed and are suggested as guidelines.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Ambient Temperature	HC55120, HC55150/1	0	-	70	°C
	HC55121, HC55130/1, HC55140/1, HC55142/3	-40	-	85	°C
V_{BH} with Respect to GND		-58	-	-8	V
V_{BL} with Respect to GND		V_{BH}	-	-8	V
V_{CC} with Respect to GND		4.75	-	5.25	V

Electrical Specifications

T_A = -40°C to 85°C, V_{CC} = +5V ±5%, V_{BH} = -48V, V_{BL} = No connect, PTG = Open, R_{F1} = R_{F2} = 0Ω, Z_T = 120kΩ, R_{LIM} = 38.3kΩ, R_D = 58.8kΩ, RDC_RSG = 20kΩ, R_{OH} = 50kΩ, C_H = 0.47µF, C_{DC} = 1.0µF, $C_{RT/REV}$ = 0.47µf, GND = 0V, RL = 600Ω. Unless Otherwise Specified. **(•)** symbol used to indicate the test applies to the part. (NA) symbol used to indicate the test does not apply to the part.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS	HC55120	HC55121	HC55130/1	HC55140/1	HC55142/3	HC55150/1
2-WIRE PORT											
Overload Level, Off Hook Forward and Reverse	1% THD, I_{DCMET} ≥ 18mA (Note 2, Figure 1)	3.2	-	-	V_{PEAK}	Forward Only	•	Forward Only	•	•	•
Overload Level, On Hook Forward and Reverse	1% THD, IDCMET ≤ 5mA (Note 3, Figure 1)	1.3	-	-	V_{PEAK}	Forward Only	•	Forward Only	•	•	•
Input Impedance (Into Tip and Ring)		-	Z_T/200	-	Ω	•	•	•	•	•	•
Longitudinal Impedance (Tip, Ring) Forward and Reverse	0 < f < 100Hz (Note 4, Figure 2)	-	0	-	Ω/Wire	Forward Only	•	Forward Only	•	•	•
LONGITUDINAL CURRENT LIMIT (TIP, RING)											
On-Hook, Off-Hook (Active), R_L = 736Ω Forward and Reverse	No False Detections, (Loop Current), LB > 45dB (Note 5, Figure 3A)	28	-	-	mA_{RMS}/Wire	Forward Only	•	Forward Only	•	•	•
On-Hook (Low Power Standby), R_L = ∞, R_D = 58.8kΩ	No False Detections (Loop Current) (Note 6, Figure 3B)	-	-	8.5	mAPEAK/Wire	•	•	•	•	•	•

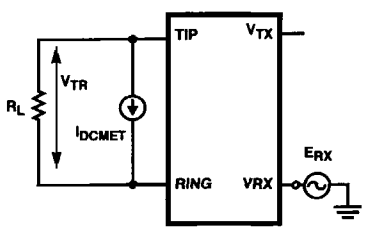


FIGURE 1. OVERLOAD LEVEL (OFF HOOK, ON HOOK)

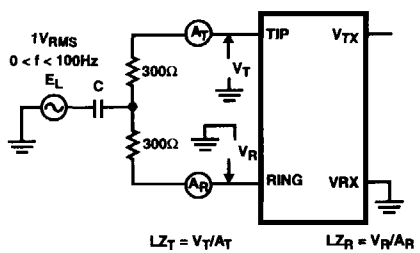


FIGURE 2. LONGITUDINAL IMPEDANCE

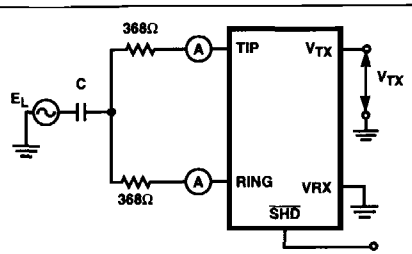


FIGURE 3A. LONGITUDINAL CURRENT LIMIT OFF-HOOK (ACTIVE)

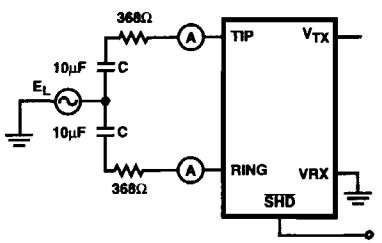


FIGURE 3B. LONGITUDINAL CURRENT LIMIT ON-HOOK (STANDBY)

Electrical Specifications T_A = -40°C to 85°C, V_{CC} = +5V ±5%, V_{BH} = -48V, V_{BL} = No connect, PTG = Open, R_{F1} = R_{F2} = 0Ω, Z_T = 120kΩ, R_{LIM} = 38.3kΩ, R_D = 58.8kΩ, RDC_RSG = 20kΩ, R_{OH} = 50kΩ, C_H = 0.47µF, C_{DC} = 1.0µF, $C_{RT/REV}$ = 0.47µf, GND = 0V, RL = 600Ω Unless Otherwise Specified. (•) symbol used to indicate the test applies to the part. (NA) symbol used to indicate the test does not apply to the part. **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS	HC55120	HC55121	HC55130/1	HC55140/1	HC55142/3	HC55150/1
OFF-HOOK LONGITUDINAL BALANCE											
						MIN	MIN	MIN	MIN	MIN	MIN
Longitudinal to Metallic (Note 7) Forward and Reverse	IEEE 455 - 1985, R_{LR}, R_{LT} = 368Ω Normal Polarity:					Forward Only		Forward Only			
	0.2kHz < f < 1.0kHz, 0°C to 70°C	-	-	-	dB	53	NA	NA	NA	NA	55
	1.0kHz < f < 3.4kHz, 0°C to 70°C	-	-	-	dB	53	NA	NA	NA	NA	55
	0.2kHz < f < 1.0kHz, -40°C to 85°C	-	-	-	dB	NA	53	63	63	53	NA
	1.0kHz < f < 3.4kHz, -40°C to 85°C	-	-	-	dB	NA	53	58	58	53	NA
	Reverse Polarity 0.2kHz < f < 3.4kHz, (Figure 4)	-	-	-	dB	NA	53	NA	58	53	55
						MIN	MIN	MIN	MIN	MIN	MIN
Longitudinal to Metallic (Note 7) Forward and Reverse	R_{LR}, R_{LT} = 300Ω, Normal Polarity:					Forward Only		Forward Only			
	0.2kHz < f < 1.0kHz, 0°C to 70°C	-	-	-	dB	53	NA	NA	NA	NA	55
	1.0kHz < f < 3.4kHz, 0°C to 70°C	-	-	-	dB	53	NA	NA	NA	NA	55
	0.2kHz < f < 1.0kHz, -40°C to 85°C	-	-	-	dB	NA	53	63	63	53	NA
	1.0kHz < f < 3.4kHz, -40°C to 85°C	-	-	-	dB	NA	53	58	58	53	NA
	Reverse Polarity 0.2kHz < f < 3.4kHz, (Figure 4)	-	-	-	dB	NA	53	NA	58	53	55
						MIN	MIN	MIN	MIN	MIN	MIN
Longitudinal to 4-Wire (Note 9) (Forward and Reverse)	Normal Polarity:					Forward Only		Forward Only			
	0.2kHz < f < 1.0kHz, 0°C to 70°C	-	-	-	dB	53	NA	NA	NA	NA	61
	1.0kHz < f < 3.4kHz,0°C to 70°C	-	-	-	dB	53	NA	NA	NA	NA	61
	0.2kHz < f < 1.0kHz, -40°C to 85°C	-	-	-	dB	NA	53	63	63	53	NA
	1.0kHz < f < 3.4kHz, -40°C to 85°C	-	-	-	dB	NA	53	58	58	53	NA
	Reverse Polarity 0.2kHz < f < 3.4kHz, (Figure 4)	-	-		dB	NA	53	NA	58	53	61
Metallic to Longitudinal (Note 10) Forward and Reverse	FCC Part 68, Para 68.310 (Note 8) 0.2kHz < f < 3.4kHz, (Figure 5)	40	50	-	dB	Forward Only	•	Forward Only	•	•	•
4-Wire to Longitudinal (Note 11) Forward and Reverse	0.2kHz < f < 3.4kHz, (Figure 5)	40	-	-	dB	Forward Only	•	Forward Only	•	•	•

Electrical Specifications T_A = -40°C to 85°C, V_{CC} = +5V ±5%, V_{BH} = -48V, V_{BL} = No connect, PTG = Open, $R_{F1} = R_{F2} = 0\Omega$, Z_T = 120kΩ, R_{LIM} = 38.3kΩ, R_D = 58.8kΩ, RDC_RSG = 20kΩ, R_{OH} = 50kΩ, C_H = 0.47µF, C_{DC} = 1.0µF, $C_{RT/REV}$ = 0.47µf, GND = 0V, RL = 600Ω. Unless Otherwise Specified. **(•)** symbol used to indicate the test applies to the part. (NA) symbol used to indicate the test does not apply to the part. **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS	HC55120	HC55121	HC55130/1	HC55140/1	HC55142/3	HC55150/1
2-Wire Return Loss Forward and Reverse	0.2kHz to 1.0kHz (Note 12, Figure 6)	30	35	-	dB	Forward Only	•	Forward Only	•	•	•
	1.0kHz to 3.4kHz (Note 12, Figure 6)	23	25	-	dB						
TIP IDLE VOLTAGE (User Programmable)											
TIPX Idle Voltage Forward and Reverse	Active, I_L < 5mA	-	-2.0	-	V	Forward Only	•	Forward Only	•	•	•
RING IDLE VOLTAGE (User Programmable)											
RINGX Idle Voltage Forward and Reverse	Active, I_L < 5mA	-	V_{BH}+2.5	-	V	Forward Only	•	Forward Only	•	•	•
	Tip open, I_L < 5mA	-	V_{BH}+2.5	-	V						
V_{TR} Forward and Reverse	Active, I_L < 5mA	-	V_{BH}-4.5	-	V	Forward Only	•	Forward Only	•	•	•
$V_{TR(ROH)}$ Pulse Metering Forward and Reverse	Active, $I_L \geq 8.5$mA, R_{OH} = 50kΩ	-	V_{BH}-8.9	-	V	NA	•	NA	NA	•	•

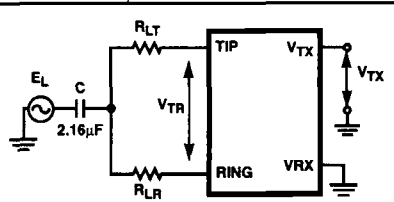


FIGURE 4. LONGITUDINAL TO METALLIC AND LONGITUDINAL TO 4-WIRE BALANCE

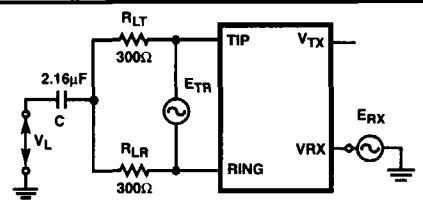


FIGURE 5. METALLIC TO LONGITUDINAL AND 4-WIRE TO LONGITUDINAL BALANCE

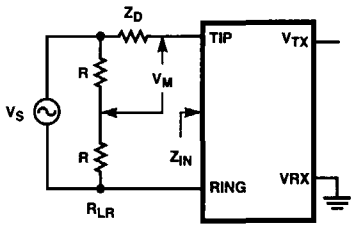


FIGURE 6. TWO-WIRE RETURN LOSS

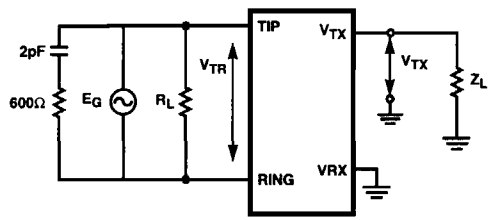


FIGURE 7. OVERLOAD LEVEL (4-WIRE TRANSMIT PORT), OUTPUT OFFSET VOLTAGE AND HARMONIC DISTORTION

Electrical Specifications T_A = -40°C to 85°C, V_{CC} = +5V ±5%, V_{BH} = -48V, V_{BL} = No connect, PTG = Open, R_{F1} = R_{F2} = 0Ω, Z_T = 120kΩ, R_{LIM} = 38.3kΩ, R_D = 58.8kΩ, RDC_RSG = 20kΩ, R_{OH} = 50kΩ, C_H = 0.47µF, C_{DC} = 1.0µF, $C_{RT/REV}$ = 0.47µf, GND = 0V, RL = 600Ω Unless Otherwise Specified. (•) symbol used to indicate the test applies to the part. (NA) symbol used to indicate the test does not apply to the part. **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS	HC55120	HC55121	HC55130/1	HC55140/1	HC55142/3	HC55150/1
4-WIRE TRANSMIT PORT (V_{TX})											
Overload Level, Off Hook (I_L≥ 18mA) Forward and Reverse	(Z_L > 20kΩ, IL 1% THD) (Note 13, Figure 7)	3.2	-	-	V_{PEAK}	Forward Only	•	Forward Only	•	•	•
Overload Level, On Hook (I_L ≤ 5mA) Forward and Reverse	(Z_L > 20kΩ, 1% THD) (Note 14, Figure 7)	1.3	-	-	V_{PEAK}	Forward Only	•	Forward Only	•	•	•
Output Offset Voltage Forward and Reverse	E_G = 0, Z_L = ∞, (Note 15, Figure 7)	-100	-	100	mV	Forward Only	•	Forward Only	•	•	•
Output Impedance (Guaranteed by Design)	0.2kHz < f < 03.4kHz	-	0.1	1	Ω	•	•	•	•	•	•
4-WIRE RECEIVE PORT (VRX)											
VRX Input Impedance (Guaranteed by Design)	0.2kHz < f < 3.4kHz	-	500	600	kΩ	•	•	•	•	•	•
FREQUENCY RESPONSE (OFF-HOOK)											
2-Wire to 4-Wire Forward and Reverse	Relative to 0dBm at 1.0kHz, E_{RX} = 0V					Forward Only		Forward Only			
	0.3kHz < f < 3.4kHz	-0.2	-	0.1	dB		•		•	•	•
	f = 8.0kHz, 12kHz, 16kHz (Note 16, Figure 8)	-1.0	-	0	dB						
4-Wire to 2-Wire Forward and Reverse	Relative to 0dBm at 1.0kHz, E_G = 0V					Forward Only		Forward Only			
	0.3kHz < f < 3.4kHz	-0.2	-	0.1	dB		•		•	•	•
	f = 8.0kHz, 12kHz	-1.0	-	0	dB						
	f = 16kHz (Note 17, Figure 8)	-2.0	-	-	dB						
4-Wire to 4-Wire Forward and Reverse	Relative to 0dBm at 1.0kHz, E_G = 0V					Forward Only		Forward Only			
	0.3kHz < f < 3.4kHz (Note 18, Figure 8)	-0.2	-	0.1	dB		•		•	•	•

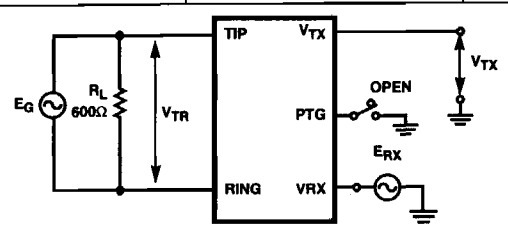


FIGURE 8. FREQUENCY RESPONSE, INSERTION LOSS, GAIN TRACKING AND HARMONIC DISTORTION

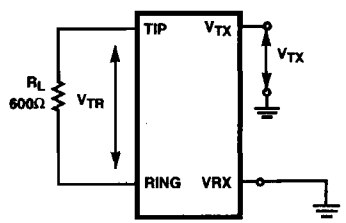


FIGURE 9. IDLE CHANNEL NOISE

Electrical Specifications T_A = -40°C to 85°C, V_{CC} = +5V ±5%, V_{BH} = -48V, V_{BL} = No connect, PTG = Open, R_{F1} = R_{F2} = 0Ω, Z_T = 120kΩ, R_{LIM} = 38.3kΩ, R_D = 58.8kΩ, RDC_RSG = 20kΩ, R_{OH} = 50kΩ, C_H = 0.47µF, C_{DC} = 1.0µF, $C_{RT/REV}$ = 0.47µf, GND = 0V, RL = 600Ω. Unless Otherwise Specified. (•) symbol used to indicate the test applies to the part. (NA) symbol used to indicate the test does not apply to the part. **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS	HC55120	HC55121	HC55130/1	HC55140/1	HC55142/3	HC55150/1
INSERTION LOSS											
2-Wire to 4-Wire Forward and Reverse	0dBm, 1kHz PTG = Open (Note 19, Figure 8)	-0.2	-	0.2	dB	Forward Only	•	Forward Only	•	•	•
4-Wire to 2-Wire Forward and Reverse	PTG = GND (Note 20, (Figure 8)	-6.22	-6.02	-5.82	dB						
	0dBm, 1kHz (Note 21, Figure 8)	-0.2	-	0.2	dB	Forward Only	•	Forward Only	•	•	•
GAIN TRACKING (Ref = -10dBm, at 1.0kHz)											
2-Wire to 4-Wire Forward and Reverse	-40dBm to +3dBm (Note 22, Figure 8)	-0.1	-	0.1	dB	Forward Only	•	Forward Only	•	•	•
	-55dBm to -40dBm (Note 22, Figure 8)	-0.2	–	0.2	dB						
4-Wire to 2-Wire Forward and Reverse	-40dBm to +3dBm (Note 23, Figure 8)	-0.1	-	0.1	dB	Forward Only	•	Forward Only	•	•	•
	-55dBm to -40dBm (Note 23, Figure 8)	-0.2	–	0.2	dB						
NOISE											
Idle Channel Noise at 2-Wire Forward and Reverse	C-Message Weighting	-	-	12	dBrnC	Forward Only	•	Forward Only	•	•	•
	Psophometric Weighting (Note 24, Figure 9)	-	-	-78	dBmp						
Idle Channel Noise at 4-Wire Forward and Reverse	C-Message Weighting	-	-	12	dBrnC	Forward Only	•	Forward Only	•	•	•
	Psophometrical Weighting (Note 25, Figure 9)	-	-	-78	dBmp						
HARMONIC DISTORTION											
2-Wire to 4-Wire Forward and Reverse	0dBm, 0.3kHz to 3.4kHz (Note 26, Figure 7)	-	-67	-50	dB	Forward Only	•	Forward Only	•	•	•
4-Wire to 2-Wire Forward and Reverse	0dBm, 0.3kHz to 3.4kHz (Note 27, Figure 8)	-	-67	-50	dB	Forward Only	•	Forward Only	•	•	•

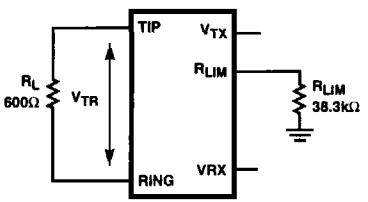


FIGURE 10. CONSTANT LOOP CURRENT TOLERANCE

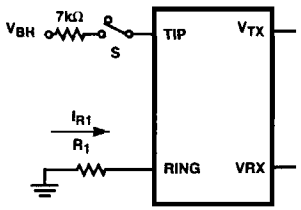


FIGURE 11. TIPX VOLTAGE

Electrical Specifications T_A = -40°C to 85°C, V_{CC} = +5V ±5%, V_{BH} = -48V, V_{BL} = No connect, PTG = Open, R_{F1} = R_{F2} = 0Ω, Z_T = 120kΩ, R_{LIM} = 38.3kΩ, R_D = 58.8kΩ, RDC_RSG = 20kΩ, R_{OH} = 50kΩ, C_H = 0.47µF, C_{DC} = 1.0µF, $C_{RT/REV}$ = 0.47µf, GND = 0V, RL = 600Ω. Unless Otherwise Specified. (•) symbol used to indicate the test applies to the part. (NA) symbol used to indicate the test does not apply to the part. **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS	HC55120	HC55121	HC55130/1	HC55140/1	HC55142/3	HC55150/1
BATTERY FEED CHARACTERISTICS											
Constant Loop Current Tolerance I_L = 26.5mA, R_{LIM} = 38.3kΩ Forward and Reverse	18mA ≤ IL ≤ 45mA, (Note 27, Figure 10)	$0.92I_L$	I_L	$1.08I_L$	mA	Forward Only	•	Forward Only	•	•	•
Tip Open State TIPX Leakage Current	S = Closed (Figure 11)	-	-	-100	µA	•	•	•	•	•	•
Tip Open State RINGX Leakage Current	R_1 = 0Ω, V_{BH} = -48V R_1 = 2.5kΩ, V_{BH} = -48V (Figure 11)	- -	26.8 17.6	- -	mA mA	•	•	•	•	•	•
Tip Open State RINGX Voltage	5mA<I_{R1} < 26mA (Figure 11)	-	V_{BH} +4.5	-	V	•	•	•	•	•	•
Tip Voltage (Ground Start)	Active State, (S Open) R_1 = 150Ω (Figure 11)	-5	-4	-	V	NA	NA	NA	•	•	NA
Tip Voltage (Ground Start)	Active State, (S Closed) Tip Lead to -48V Through 7kΩ, Ring Lead to Ground Through 150Ω (Figure 11)	-5	-4	-	V	NA	NA	NA	•	•	NA
Open Circuit State Loop Current	(Active) R_L = 0Ω	-100	0	100	µA	•	•	•	•	•	•
LOOP CURRENT DETECTOR											
Programmable Threshold Forward and Reverse	I_{LTh} = (500/ R_D) ≥ 5mA, I_{LTh} = 8.5mA R_D = 58.8kΩ	$0.9•I_{LT}$ Th	I_{LTh}	$1.1•I_{LT}$ Th	mA	Forward Only	•	Forward Only	•	•	•
GROUND KEY DETECTOR											
Ground Key Detector Threshold Tip/Ring Current Difference	Tip Open Active (Note 29, R1 = 2.5kΩ, Figure 12)	5 -	8 20	11 -	mA mA	•	•	NA	•	•	NA
LINE VOLTAGE MEASUREMENT											
Pulse Width ($\overline{GKD_LVM}$)		-	0.36	-	ms/V	NA	NA	NA	•	•	•
RING TRIP DETECTOR (DT, DR)											
Ring Trip Comparator Current	Source Res = 2MΩ	-	2	-	µA	•	•	•	•	•	•
Input Common-Mode Range	Source Res = 2MΩ	-	-	±200	V	•	•	•	•	•	•

Electrical Specifications T_A = -40°C to 85°C, V_{CC} = +5V ±5%, V_{BH} = -48V, V_{BL} = No connect, PTG = Open, R_{F1} = R_{F2} = 0Ω, Z_T = 120kΩ, R_{LIM} = 38.3kΩ, R_D = 58.8kΩ, RDC_RSG = 20kΩ, R_{OH} = 50kΩ, C_H = 0.47µF, C_{DC} = 1.0µF, $C_{RT/REV}$ = 0.47µf, GND = 0V, RL = 600Ω. Unless Otherwise Specified. **(•)** symbol used to indicate the test applies to the part. (NA) symbol used to indicate the test does not apply to the part. **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS	HC55120	HC55121	HC55130/1	HC55140/1	HC55142/3	HC55150/1
RING RELAY DRIVER											
V_{SAT} at 50mA	I_{OL} = 50mA	-	0.3	0.5	V	•	•	•	•	•	•
Off-State Leakage Current	V_{OH} = 13.2V	-	-	10	µA	•	•	•	•	•	•
TEST RELAY DRIVER (TRLY1, TRLY2)											
V_{SAT} at 50mA	I_{OL} = 50mA	-	0.3	0.5	V	NA	NA	NA	NA	NA	NA
Off-State Leakage Current	V_{OH} = 13.2V	-	-	10	µA	NA	NA	NA	NA	NA	NA

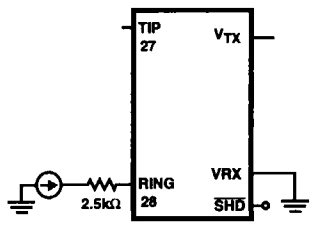


FIGURE 12. GROUND KEY DETECT

DIGITAL INPUTS (C1, C2, C3)											
Input Low Voltage, V_{IL}		0	-	0.8	V	•	•	•	•	•	•
Input High Voltage, V_{IH}		2.0	-	V_{CC}	V	•	•	•	•	•	•
Input Low Current, I_{IL}	V_{IL} = 0.4V	-	-	-50	µA	•	•	•	•	•	•
Input High Current, I_{IH}	V_{IH} = 2.5V	-	25	50	µA	•	•	•	•	•	•
DETECTOR OUTPUTS ($\overline{SHD}$, $\overline{GKD}$_$\overline{LVM}$)											
$\overline{SHD}$ Output Low Voltage, V_{OL} Forward, Reverse and Low Power Standby	I_{OL} = 1mA	-	-	0.5	V	Forward Only	•	Forward Only	•	•	•
$\overline{SHD}$ Output High Voltage, V_{OH} Forward, Reverse and Low Power Standby	I_{OH} = 100µA	2.7	-	-	V	Forward Only	•	Forward Only	•	•	•
$\overline{GKD}$_$\overline{LVM}$ Output Low Voltage, V_{OL} Forward and Tip Open	I_{OL} = 1mA R_1 = 2.5kΩ (Figure 11)	-	-	0.5	V	$\overline{GKD}$	$\overline{GKD}$	NA	$\overline{GKD}$_ $\overline{LVM}$	$\overline{GKD}$_ $\overline{LVM}$	$\overline{LVM}$
$\overline{GKD}$_$\overline{LVM}$ Output High Voltage, V_{OH} Forward and Tip Open	I_{OH} = 100µA	2.7	-	-	V	•$\overline{GKD}$	$\overline{GKD}$	NA	$\overline{GKD}$_ $\overline{LVM}$	$\overline{GKD}$_ $\overline{LVM}$	$\overline{LVM}$
Internal Pull-Up Resistor			15	-	kΩ	•	•	•	•	•	•

Electrical Specifications T_A = -40°C to 85°C, V_{CC} = +5V ±5%, V_{BH} = -48V, V_{BL} = No connect, PTG = Open, R_{F1} = R_{F2} = 0Ω, Z_T = 120kΩ, R_{LIM} = 38.3kΩ, R_D = 58.8kΩ, RDC_RSG = 20kΩ, R_{OH} = 50kΩ, C_H = 0.47µF, C_{DC} = 1.0µF, $C_{RT/REV}$ = 0.47µf, GND = 0V, RL = 600Ω Unless Otherwise Specified. (•) symbol used to indicate the test applies to the part. (NA) symbol used to indicate the test does not apply to the part. **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS	HC55120	HC55121	HC55130/1	HC55140/1	HC55142/3	HC55150/1
POWER DISSIPATION (V_{BH} = -48V, V_{BL} = -24V)											
Open Circuit State Forward and Reverse	C1, C2, C3 = 0, 0,0	-	10	-	mW	Forward Only	•	Forward Only	•	•	•
On-Hook, Low Power Standby Forward and Reverse	C1, C2, C3 = 1, 0, 1	-	15	-	mW	Forward Only	•	Forward Only	•	•	•
On-Hook, Active Forward and Reverse	C1, C2, C3 = 0, 1, 0 I_L = 0mA, Longitudinal Current = 0mA	-	52	-	mW	Forward Only	•	Forward Only	•	•	•
POWER SUPPLY CURRENTS (V_{BH} = -48V, V_{BL} = -24V)											
V_{CC} Current, I_{CC}, Forward and Reverse	Open Circuit State	-	0.95	-	mA	Forward Only	•	Forward Only	•	•	•
V_{BH} Current, I_{BH} Forward and Reverse		-	-0.1	-	mA	Forward Only	•	Forward Only	•	•	•
V_{BL} Current, I_{BL} Forward and Reverse		-	-0.001	-	mA	Forward Only	•	Forward Only	•	•	•
V_{CC} Current, I_{CC} Forward and Reverse	Low Power Standby State I_L = 0mA, Longitudinal Current = 0mA	-	0.95	-	mA	Forward Only	•	Forward Only	•	•	•
V_{BH} Current, I_{BH} Forward and Reverse		-	-0.1	-	mA	Forward Only	•	Forward Only	•	•	•
V_{BL} Current, I_{BL} Forward and Reverse		-	-0.001	-	mA	Forward Only	•	Forward Only	•	•	•
V_{CC} Current, I_{CC} Forward and Reverse	Active State I_L = 0mA, Longitudinal Current = 0mA	-	2.7	-	mA	Forward Only	•	Forward Only	•	•	•
V_{BH} Current, I_{BH} Forward and Reverse		-	-0.8	-	mA	Forward Only	•	Forward Only	•	•	•
V_{BL} Current, I_{BL} Forward and Reverse		-	-0.001	-	mA	Forward Only	•	Forward Only	•	•	•
POWER SUPPLY REJECTION RATIOS											
V_{CC} to 2 or 4 Wire Port Forward and Reverse	Active State R_L = 600Ω 50Hz < f < 3400Hz, V_{IN} =100mV	-	40	-	dB	Forward Only	•	Forward Only	•	•	•
V_{BH} to 2 or 4 Wire Port Forward and Reverse		-	40	-	dB	Forward Only	•	Forward Only	•	•	•
V_{BL} to 2 or 4 Wire Port Forward and Reverse			40	-	dB	Forward Only	•	Forward Only	•	•	•
RFI Rejection	Figure 13, 50kHz≤ f ≤ 100MHz High	-	TBD	-		•	•	•	•	•	•
TEMPERATURE GUARD											
Junction Threshold Temperature		-	160	-	°C	•	•	•	•	•	•

Notes

2. **Overload Level (Two-Wire Port, Off Hook)** - The overload level is specified at the 2-wire port (V_{TR}) with the signal source at the 4-wire receive port (E_{RX}). R_L = 600Ω, $I_{DCMET} \geq$ 18mA. Increase the amplitude of E_{RX} until 1% THD is measured at V_{TR}. Reference Figure 1.

3. **Overload Level (Two-Wire port, On Hook)** - The overload level is specified at the 2-wire port (V_{TR}) with the signal source at the 4-wire receive port (E_{RX}). $R_L = \infty$, I_{DCMET} = 0mA. Increase the amplitude of E_{RX} until 1% THD is measured at V_{TR}. Reference Figure 1.

4. **Longitudinal Impedance** - The longitudinal impedance is computed using the following equations, where TIP and RING voltages are referenced to ground. L_{ZT}, L_{ZR}, V_T, V_R, A_R and A_T are defined in Figure 2.
(TIP) $L_{ZT} = V_T/A_T$
(RING) $L_{ZR} = V_R/A_R$
where: $E_L = 1V_{RMS}$ (0Hz to 100Hz)

5. **Longitudinal Current Limit (On/Off-Hook Active)** - Off-Hook longitudinal current limit is determined by increasing the (60Hz) amplitude of E_L (Figure 3A) until the 2-wire longitudinal current is greater than 28mA$_{RMS}$/Wire. Under this condition, $\overline{SHD}$ pin remains low (no false detection) and the 2-wire to 4-wire longitudinal balance is verified to be greater than 45dB (LB_{2-4} = 20log VTX/E_L).

6. **Longitudinal Current Limit (On-Hook Standby)** - On-Hook longitudinal current limit is determined by increasing the (60Hz) amplitude of E_L (Figure 3B) until the 2-wire longitudinal current is greater than 8.5mA$_{RMS}$/Wire. Under this condition, $\overline{SHD}$ pin remains high (no false detection).

7. **Longitudinal to Metallic Balance** - The longitudinal to metallic balance is computed using the following equation:
BLME = 20 • log (E_L/V_{TR}), where: E_L and V_{TR} are defined in Figure 4.

8. **Metallic to Longitudinal FCC Part 68, Para 68.310** - The metallic to longitudinal balance is defined in this spec.

9. **Longitudinal to Four-Wire Balance** - The longitudinal to 4-wire balance is computed using the following equation:
BLFE = 20 • log (E_L/V_{TX}),: E_L and V_{TX} are defined in Figure 4.

10. **Metallic to Longitudinal Balance** - The metallic to longitudinal balance is computed using the following equation:
BMLE = 20 • log (E_{TR}/V_L), E_{RX} = 0
where: E_{TR}, V_L and E_{RX} are defined in Figure 5.

11. **Four-Wire to Longitudinal Balance** - The 4-wire to longitudinal balance is computed using the following equation:
BFLE = 20 • log (E_{RX}/V_L), E_{TR} = source is removed.
where: E_{RX}, V_L and E_{TR} are defined in Figure 5.

12. **Two-Wire Return Loss** - The 2-wire return loss is computed using the following equation:
r = -20 • log ($2V_M/V_S$)
where: Z_D = The desired impedance; e.g., the characteristic impedance of the line, nominally 600Ω. (Reference Figure 6).

13. **Overload Level (4-Wire port Off-Hook)** - The overload level is specified at the 4-wire transmit port (V_{TX}) with the signal source (E_G) at the 2-wire port, Z_L = 20kΩ, R_L = 600Ω (Reference Figure 7). Increase the amplitude of E_G until 1% THD is measured at V_{TX}. Note the PTG pin is open, and the gain from the 2-wire port to the 4-wire port is equal to 1.

14. **Overload Level (4-Wire port On-Hook)** - The overload level is specified at the 4-wire transmit port (V_{TX}) with the signal source (E_G) at the 2-wire port, Z_L = 20kΩ, $R_L = \infty$ (Reference Figure 7). Increase the amplitude of E_G until 1% THD is measured at V_{TX}. Note the PTG pin is open, and the gain from the 2-wire port to the 4-wire port is equal to 1.

15. **Output Offset Voltage** - The output offset voltage is specified with the following conditions: E_G = 0, R_L = 600Ω, $Z_L = \infty$ and is measured at V_{TX}. E_G, R_L, V_{TX} and Z_L are defined in Figure 7.

16. **Two-Wire to Four-Wire Frequency Response** - The 2-wire to 4-wire frequency response is measured with respect to E_G = 0dBm at 1.0kHz, E_{RX} = 0V (VRX input floating), R_L = 600Ω. The frequency response is computed using the following equation:
F_{2-4} = 20 • log (V_{TX}/V_{TR}), vary frequency from 300Hz to 3.4kHz and compare to 1kHz reading.
V_{TX}, V_{TR}, R_L and E_G are defined in Figure 8.

17. **Four-Wire to Two-Wire Frequency Response** - The 4-wire to 2-wire frequency response is measured with respect to E_{RX} = 0dBm at 1.0kHz, E_G source removed from circuit, R_L = 600Ω. The frequency response is computed using the following equation:
F_{4-2} = 20 • log (V_{TR}/E_{RX}), vary frequency from 300Hz to 3.4kHz and compare to 1kHz reading.
V_{TR}, R_L and E_{RX} are defined in Figure 8.

18. **Four-Wire to Four-Wire Frequency Response** - The 4-wire to 4-wire frequency response is measured with respect to E_{RX} = 0dBm at 1.0kHz, E_G source removed from circuit, R_L = 600Ω. The frequency response is computed using the following equation:
F_{4-4} = 20 • log (V_{TX}/E_{RX}), vary frequency from 300Hz to 3.4kHz and compare to 1kHz reading.
V_{TX}, R_L and E_{RX} are defined in Figure 8.

19. **Two-Wire to Four-Wire Insertion Loss (PTG = Open)** - The 2-wire to 4-wire insertion loss is measured with respect to E_G = 0dBm at 1.0kHz input signal, E_{RX} = 0 (VRX input floating), R_L = 600Ω and is computed using the following equation:
L_{2-4} = 20 • log (V_{TX}/V_{TR})
where: V_{TX}, V_{TR}, R_L and E_G are defined in Figure 8. (Note: The fuse resistors, R_F, impact the insertion loss. The specified insertion loss is for $R_{F1} = R_{F2}$ = 0).

20. **Two-Wire to Four-Wire Insertion Loss (PTG = AGND)** - The 2-wire to 4-wire insertion loss is measured with respect to E_G = 0dBm at 1.0kHz input signal, E_{RX} = 0 (VRX input floating), R_L = 600Ω and is computed using the following equation:
L_{2-4} = 20 • log (V_{TX}/V_{TR})
where: V_{TX}, V_{TR}, R_L and E_G are defined in Figure 8. (Note: The fuse resistors, R_F, impact the insertion loss. The specified insertion loss is for $R_{F1} = R_{F2}$ = 0).

21. **Four-Wire to Two-Wire Insertion Loss** - The 4-wire to 2-wire insertion loss is measured based upon E_{RX} = 0dBm, 1.0kHz input signal, E_G source removed from circuit, R_L = 600Ω and is computed using the following equation:
L_{4-2} = 20 • log (V_{TR}/E_{RX})
where: V_{TR}, R_L and E_{RX} are defined in Figure 8.

22. **Two-Wire to Four-Wire Gain Tracking** - The 2-wire to 4-wire gain tracking is referenced to measurements taken for E_G = -10dBm, 1.0kHz signal, E_{RX} = 0 (VRX output floating), R_L = 600Ω and is computed using the following equation.

    $G_{2\text{-}4} = 20 \bullet \log (V_{TX}/V_{TR})$ vary amplitude -40dBm to +3dBm, or -55dBm to -40dBm and compare to -10dBm reading.

    V_{TX}, R_L and V_{TR} are defined in Figure 8.

23. **Four-Wire to Two-Wire Gain Tracking** - The 4-wire to 2-wire gain tracking is referenced to measurements taken for E_{RX} = -10dBm, 1.0kHz signal, E_G source removed from circuit, R_L = 600Ω and is computed using the following equation:

    $G_{4\text{-}2} = 20 \bullet \log (V_{TR}/E_{RX})$ vary amplitude -40dBm to +3dBm, or -55dBm to -40dBm and compare to -10dBm reading.

    V_{TR}, R_L and E_{RX} are defined in Figure 8. The level is specified at the 4-wire receive port and referenced to a 600Ω impedance level.

24. **Two-Wire Idle Channel Noise** - The 2-wire idle channel noise at V_{TR} is specified with the 2-wire port terminated in 600Ω (R_L) and with the 4-wire receive port (VTX) floating (Reference Figure 9).

25. **Four-Wire Idle Channel Noise** - The 4-wire idle channel noise at V_{TX} is specified with the 2-wire port terminated in 600Ω (R_L). The noise specification is with respect to a 600Ω impedance level at V_{TX}. The 4-wire receive port (VTX) floating (Reference Figure 9).

26. **Harmonic Distortion (2-Wire to 4-Wire)** - The harmonic distortion is measured with the following conditions. E_G = 0dBm at 1kHz, R_L = 600Ω. Measurement taken at V_{TX}. (Reference Figure 7).

27. **Harmonic Distortion (4-Wire to 2-Wire)** - The harmonic distortion is measured with the following conditions. E_{RX} = 0dBm0. Vary frequency between 300Hz and 3.4kHz, R_L = 600Ω. Measurement taken at V_{TR}. (Reference Figure 8).

28. **Constant Loop Current** - The constant loop current is calculated using the following equation:

    $I_L = 1000/R_{LIM} = V_{TR}/600$ (Reference Figure 10).

29. **Ground Key Detector** - (TRIGGER) Ground the Ring pin through a 2.5kΩ resistor and verify that $\overline{GKD}$ goes low.

    (RESET) Disconnect the Ring pin and verify that $\overline{GKD}$ goes high.

    (Hysteresis) Compare difference between trigger and reset.

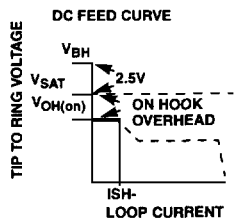
Circuit Operation and Design Information

The UniSLIC14 family of SLIC's operate as a voltage feed current sense subscriber line interface circuit on the 2-wire side, yet appear as a current feed voltage sense SLIC on the 4-wire side. This architecture allows easy implementation of thermal management on the 2-wire side and easy connection to DSP CODEC's on the 4-wire side. Thus, for long loop applications the SLIC provides a programmed constant voltage to the tip and ring terminals while sensing the tip to ring current.

The following discussion separates the SLIC's operation into it's DC and AC paths, then follows up with additional circuit and design information.

DC Feed Curve

The DC feed curve for the UniSLIC14 family is user programmable. The user has complete control over: The on hook and off hook overhead voltages, resistance of the feed curve, minimum open circuit voltage, the value of the current limit and the saturation guard.



The on hook overhead voltage $V_{OH}(on)$ is independent of the V_{BH} battery voltage. So once set, the on hook voltage remains constant as the V_{BH} battery voltage changes. $V_{OH}(on)$ also remains constant over temperature and line leakages up to ISH-. ISH- is equal to 0.6 times the Switch Hook Detect threshold current I_{SHD}. The on hook overhead voltage, required for a given signal level, is calculated with Equation 1,

$$V_{OH(on)} = V_{sp(on)} \times \left(1 + \frac{2R_P + 50}{Z_O}\right) \quad \text{(EQ. 1)}$$

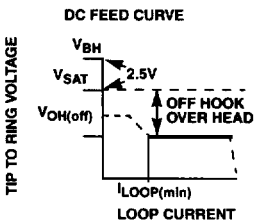
where $V_{OH(on)}$ = On hook overhead voltage

$V_{sp(on)}$ = Required OHT (Vpeak) on hook voltage

R_P = Protection Resistors (Typically 30Ω)

Z_O = Line impedance for (voice)

Reference Figure 13 for R_P and Z_O



The off hook overhead voltage $V_{OH}(off)$ is also independent of the V_{BH} battery voltage and remains constant over temperature. The required off hook overhead voltage is the sum of the voltage drop across the internal sense resistors, the protection resistors, the speech signal and pulse metering signal. The off hook overhead voltage is calculated with Equations 2 and 3.

$$V_{OH(off)} = V_{OH(Rsense)} + V_{OH(sp)} + V_{OH(pm)} \quad \text{(EQ. 2)}$$

where $V_{OH(off)}$ = Off hook overhead voltage

$V_{OH}(R_{sense})$ = Required overhead for voltage drop across sense resistors as a result of the DC loop current (reference Figure 13).

4 TELECOM SLICs

$V_{OH(sp)}$ = Required (peak) off hook voltage for speech.

$V_{OH(pm)}$ = Required (peak) off hook voltage for pulse metering.

$$V_{OH(off)} = 50 \times I_{LOOP(max)} + V_{sp(off)} \times \left(1 + \frac{2R_P + 50}{Z_O}\right) + V_{pm(off)} \times \left(1 + \frac{2R_P + 50}{Z_{pm}}\right) \quad \text{(EQ. 3)}$$

where $I_{LOOP(max)}$ = Desired loop current limit.

$V_{sp(off)}$ = Required (peak) off hook voltage for speech.

$V_{pm(off)}$ = Required (peak) off hook voltage for pulse metering.

Z_{pm} = Line impedance (pulse metering, typically 200Ω).

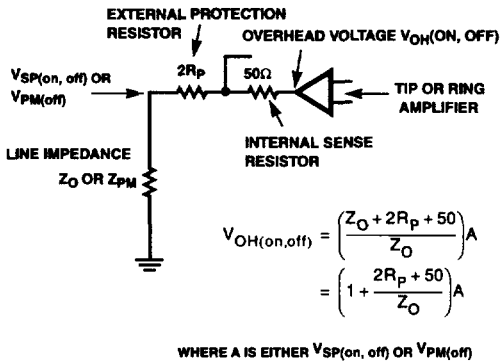
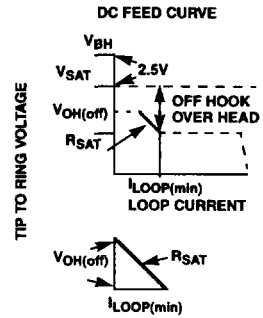


FIGURE 13. OVERHEAD VOLTAGE OF THE TIP AND RING AMPLIFIERS

The Overhead voltage is defined at the output of the tip or ring amplifiers. The off hook overhead voltage requirement is the voltage drop across the internal sense resistors at maximum loop current, plus the required voltage for both speech and pulse metering. The two protection resistors (R_P) are considered as part of the load.

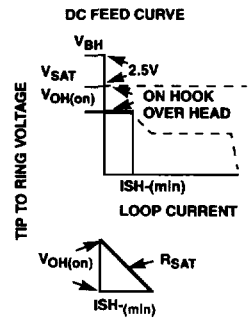


For a constant current design, the R_{SAT} resistance of the DC feed curve is equal to the V_{OH}(off) voltage divided by the minimum loop current requirement (Equation 4).

The external saturation guard resistor RDC_RSG can now be calculated and is given in Equation 5.

$$R_{SAT} = \frac{V_{OH(off)}}{I_{LOOP(min)}} \quad \text{(EQ. 4)}$$

$$RDC_RGS = 50 \times R_{SAT} \quad \text{(EQ. 5)}$$



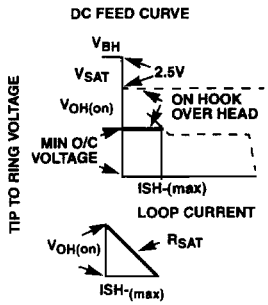
The minimum ISH- is equal to V_{OH}(on) divided by R_{SAT} as shown in Equation 6.

ISH- is used to find the minimum and maximum Switch Hook Detect thresholds (I_{SHD}) for a given design. The minimum $I_{SHD(min)}$ is established by the on hook overhead voltage requirement. The maximum $I_{SHD(max)}$ is established by the minimum open circuit voltage requirement.

$$ISH\text{-}min = \frac{V_{OH(on)}}{R_{SAT}} = \frac{V_{SP(on)} \times \left(1 + \frac{2R_P + 50}{Z_O}\right)}{R_{SAT}} \quad \text{(EQ. 6)}$$

The minimum Switch Hook Detect threshold current ($I_{SHD(min)}$) is defined by Equation 7.

$$I_{SHD(min)} = 1.7 \times ISH\text{-}(min) \quad \text{(EQ. 7)}$$



The maximum ISH- is determined by the minimum open circuit voltage requirement (Typical value is -43 volts).

Equation 8 determines the maximum ISH- allowed for a given minimum open circuit voltage.

$$ISH\text{-}(max) = \frac{V_{BH}\text{-}V_{SAT}\text{-}V_{O/C}}{R_{SAT}} \quad \text{(EQ. 8)}$$

The maximum Switch Hook Detect Current threshold is defined by Equation 9.

$$I_{SHD(MAX)} = 1.7 \times ISH\text{-}(max) \quad \text{(EQ. 9)}$$

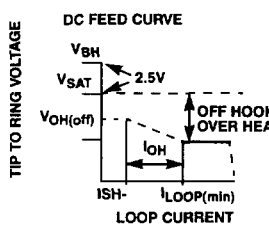
The above analysis establishes a range for the Switch Hook Detect threshold current to meet the selected requirements. After selecting an I_{SHD} threshold between the $I_{SHD(min)}$ and $I_{SHD(max)}$, the programming resistor is determined by Equation 10.

$$R_D = \frac{500}{I_{SHD}} \quad \text{(EQ. 10)}$$

The true value of ISH-, for the selected value of I_{SHD} is given by Equation 11:

$$ISH\text{-} = I_{SHD}\ (0.6) \quad \text{(EQ. 11)}$$

Verify that the value of ISH- is above the suspected line leakage of the application. The UniSLIC family will provide a constant on hook voltage level for leakage currents up to this value of line leakage.



The ROH resistor, which is used to set the offhook overhead voltage, is calculated using Equation 12.

IOH is the difference between the $I_{LOOP(min)}$ and ISH-.

$$R_{OH(max)} = \frac{500}{IOH} = \frac{500}{I_{LOOP(min)}\text{-}ISH\text{-}} \quad \text{(EQ. 12)}$$

The current limit is set by a single resistor and is calculated using Equation 13:

$$R_{LIM} = \frac{1000}{I_{LOOP(max)}} \quad \text{(EQ. 13)}$$

The maximum loop resistance for the given conditions is calculated by Equation 14.

$$R_{LOOP(max)} = \frac{V_{BH}\text{-}V_{SAT}}{I_{LOOP(min)}} \text{-}50\text{-}\frac{V_{SP(off)}}{I_{LOOP(min)}} \times \left(1 + \frac{2R_P + 50}{Z_0}\right) - \frac{V_{PM(off)}}{I_{LOOP(min)}} \times \left(1 + \frac{2R_P + 50}{Z_{PM}}\right) \text{-}2R_P \quad \text{(EQ. 14)}$$

SLIC in the Standby Mode

Overall system power is saved by configuring the SLIC in the standby state when not in use. In the standby state the tip and ring amplifiers are disabled and internal resistors are connected between tip to ground and ring to V_{BH}. This connection enables a loop current to flow when the phone goes off hook. The loop current detector then detects this current and the $\overline{SHD}$ pin goes low.

SLIC in the Active Mode

Figure 14 shows a simplified AC transmission model. Circuit analysis yields the following design equations:

Node Equation

$$\frac{V_{RX}}{500K} - \frac{V_A}{1000K} = I_X \quad \text{(EQ. 15)}$$

Loop Equation

$$I_X 500k - V_{TX'} = I_X 500k = 0 \quad \text{(EQ. 16)}$$

Loop Equation

$$V_{TR}\text{-}I_M 2R_P + V_{TX'} = 0 \quad \text{(EQ. 17)}$$

where:

V_{RX} = Is the input voltage at the VRX pin.

V_A = Is an internal node voltage that is a function of the loop current detector and the impedance matching networks

I_X = Internal current in the SLIC that is the result between the input receive current and the feedback current.

I_M = Is the AC metallic current.

R_P = Is a fuse resistor.

Z_T = Is used to set the SLIC's 2-wire impedance.

V_{TX}' = Is the tip to ring voltage at the output pins of the SLIC.

V_{TR} = Is the tip to ring voltage including the voltage across the protection resistors.

Z_L = Is the line impedance.

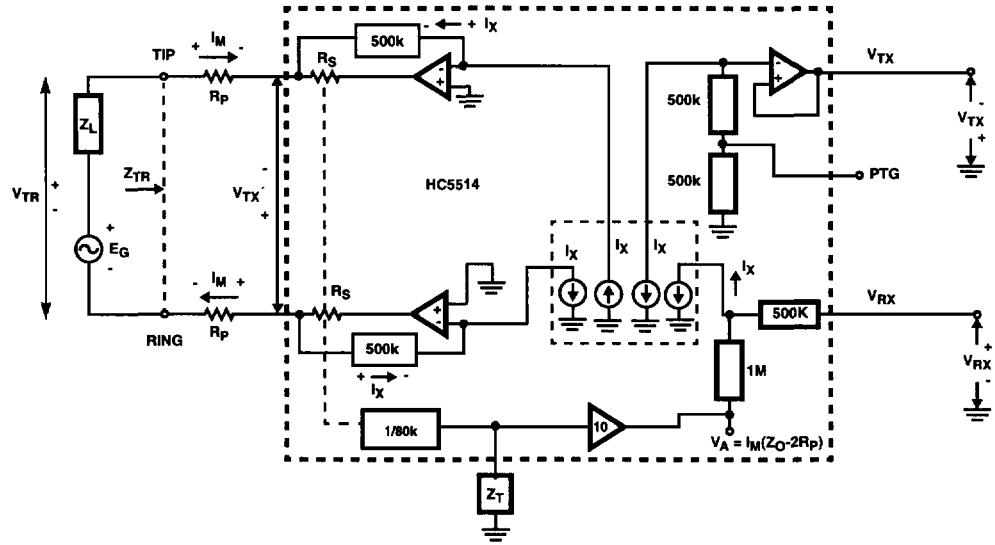


FIGURE 14. SIMPLIFIED AC TRANSMISSION CIRCUIT

(AC) 4-Wire to 2-Wire Gain

The 4-wire to 2-wire gain is equal to V_{TR}/V_{RX}.

From Equations 15, 16 and 17 with $E_G = 0$.

$$A_{4\text{-}2} = -2\frac{Z_L}{Z_O + Z_L} \quad \text{(EQ. 18)}$$

(AC) 2-Wire to 4-Wire Gain

The 2-wire to 4-wire gain is equal to V_{TX}/E_G with $V_{RX} = 0$.

$$A_{2\text{-}4} = \frac{V_{TX}}{E_G} = -\frac{Z_O - 2R_P}{Z_O + Z_L} \quad \text{(EQ. 19)}$$

(AC) 4-Wire to 4-Wire Gain

The 4-wire to 4-wire gain is equal to V_{TX}/V_{RX}.

From Equations 15, 16 and 17 with $E_G = 0$.

$$A_{4-4} = \frac{V_{TX}}{V_{RX}} = 2\left(\frac{Z_L - 2R_P}{Z_L + Z_0}\right) \quad \text{(EQ. 20)}$$

(AC) 2-Wire Impedance

The AC 2-wire impedance (Z_{TR}) is the impedance looking into the SLIC, including the fuse resistors. The formula to calculate the proper Z_T for matching the 2-wire impedance is shown in Equation 21.

$$Z_T = 200 \bullet (Z_{TR} - 2R_P) \quad \text{(EQ. 21)}$$

Equation 21 can now be used to match the SLIC's impedance to any known line impedance (Z_{TR}).

EXAMPLE:

Calculate Z_T to make $Z_{TR} = 600\Omega$ in series with 2.16µF. $R_P = 30\Omega$.

$$Z_T = 200 \bullet \left(600 + \frac{1}{j\omega \bullet 2.16 \bullet 10^{-6}} - 2 \bullet 30\right) \quad \text{(EQ. 22)}$$

$Z_T = 114k\Omega$ in series with 0.0108µF.

Layout Considerations

Floating the PTG Pin:

The PTG pin is a high impedance pin that is used to reduce the 2-wire to 4-wire gain to 0dB. If 0dB is required, it is necessary to float the PTG pin. The PC board interconnect should be as short as possible to minimize stray capacitance on this pin. Stray capacitance on this pin forms a low pass filter and will cause the 2-wire to 4-wire gain to roll off at the higher frequencies.

If a 2-wire to 4-wire gain of -6dB is required in the design, the PTG pin should be grounded at the pin.

Layout of the 2-Wire Impedance Matching Resistor Z_T:

Proper connection to this pin is to have the external Z_T network as close to the pin as possible.

The Z_T pin is a high impedance pin that is used to set the proper feedback for matching the impedance of the 2-wire side. This will eliminate circuit board capacitance on this pin to maintain the 2-wire return loss across frequency.

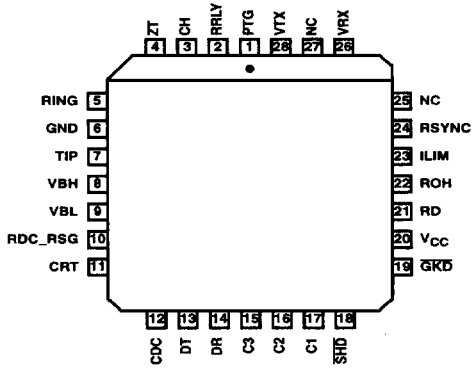
SPM Pin:

For optimum performance, the PC board interconnect connected to the SPM pin should be as short as possible.

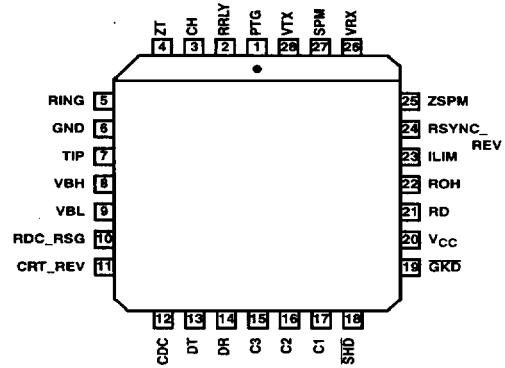
TABLE 1. DETECTOR STATES

STATE	C3	C2	C1	SLIC OPERATING STATE	ACTIVE DETECTOR	OUTPUT	
						SHD	GKD_ LVM
0	0	0	0	Open Circuit State		HIGH	HIGH
1	0	0	1	Ringing State	Ring Trip Detector	↓	HIGH
2	0	1	0	Forward Active State	Loop Current Detector	↓	
					Ground Key Detector		↓
3	0	1	1	Test Active State Requires previous state to be in the Forward Active state to determine the On hook or Off hook status of the line.	**On Hook** Loopback Detector	LOW	
					Ground Key Detector		↓
					On Hook Loop Current Detector	LOW	
					Line Voltage Detector		⎍
4	1	0	0	Tip Open State	Ground Key Detector	↓	↓
5	1	0	1	Low Power Standby State	Loop Current Detector	↓	
					Ground Key Detector		↓
6	1	1	0	Reverse Active State	Loop Current Detector	↓	
					Ground Key Detector		↓
7	1	1	1	Test Reversal Active State Requires previous state to be in the Reverse Active state to determine the On hook or Off hook status of the line.	**On Hook** Loop Current Detector	↓	HIGH
					On Hook Loop Current Detector	LOW	
					Line Voltage Detector		⎍
8	X	X	X	Thermal Shutdown		LOW	LOW

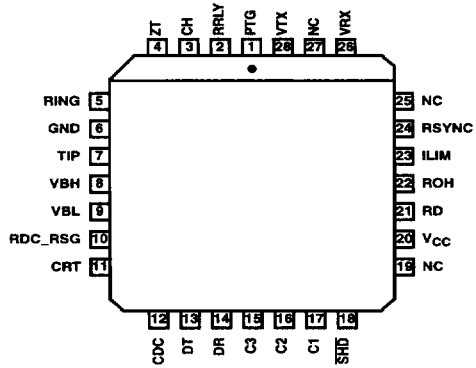
HC55120
(28 PIN PLCC)
TOP VIEW



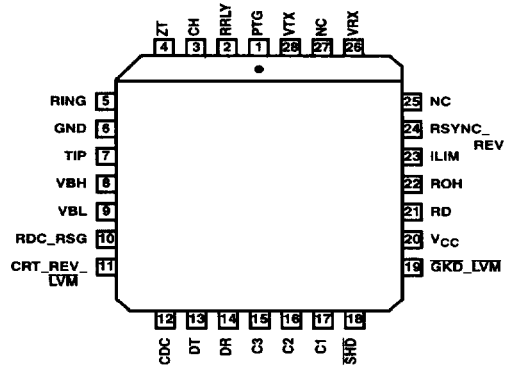
HC55121
(28 PIN PLCC)
TOP VIEW



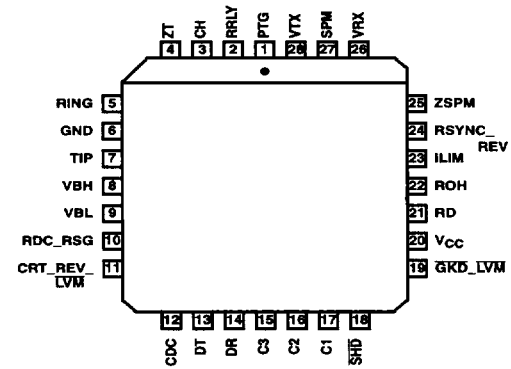
HC55130
(28 PIN PLCC)
TOP VIEW



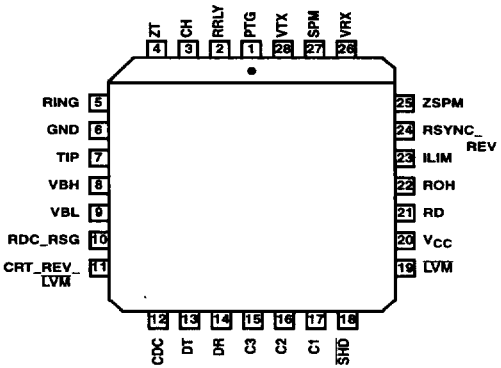
HC55140
(28 PIN PLCC)
TOP VIEW



HC55142
(28 PIN PLCC)
TOP VIEW

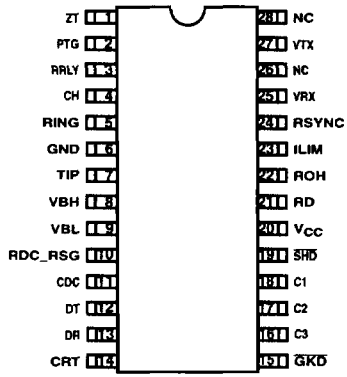


HC55150
(28 PIN PLCC)
TOP VIEW

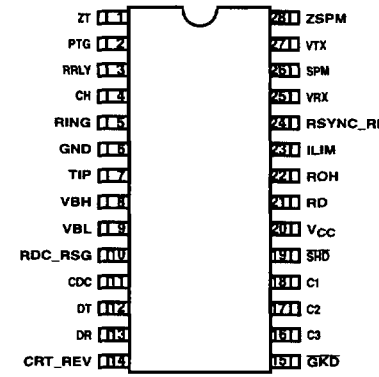


Pinouts SOIC Packages

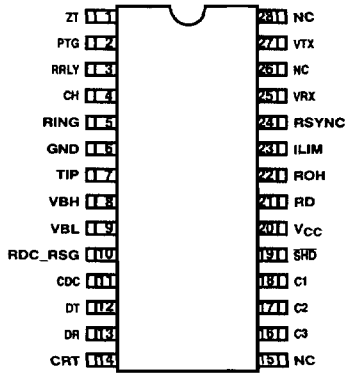
HC55120
(28 PIN SOIC)
TOP VIEW



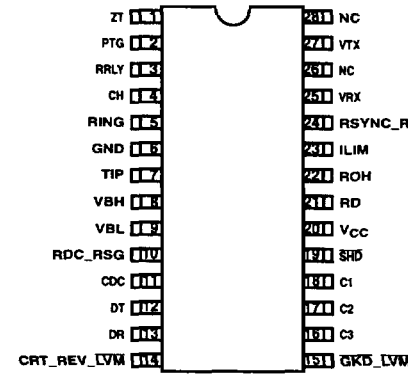
HC55121
(28 PIN SOIC)
TOP VIEW



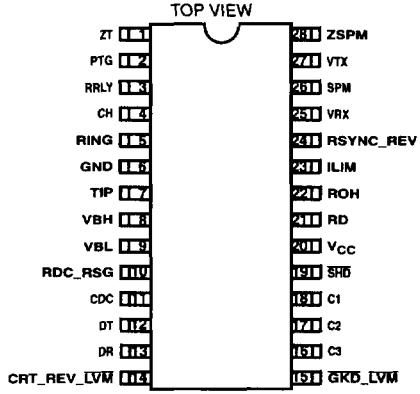
HC55130
(28 PIN SOIC)
TOP VIEW



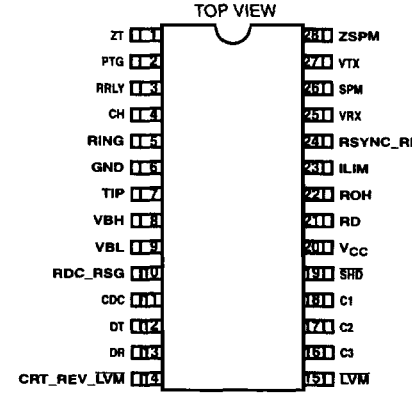
HC55140
(28 PIN SOIC)
TOP VIEW



HC55142
(28 PIN SOIC)
TOP VIEW



HC55150
(28 PIN SOIC)
TOP VIEW



Pin Descriptions

28 PIN PLCC	32 PIN PLCC	28 PIN SOIC	SYMBOL	DESCRIPTION
1	1	2	PTG	Programmable Transmit Gain - The 2-wire to 4-wire transmission gain is 0dB if this pin is left floating and -6.02dB if tied to ground. The -6.02dB gain option is useful in systems where Pulse Metering is used. See Figure 14.
2	2	3	RRLY	Ring Relay Driver Output - The relay coil may be connected to a maximum of 14 volts.
3	3	4	CH	AC/DC Separation Capacitor - CH is required to properly process the AC current from the DC loop current. Recommended value 0.47µF.
4	4	1	ZT	2-Wire Impedance Matching Pin - Impedance matching of the 2-wire side is accomplished by placing an impedance between the Z_T pin and ground. See Equation 21.
5	5	5	RING	Connects via protection resistors (R_P reference Figure 15 - 18) to ring wire of subscriber pair.
6	6	6	GND	Analog and Digital ground.
7	7	7	TIP	Connects via protection resistors (R_P reference Figure 19) to tip wire of subscriber pair.
8	8	8	V_{BH}	High Battery Supply (negative with respect to GND pin 6).
9	9	9	V_{BL}	Low Battery Supply (negative with respect to GND pin 6, magnitude $\leq V_{BH}$).
10	10	10	RDC_RSG	Resistive Feed/Saturation Guard - Performs the saturation guard function on constant current designs and sets the slope of the resistive feed curve for constant voltage designs.
11	11	14	CRT_REV _$\overline{LVM}$	Ring Trip, Soft Polarity Reversal and Line Voltage Measurement - A capacitor when placed between the CRT_REV_$\overline{LVM}$ pin and ground performs 3 mutually exclusive functions. When the SLIC is configured in the Ringing mode it provides filtering of the ringing signal to prevent false detect. When the SLIC is transitioning between the Forward Active State and Reverse Active State it provides Soft Polarity Reversal and performs charge storage in the Line Voltage Measurement State. Recommended value 0.47µF.
12	12	11	CDC	Filter Capacitor- The CDC Capacitor removes the VF signals from the battery feed control loop.
13	13	12	DT	Tip side of Ring Trip Detector - Ring trip detection is accomplished by connecting an external network to a detector in the SLIC with inputs DT and DR. Ring trip occurs when the voltage on DT is more negative than the voltage on DR.
14	14	13	DR	Ring Side of Ring Trip Detector - Ring trip detection is accomplished by connecting an external network to a detector in the SLIC with inputs DT and DR. Ring trip occurs when the voltage on DR is more positive than the voltage on DT.
-	15	-	C5	Activates Test Relay TRLY1.
-	16	-	C4	Activates Test Relay TRLY2.
15	17	16	C3	TTL Compatible Logic Input. The logic states of C1, C2 and C3 determine the operating states of the SLIC. Reference Table 1 for details.
16	18	17	C2	TTL Compatible Logic Input. The logic states of C1, C2 and C3 determine the operating states of the SLIC. Reference Table 1 for details.
17	19	18	C1	TTL Compatible Logic Input. The logic states of C1, C2 and C3 determine the operating states of the SLIC. Reference Table 1 for details.
18	20	19	$\overline{SHD}$	Switch Hook Detect - Active during off hook, ground key and loopback. Reference Table 1 for details.
19	21	15	GKD_$\overline{LVM}$	Ground Key Detector and Line Voltage Measurement - Reference Table 1 for details.
20	22	20	VCC	5V Supply.

Pin Descriptions (Continued)

28 PIN PLCC	32 PIN PLCC	28 PIN SOIC	SYMBOL	DESCRIPTION
21	23	21	RD	Loop Current Threshold Programming Pin - A resistor between this pin and ground will determine the trigger level for the loop current detect circuit. See Equation 10.
22	24	22	ROH	Off Hook Overload Setting Resistor - Used to set combined overhead for voice and pulse metering signals. See Equation 12.
23	25	23	ILIM	Current Limit Programming Pin - A resistor between this pin and ground will determine the constant current limit of the feed curve. See Equation 13.
24	26	24	RSYNC_REV	Ring Synchronization Input and Reversal Time Setting. A resistor between this pin and GND (pin 6) determines the polarity reversal time. Synchronization of the closing of the relay to connect the ringing signal to the subscriber pair is achieved via the grounding of this pin.
25	27	28	ZSPM	Pulse Metering Signal Impedance Pin - A resistor on the input of this pin will allow programming of the source impedance of the pulse metering signal for maximum signal on the 2-wire loop.
26	28	25	VRX	Receive Input - Ground referenced 4-wire side.
27	29	26	SPM	Pulse Metering Signal Input.
28	30	27	VTX	Transmit Output - Ground referenced 4-wire side.
-	31	-	TRLY1	Test Relay Driver 1.
-	32	-	TRLY2	Test Relay Driver 2.

Basis Application Circuit — Voice Only 28 Pin PLCC Package

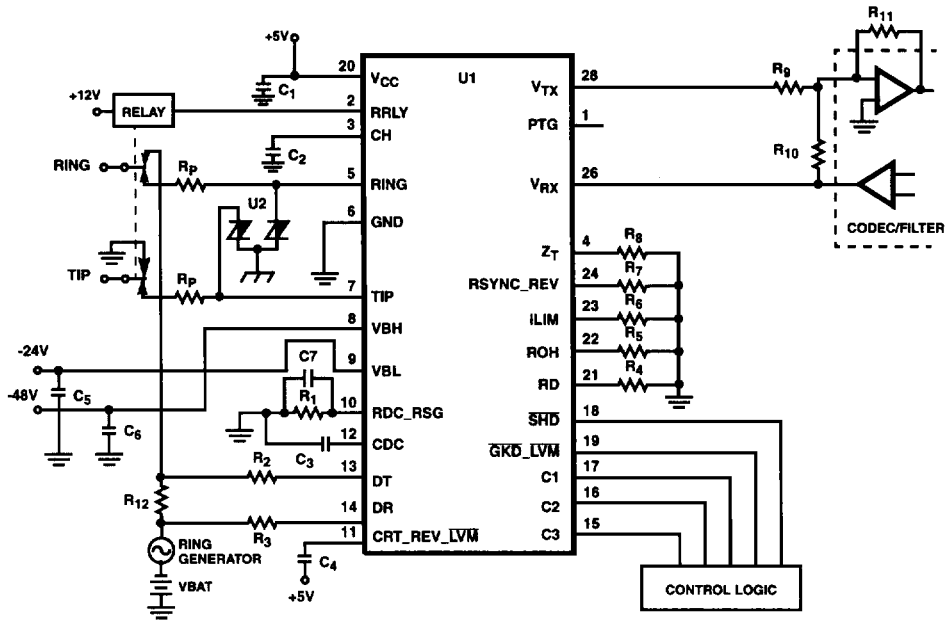


FIGURE 15. UniSLIC14 VOICE ONLY BASIC APPLICATION CIRCUIT

TABLE 2. BASIC APPLICATION CIRCUIT COMPONENT LIST

COMPONENT	VALUE	TOLERANCE	RATING
U1 - SLIC	UniSLIC14 Family	N/A	N/A
U2 - Dual Asymmetrical Transient Voltage Suppressor	TISP1072F3	N/A	N/A
RP (Line Feed Resistors)	30Ω	Matched 1%	2.0W
R1 (RDC_RSG Resistor)	13kΩ	1%	1/4W
R2, R3	2 MegΩ	1%	1/4W
R4 (RD Resistor)	43.2kΩ	1%	1/4W
R5 (ROH Resistor)	37.4kΩ	1%	1/4W
R6 (RILIM Resistor)	33.2kΩ	1%	1/4W
R7 (RSYNC_REV Resistor)	34.8kΩ	1%	1/4W
R8 (RZT Resistor)	107kΩ	1%	1/4W
R9, R10, R11	20kΩ	1%	1/4W
R12	400Ω	5%	2W
C1	0.1µF + 1.0µF	20%	10V
C5	0.1µF + 1.0µF	20%	50V
C6	0.1µF + 1.0µF	20%	100V
C2, C4, C7	0.47µF	20%	10V
C3	2.2µF	20%	50V

Design Parameters: Maximum onhook voltage = 0.775V_{RMS}, Maximum Offhook Voice = 3.1Vpeak, Switch Hook Threshold = 11.6mA, Loop Current Limit = 29.6mA, Synthesize Device Impedance = 600 -60 = 540Ω, with 30Ω protection resistors, impedance across Tip and Ring terminals = 600Ω. Where applicable, these component values apply to the Basic Application Circuits for the HC55120, HC55121, HC55130, HC55140, HC55142 and HC55150. Pins not shown in the Basic Application Circuit are no connect (NC) pins.

Basis Application Circuit — Pulse Metering 28 Pin PLCC Package

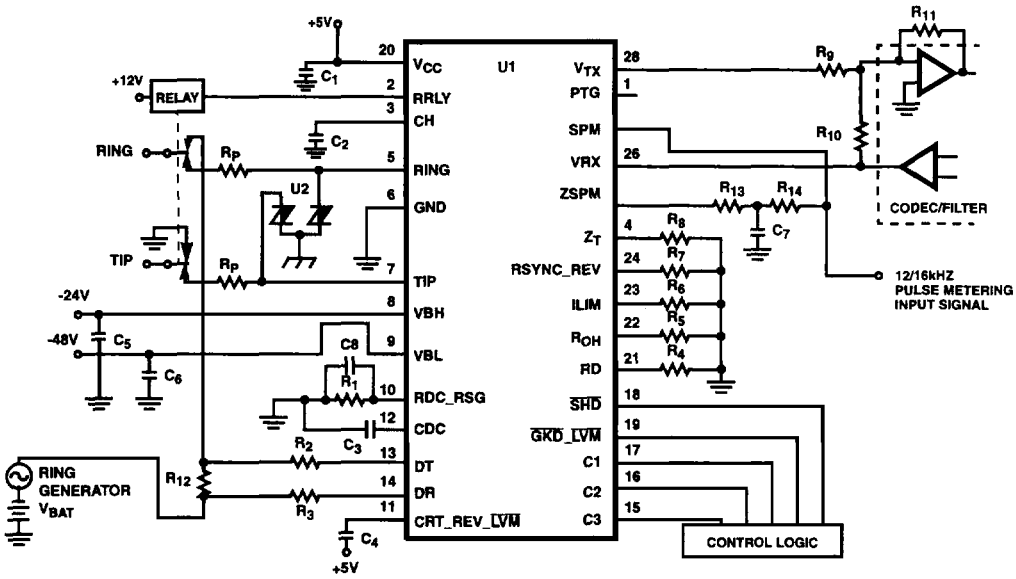


FIGURE 16. UniSLIC14 PULSE METERING BASIC APPLICATION CIRCUIT

TABLE 3. BASIC APPLICATION CIRCUIT COMPONENT LIST

COMPONENT	VALUE	TOLERANCE	RATING
U1 - SLIC	UniSLIC14 Family	N/A	N/A
U2 - Dual Asymmetrical Transient Voltage Suppressor	TISP1072F3	N/A	N/A
RP (Line Feed Resistors)	30Ω	Matched 1%	2.0W
R1 (RDC_RSG Resistor)	19.1kΩ	1%	1/4W
R2, R3	2 MegΩ	1%	1/4W
R4 (RD Resistor)	51.1kΩ	1%	1/4W
R5 (ROH Resistor)	34.8kΩ	1%	1/4W
R6 (RILIM Resistor)	33.2kΩ	1%	1/4W
R7 (RSYNC_REV Resistor)	34.8kΩ	1%	1/4W
R8 (RZT Resistor)	107kΩ	1%	1/4W
R9, R10, R11	20kΩ	1%	1/4W
R12	400Ω	5%	2W
R13, R14	10.7kΩ	1%	1/4W
C1	0.1µF + 1.0µF	20%	10V
C5	0.1µF + 1.0µF	20%	50V
C6	0.1µF + 1.0µF	20%	100V
C2, C4, C8	0.47µF	20%	10V
C3	2.2µF	20%	50V
C7	680pF	10%	10V

Design Parameters: Maximum onhook voltage = 0.775V_{RMS}, Maximum offhook voice = 1.1Vpeak, Maximum simultaneous pulse metering signal = 3.1Vpeak, Switch Hook Threshold = 9.8mA, Loop Current Limit = 29.6mA, Synthesize Device Impedance = 600-60 = 540Ω, with 30Ω protection resistors, impedance across Tip and Ring terminals = 600Ω. Where applicable, these component values apply to the Basic Application Circuits for the HC55120, HC55121, HC55130, HC55140, HC55142 and HC55150. Pins not shown in the Basic Application Circuit are no connect (NC) pins.

Basis Application Circuit

Voice Only 28 Pin SOIC Package

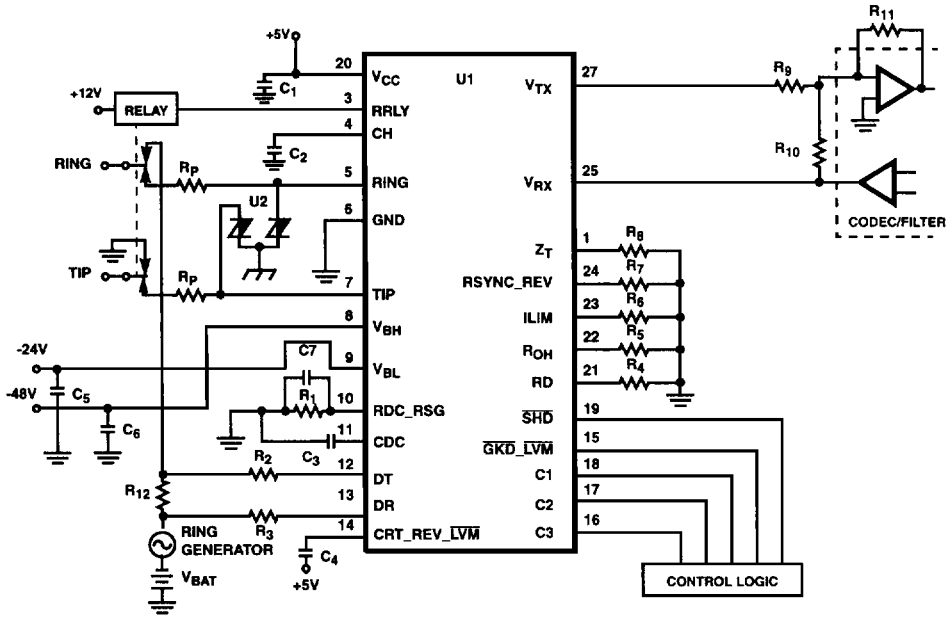


FIGURE 17. UniSLIC14 VOICE ONLY BASIC APPLICATION CIRCUIT

TABLE 4. BASIC APPLICATION CIRCUIT COMPONENT LIST

COMPONENT	VALUE	TOLERANCE	RATING
U1 - SLIC	UniSLIC14 Family	N/A	N/A
U2 - Dual Asymmetrical Transient Voltage Suppressor	TISP1072F3	N/A	N/A
RP (Line Feed Resistors)	30Ω	Matched 1%	2.0W
R1 (RDC_RSG Resistor)	13kΩ	1%	1/4W
R2, R3	2 MegΩ	1%	1/4W
R4 (RD Resistor)	43.2kΩ	1%	1/4W
R5 (ROH Resistor)	37.4kΩ	1%	1/4W
R6 (RILIM Resistor)	33.2kΩ	1%	1/4W
R7 (RSYNC_REV Resistor)	34.8kΩ	1%	1/4W
R8 (RZT Resistor)	107kΩ	1%	1/4W
R9, R10, R11	20kΩ	1%	1/4W
R12	400Ω	5%	2W
C1	0.1µF + 1.0µF	20%	10V
C5	0.1µF + 1.0µF	20%	50V
C6	0.1µF + 1.0µF	20%	100V
C2, C4, C7	0.47µF	20%	10V
C3	2.2µF	20%	50V

Design Parameters: Maximum onhook voltage = 0.775V_{RMS}, Maximum offhook voice = 3.1Vpeak, Switch Hook Threshold = 11.6mA, Loop Current Limit = 29.6mA, Synthesize Device Impedance = 600-60 = 540Ω, with 30Ω protection resistors, impedance across Tip and Ring terminals = 600Ω. Where applicable, these component values apply to the Basic Application Circuits for the HC55120, HC55121, HC55130, HC55140, HC55142 and HC55150. Pins not shown in the Basic Application Circuit are no connect (NC) pins.

Basis Application Circuit

Pulse Metering 28 Pin SOIC Package

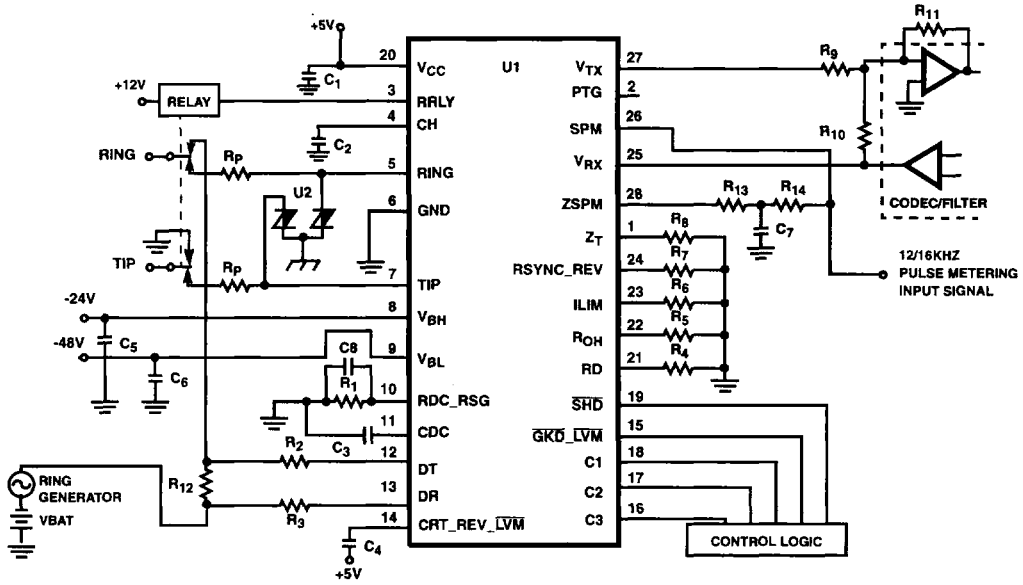


FIGURE 18. UniSLIC14 PULSE METERING BASIC APPLICATION CIRCUIT

TABLE 5. BASIC APPLICATION CIRCUIT COMPONENT LIST

COMPONENT	VALUE	TOLERANCE	RATING
U1 - SLIC	UniSLIC14 Family	N/A	N/A
U2 - Dual Asymmetrical Transient Voltage Suppressor	TISP1072F3	N/A	N/A
RP (Line Feed Resistors)	30Ω	Matched 1%	2.0W
R1 (RDC_RSG Resistor)	19.1kΩ	1%	1/4W
R2, R3	2 MegΩ	1%	1/4W
R4 (RD Resistor)	51.1kΩ	1%	1/4W
R5 (ROH Resistor)	34.8kΩ	1%	1/4W
R6 (RILIM Resistor)	33.2kΩ	1%	1/4W
R7 (RSYNC_REV Resistor)	34.8kΩ	1%	1/4W
R8 (RZT Resistor)	107kΩ	1%	1/4W
R9, R10, R11	20kΩ	1%	1/4W
R12	400Ω	5%	2W
R13, R14	10.7kΩ	1%	1/4W
C1	0.1µF + 1.0µF	20%	10V
C5	0.1µF + 1.0µF	20%	50V
C6	0.1µF + 1.0µF	20%	100V
C2, C4, C8	0.47µF	20%	10V
C3	2.2µF	20%	50V
C7	680pF	10%	10V

Design Parameters: Maximum onhook voltage = 0.775V_{RMS}, Maximum offhook voice = 1.1Vpeak, Maximum simultaneous pulse metering signal = 3.1Vpeak, Switch Hook Threshold = 9.8mA, Loop Current Limit = 29.6mA, Synthesize Device Impedance = 600-60 = 540Ω, with 30Ω protection resistors, impedance across Tip and Ring terminals = 600Ω. Where applicable, these component values apply to the Basic Application Circuits for the HC55120, HC55121, HC55130, HC55140, HC55142 and HC55150. Pins not shown in the Basic Application Circuit are no connect (NC) pins.