

N-channel 100 V, 9.0 mΩ typ., 110 A STripFET™ II Power MOSFETs in D<sup>2</sup>PAK, TO-220 and TO-247 packages

Datasheet - production data

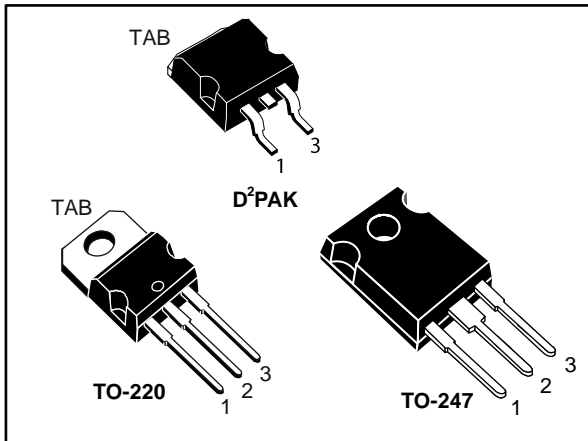
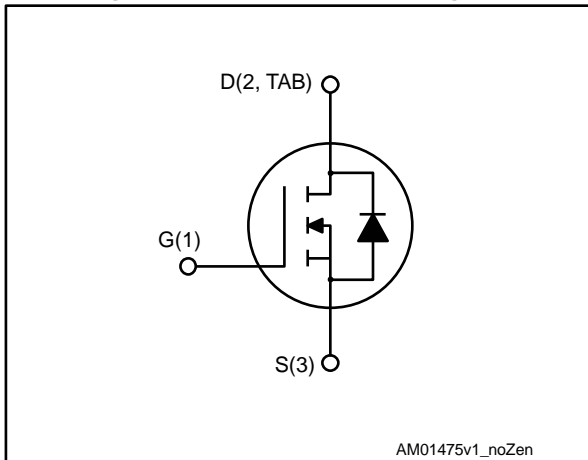


Figure 1: Internal schematic diagram



## Features

Order code	V <sub>DS</sub>	R <sub>DS(on)</sub> max.	I <sub>D</sub>
STB120NF10T4	100 V	10.5 mΩ	110 A
STP120NF10			
STW120NF10			

- Exceptional dv/dt capability
- 100% avalanche tested
- Low gate charge

## Applications

- Switching applications

## Description

These Power MOSFETs have been developed using STMicroelectronics' unique STripFET process, which is specifically designed to minimize input capacitance and gate charge. This renders the devices suitable for use as primary switch in advanced high-efficiency isolated DC-DC converters for telecom and computer applications, and applications with low gate charge driving requirements.

Table 1: Device summary

Order code	Marking	Package	Packing
STB120NF10T4	B120NF10	D <sup>2</sup> PAK	Tape and reel
STP120NF10	P120NF10	TO-220	Tube
STW120NF10	120NF10	TO-247	

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# 1 Electrical ratings

**Table 2: Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	100	V
$V_{GS}$	Gate-source voltage	$\pm 20$	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	110	A
	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	77	A
$I_{DM}^{(1)}$	Drain current (pulsed)	440	A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	312	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	10	V/ns
$E_{AS}^{(3)}$	Single pulse avalanche energy	550	mJ
$T_j$	Operating junction temperature range	-55 to 175	$^\circ\text{C}$
$T_{stg}$	Storage temperature range		

**Notes:**

<sup>(1)</sup>Pulse width is limited by safe operating area.

<sup>(2)</sup> $I_{SD} \leq 110\text{ A}$ ,  $di/dt \leq 300\text{ A}/\mu\text{s}$ ,  $V_{DD} = 80\% V_{(BR)DSS}$

<sup>(3)</sup>Starting  $T_j = 25\text{ }^\circ\text{C}$ ,  $I_D = 60\text{ A}$ ,  $V_{DD} = 50\text{ V}$

**Table 3: Thermal data**

Symbol	Parameter	Value			Unit
		TO-220	TO-247	D <sup>2</sup> PAK	
$R_{thj-case}$	Thermal resistance junction-case	0.48			$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient	62.5			$^\circ\text{C}/\text{W}$
$R_{thj-pcb}$	Thermal resistance junction-pcb <sup>(1)</sup>	35			$^\circ\text{C}/\text{W}$

**Notes:**

<sup>(1)</sup>When mounted on an 1-inch<sup>2</sup> FR-4, 2 Oz copper board.

## 2 Electrical characteristics

(T<sub>CASE</sub> = 25 °C unless otherwise specified)

**Table 4: On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source breakdown voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	100			V
I <sub>DSS</sub>	Zero gate voltage drain current	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 100 V			1	μA
		V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 100 V, T <sub>c</sub> = 125 °C <sup>(1)</sup>			10	μA
I <sub>GSS</sub>	Gate-source leakage current	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±20 V			±100	nA
V <sub>GS(th)</sub>	Gate threshold voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	2		4	V
R <sub>DS(on)</sub>	Static drain-source on-resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 60 A		9.0	10.5	mΩ

**Notes:**

<sup>(1)</sup>Defined by design, not subject to production test.

**Table 5: Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C <sub>iss</sub>	Input capacitance	V <sub>DS</sub> = 25 V, f = 1 MHz, V <sub>GS</sub> = 0 V	-	5200		pF
C <sub>OSS</sub>	Output capacitance			785		pF
C <sub>rSS</sub>	Reverse transfer capacitance			325		pF
Q <sub>g</sub>	Total gate charge	V <sub>DD</sub> = 80 V, I <sub>D</sub> = 120 A, V <sub>GS</sub> = 0 to 10 V (see <a href="#">Figure 14: "Test circuit for gate charge behavior"</a> )	-	172	233 <sup>(1)</sup>	nC
Q <sub>gs</sub>	Gate-source charge			32		nC
Q <sub>gd</sub>	Gate-drain charge			64		nC

**Notes:**

<sup>(1)</sup>Defined by design, not subject to production test.

**Table 6: Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t <sub>d(on)</sub>	Turn-on delay time	V <sub>DD</sub> = 50 V, I <sub>D</sub> = 60 A, R <sub>G</sub> = 4.7 Ω, V <sub>GS</sub> = 10 V (see <a href="#">Figure 13: "Test circuit for resistive load switching times"</a> and <a href="#">Figure 18: "Switching time waveform"</a> )	-	25	-	ns
t <sub>r</sub>	Rise time		-	90	-	ns
t <sub>d(off)</sub>	Turn-off delay time		-	132	-	ns
t <sub>f</sub>	Fall time		-	68	-	ns

Table 7: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source drain current		-		110	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		440	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 120 \text{ A}$ , $V_{GS} = 0 \text{ V}$	-		1.3	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 120 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$ , $V_{DD} = 40 \text{ V}$ , $T_j = 150 \text{ }^\circ\text{C}$ (see <a href="#">Figure 15: "Test circuit for inductive load switching and diode recovery times"</a> )	-	152		ns
$Q_{rr}$	Reverse recovery charge		-	760		nC
$I_{RRM}$	Reverse recovery current		-	10		A

**Notes:**

<sup>(1)</sup>Pulse width is limited by safe operating area.

<sup>(2)</sup>Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

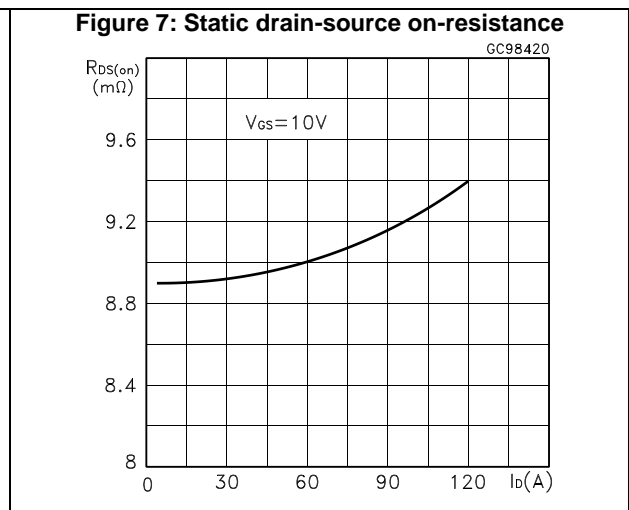
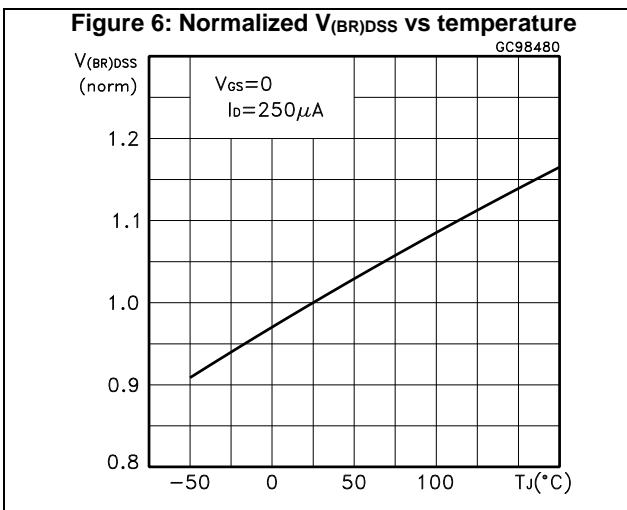
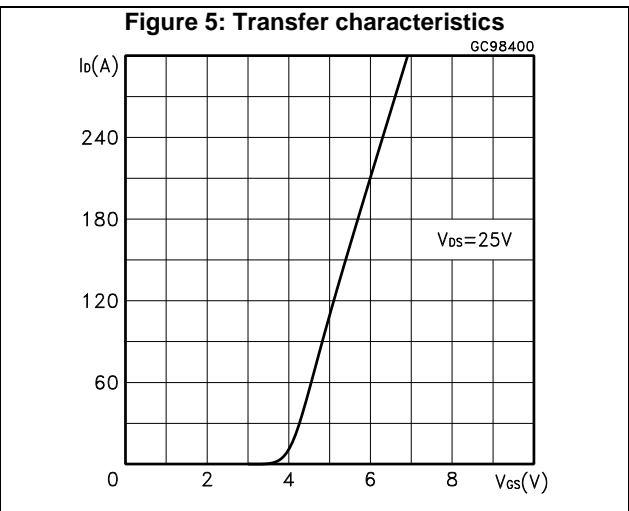
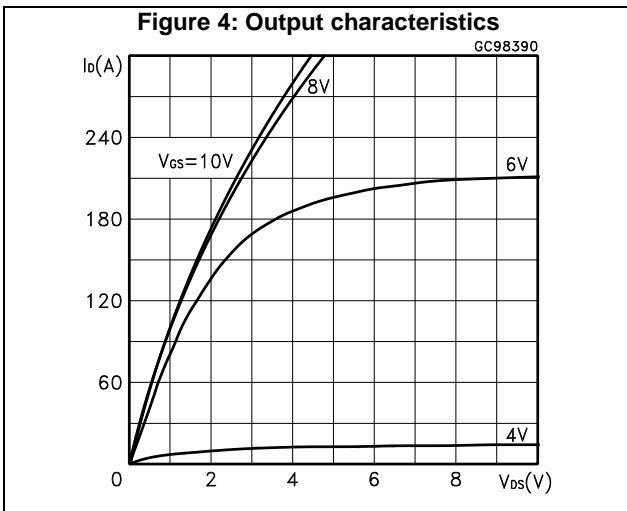
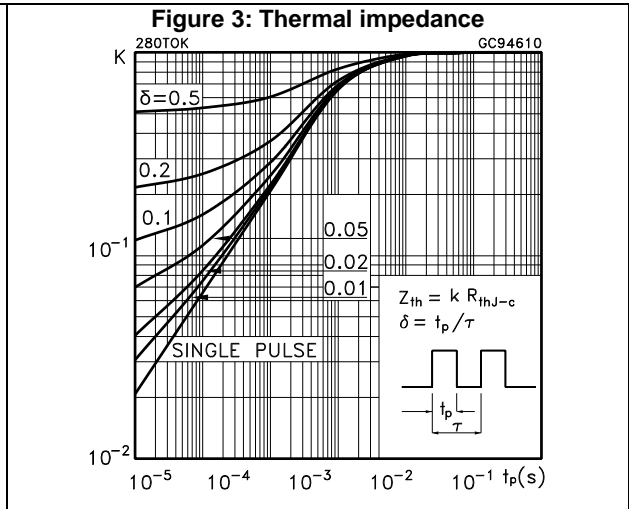
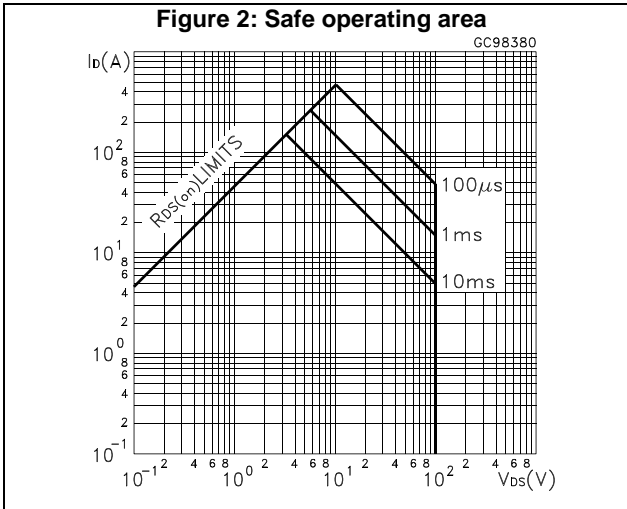


Figure 8: Gate charge vs gate-source voltage

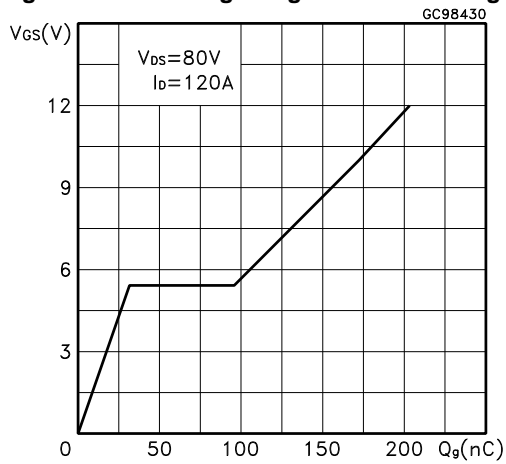


Figure 9: Capacitance variations

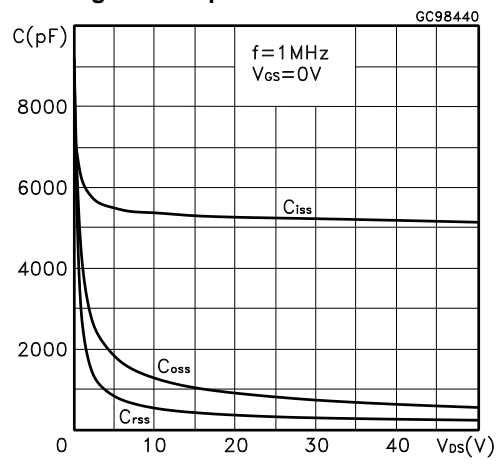


Figure 10: Normalized gate threshold voltage vs temperature

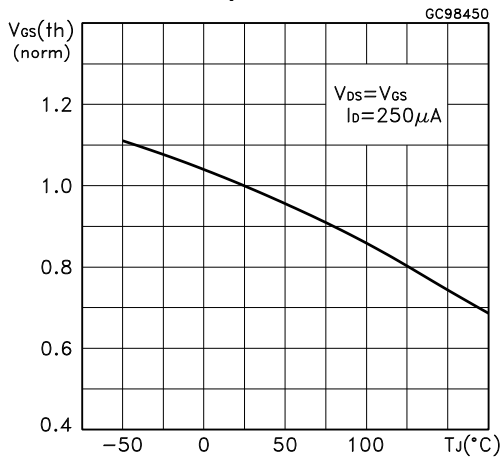


Figure 11: Normalized on-resistance vs temperature

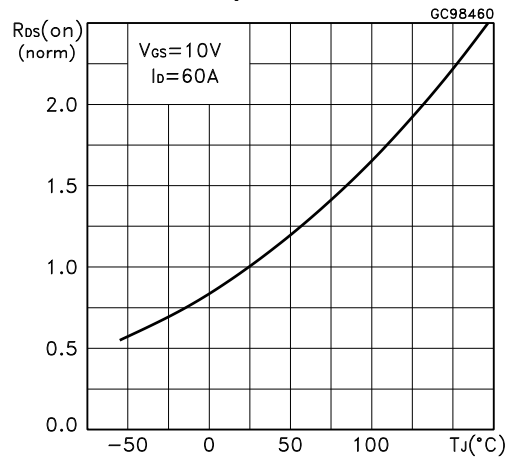
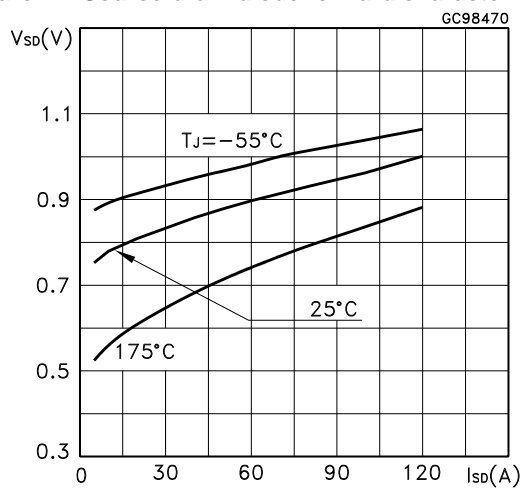


Figure 12: Source-drain diode forward characteristics



### 3 Test circuits

**Figure 13: Test circuit for resistive load switching times**



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**Figure 14: Test circuit for gate charge behavior**



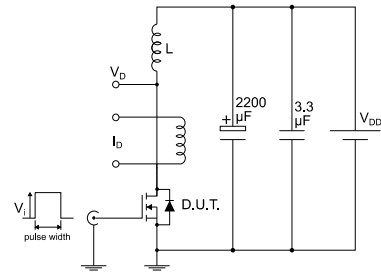
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**Figure 15: Test circuit for inductive load switching and diode recovery times**



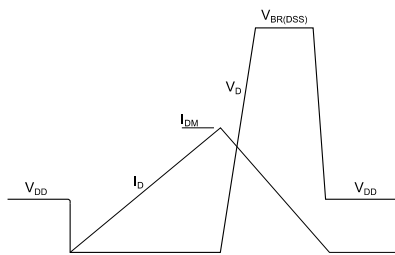
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**Figure 16: Unclamped inductive load test circuit**



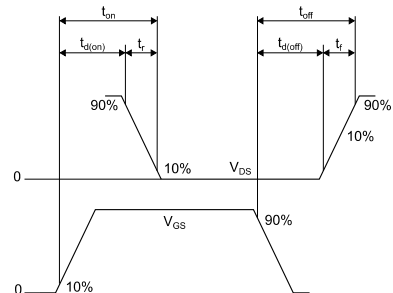
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**Figure 17: Unclamped inductive waveform**



AM01472v1

**Figure 18: Switching time waveform**



AM01473v1



## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

### 4.1 D<sup>2</sup>PAK (TO-263) type A2 package information

Figure 19: D<sup>2</sup>PAK (TO-263) type A2 package outline

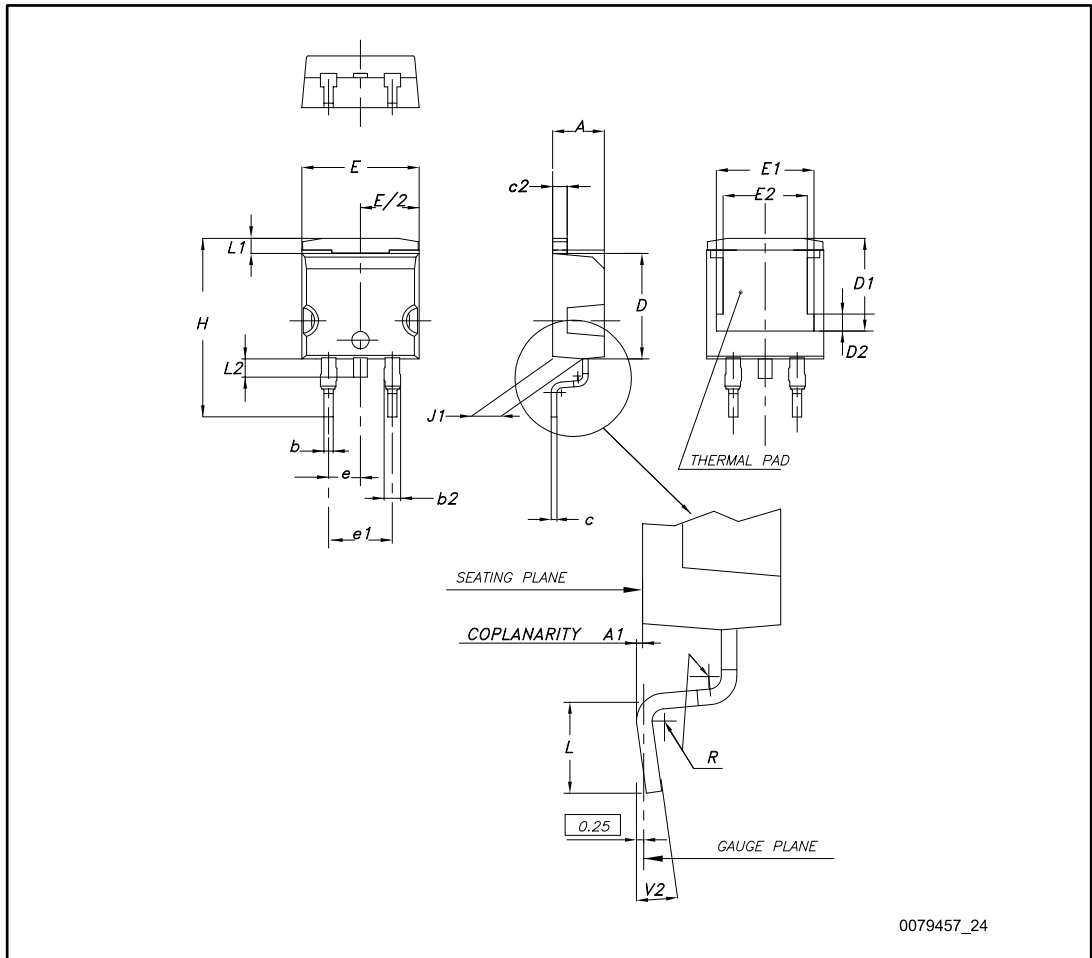
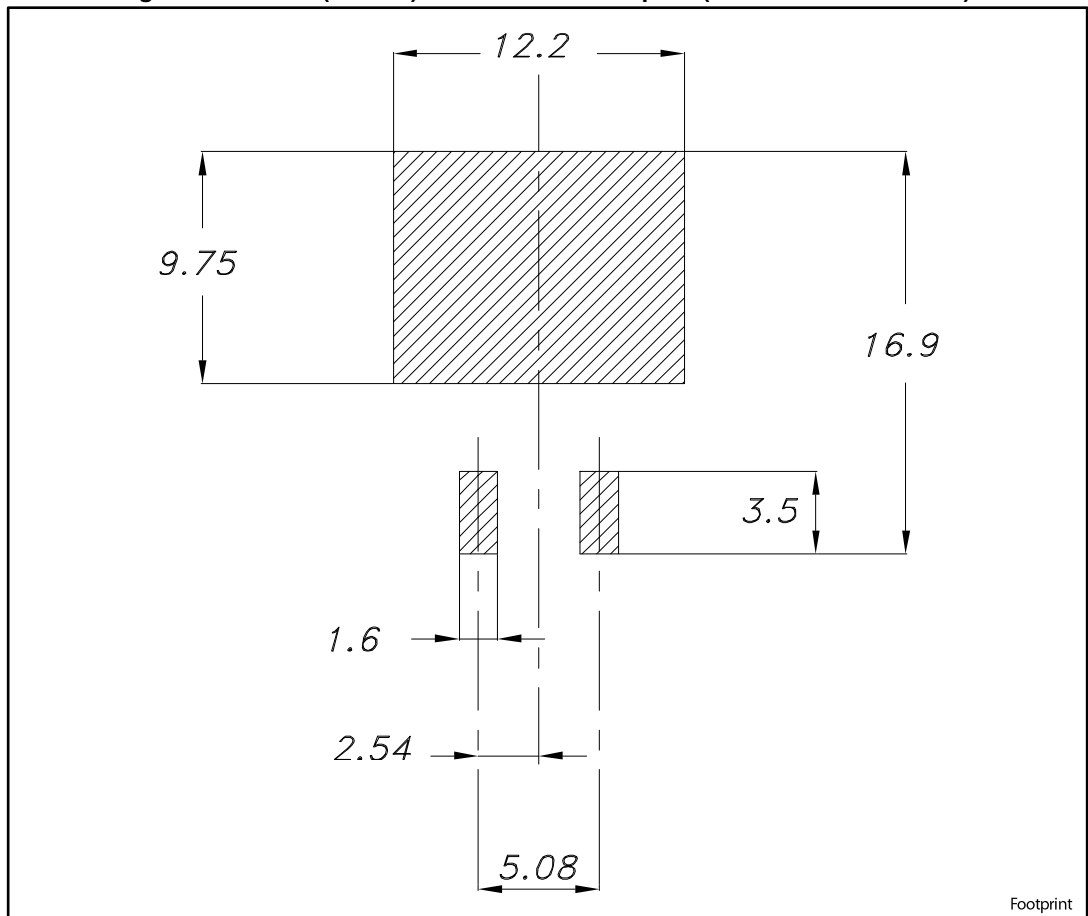


Table 8: D<sup>2</sup>PAK (TO-263) type A2 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50	7.75	8.00
D2	1.10	1.30	1.50
E	10.00		10.40
E1	8.70	8.90	9.10
E2	7.30	7.50	7.70
e		2.54	
e1	4.88		5.28
H	15.00		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.40	
V2	0°		8°

Figure 20: D<sup>2</sup>PAK (TO-263) recommended footprint (dimensions are in mm)



### 4.2 D<sup>2</sup>PAK packing information

Figure 21: D<sup>2</sup>PAK tape outline

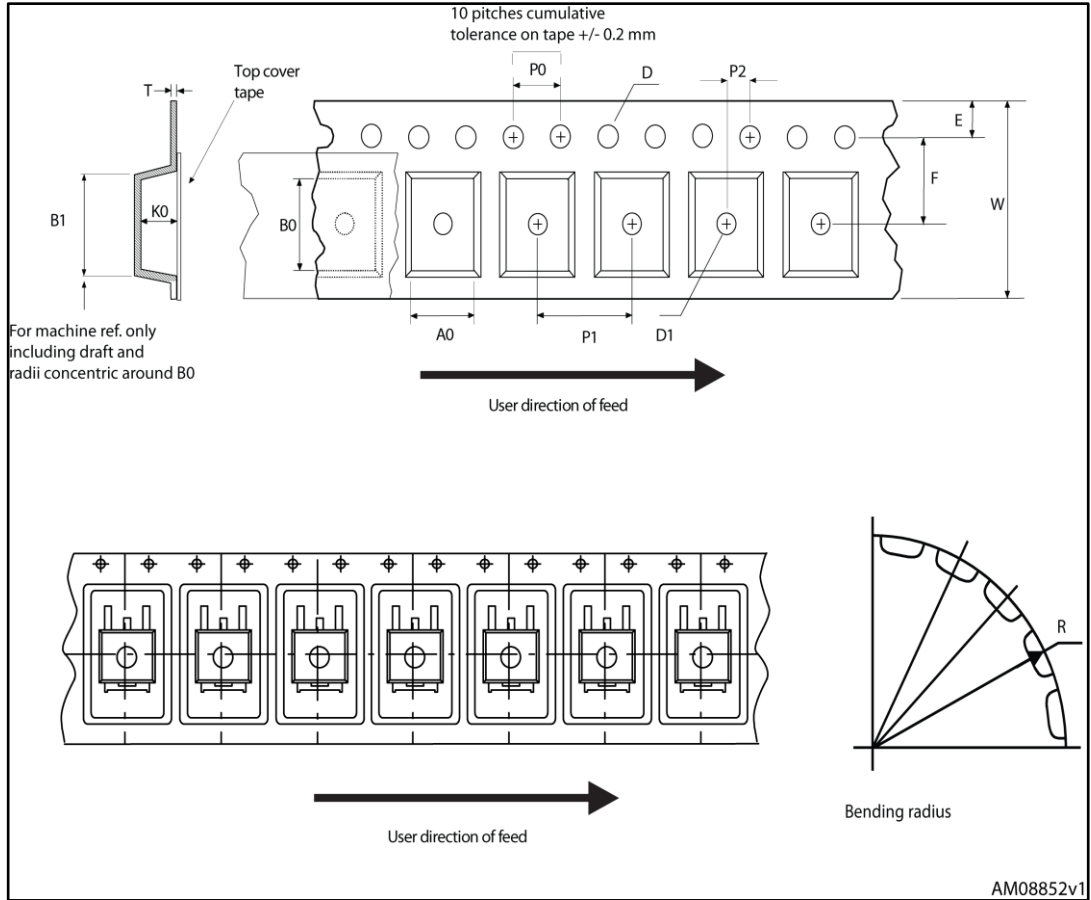
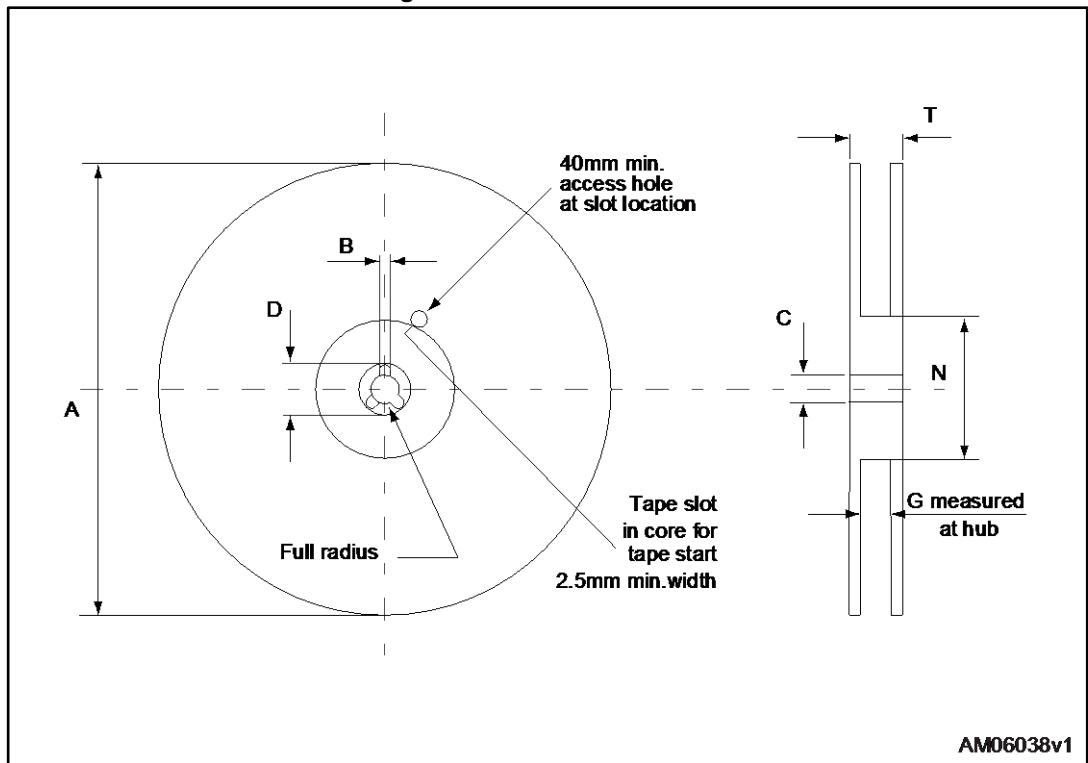


Figure 22: D<sup>2</sup>PAK reel outline



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Table 9: D<sup>2</sup>PAK tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base quantity		1000
P2	1.9	2.1	Bulk quantity		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

### 4.3 TO-220 package information

Figure 23: TO-220 type A package outline

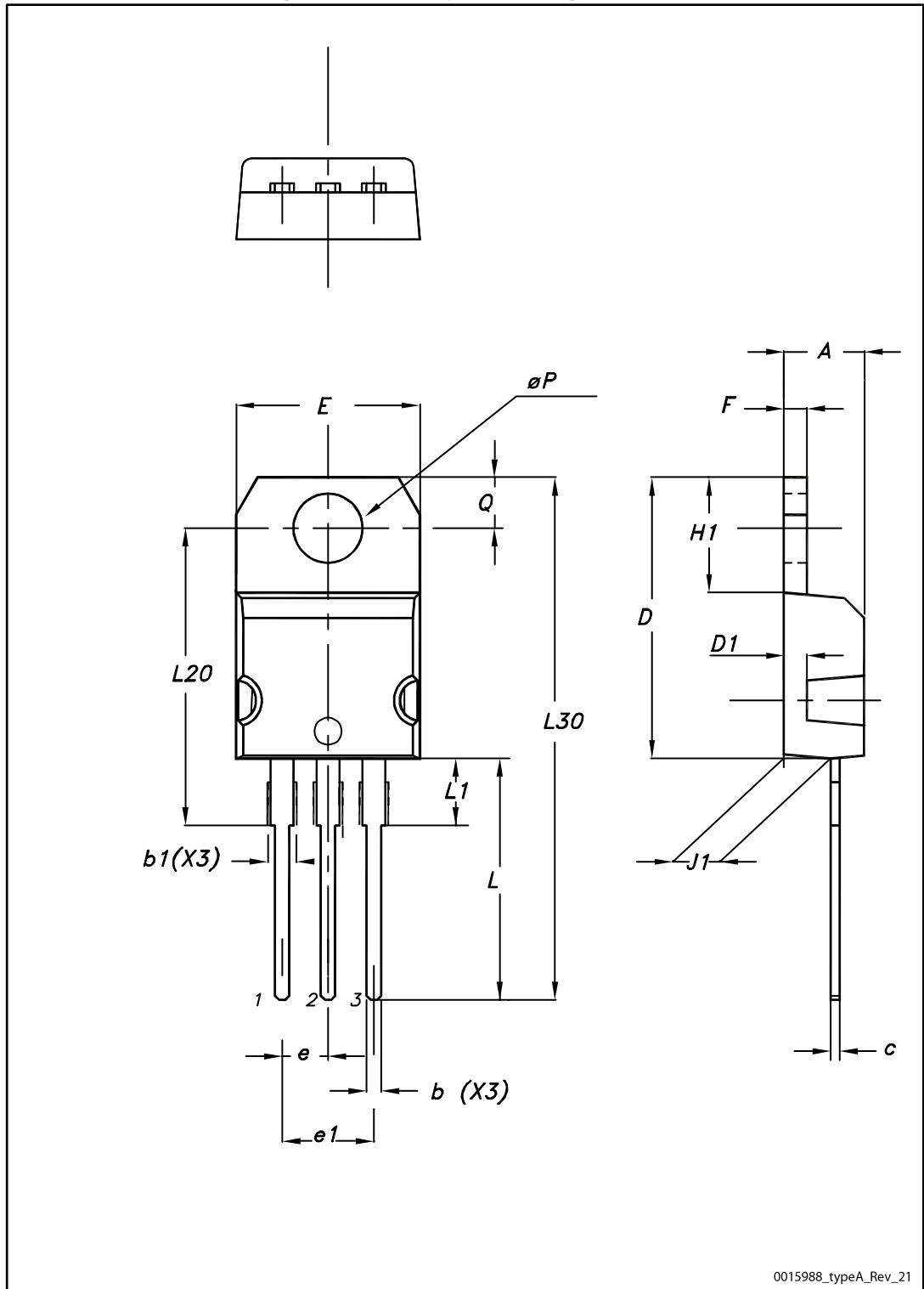


Table 10: TO-220 type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95

### 4.4 TO-247 package information

Figure 24: TO-247 package outline

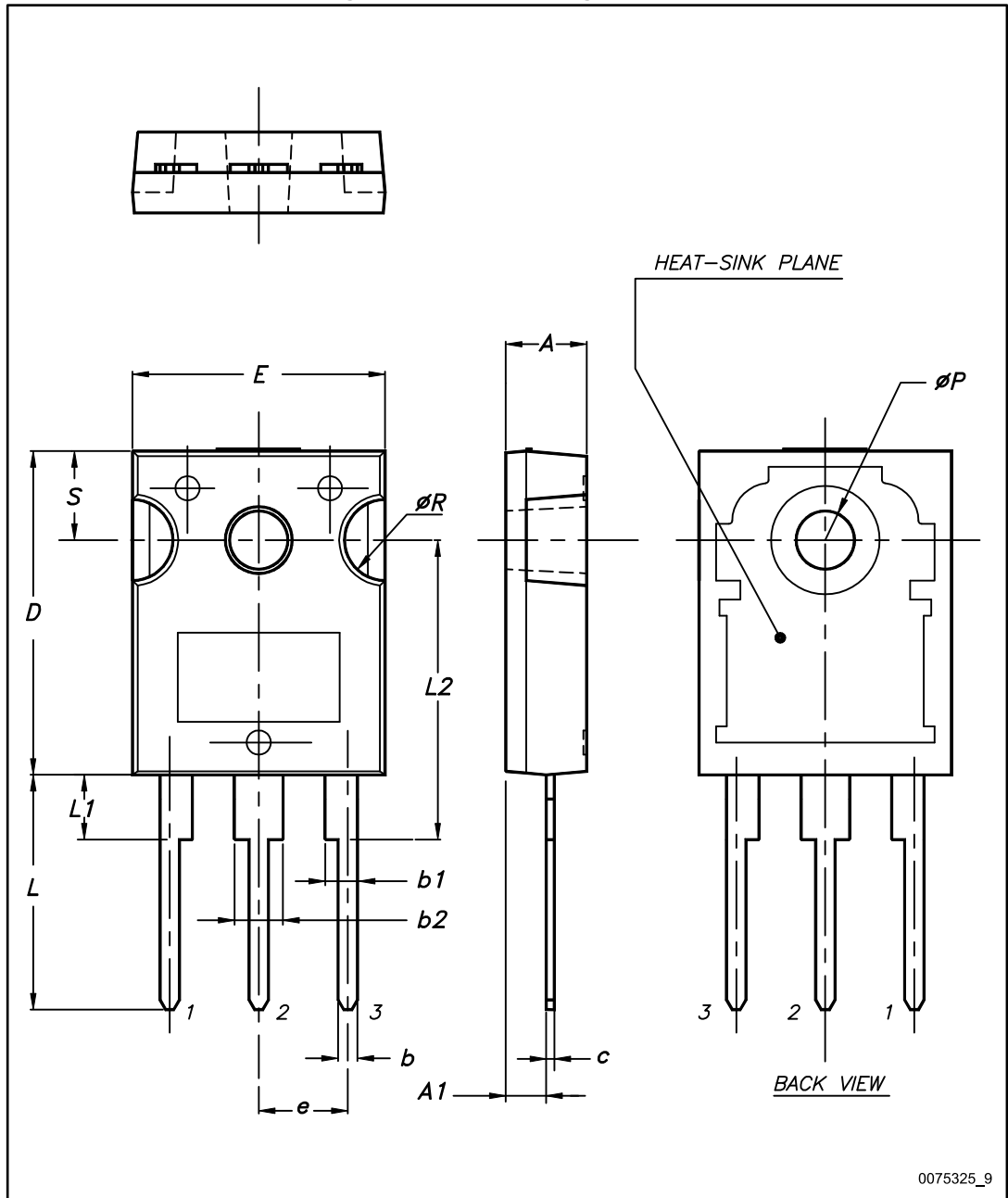




Table 11: TO-247 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70

## 5 Revision history

Table 12: Document revision history

Date	Revision	Changes
20-Mar-2006	2	Preliminary datasheet
31-Mar-2006	3	Typing error
19-Jun-2006	4	New template, no content change
28-Jun-2006	5	New I <sub>D</sub> value on <i>Table 2</i>
05-Oct-2006	6	New value on <i>Table 7</i>
11-May-2011	7	Added new package and mechanical data: TO-220FP
03-Nov-2017	8	Part number STF120NF10 has been moved to a separate datasheet. Updated features, description and device summary on cover page. Updated <i>Table 2: "Absolute maximum ratings"</i> , <i>Table 3: "Thermal data"</i> and <i>Table 4: "On/off states"</i> . Updated <i>Section 4: "Package information"</i> . Minor text changes

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