



# PMDPB80XP

20 V, dual P-channel Trench MOSFET

Rev. 1 — 30 May 2012

Product data sheet

## 1. Product profile

### 1.1 General description

Dual P-channel enhancement mode Field-Effect Transistor (FET) in a small and leadless ultra thin DFN2020-6 (SOT1118) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

### 1.2 Features and benefits

- 1.8 V  $R_{DSon}$  rated for low voltage gate drive
- Trench MOSFET technology
- Small and leadless ultra thin SMD plastic package: 2 x 2 x 0.65 mm
- Exposed drain pad for excellent thermal conduction

### 1.3 Applications

- Charging switch for portable devices
- DC/DC converters
- Small brushless DC motor drive
- Power management in battery-driven portables
- Hard disc and computing power management

### 1.4 Quick reference data

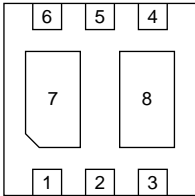
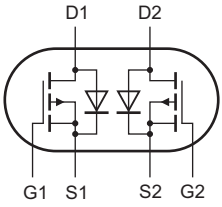
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Per transistor</b>						
$V_{DS}$	drain-source voltage	$T_j = 25\text{ °C}$	-	-	-20	V
$V_{GS}$	gate-source voltage		-12	-	12	V
$I_D$	drain current	$V_{GS} = -4.5\text{ V}$ ; $T_{amb} = 25\text{ °C}$ ; $t \leq 5\text{ s}$	[1]	-	-3.7	A
<b>Static characteristics (per transistor)</b>						
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = -4.5\text{ V}$ ; $I_D = -2.7\text{ A}$ ; $T_j = 25\text{ °C}$	-	80	102	m $\Omega$

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm<sup>2</sup>.

## 2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source TR1	 <p>Transparent top view SOT1118 (DFN2020-6)</p>	 <p>017aaa258</p>
2	G1	gate TR1		
3	D2	drain TR2		
4	S2	source TR2		
5	G2	gate TR2		
6	D1	drain TR1		
7	D1	drain TR1		
8	D2	drain TR2		

## 3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMDPB80XP	DFN2020-6	plastic thermal enhanced ultra thin small outline package; no leads; 6 terminals	SOT1118

## 4. Marking

Table 4. Marking codes

Type number	Marking code
PMDPB80XP	1U

## 5. Limiting values

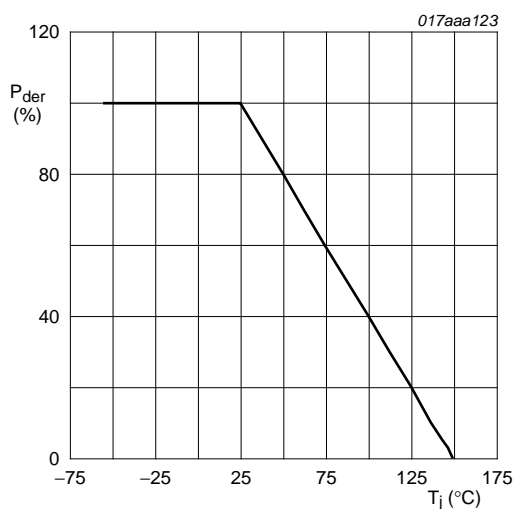
**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit	
<b>Per transistor</b>						
$V_{DS}$	drain-source voltage	$T_j = 25\text{ °C}$	-	-20	V	
$V_{GS}$	gate-source voltage		-12	12	V	
$I_D$	drain current	$V_{GS} = -4.5\text{ V}; T_{amb} = 25\text{ °C}; t \leq 5\text{ s}$	[1]	-	-3.7	A
		$V_{GS} = -4.5\text{ V}; T_{amb} = 25\text{ °C}$	[1]	-	-2.7	A
		$V_{GS} = -4.5\text{ V}; T_{amb} = 100\text{ °C}$	[1]	-	-1.7	A
$I_{DM}$	peak drain current	$T_{amb} = 25\text{ °C};$ single pulse; $t_p \leq 10\text{ }\mu\text{s}$	-	-11	A	
$P_{tot}$	total power dissipation	$T_{amb} = 25\text{ °C}$	[2]	-	485	mW
			[1]	-	1100	mW
		$T_{sp} = 25\text{ °C}$		-	6250	mW
<b>Source-drain diode</b>						
$I_S$	source current	$T_{amb} = 25\text{ °C}$	[1]	-	-1.1	A
<b>Per device</b>						
$T_j$	junction temperature		-55	150	°C	
$T_{amb}$	ambient temperature		-55	150	°C	
$T_{stg}$	storage temperature		-65	150	°C	

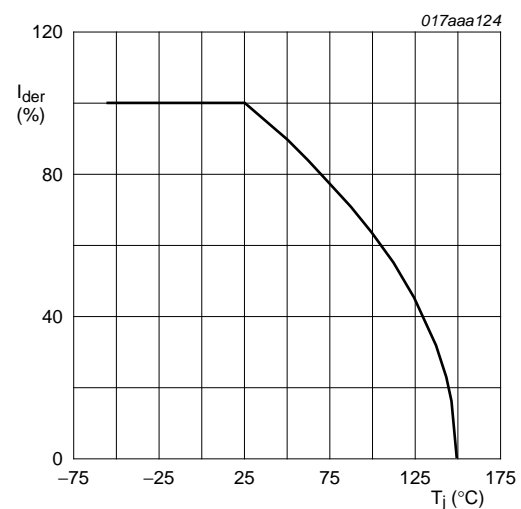
[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm<sup>2</sup>.

[2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.



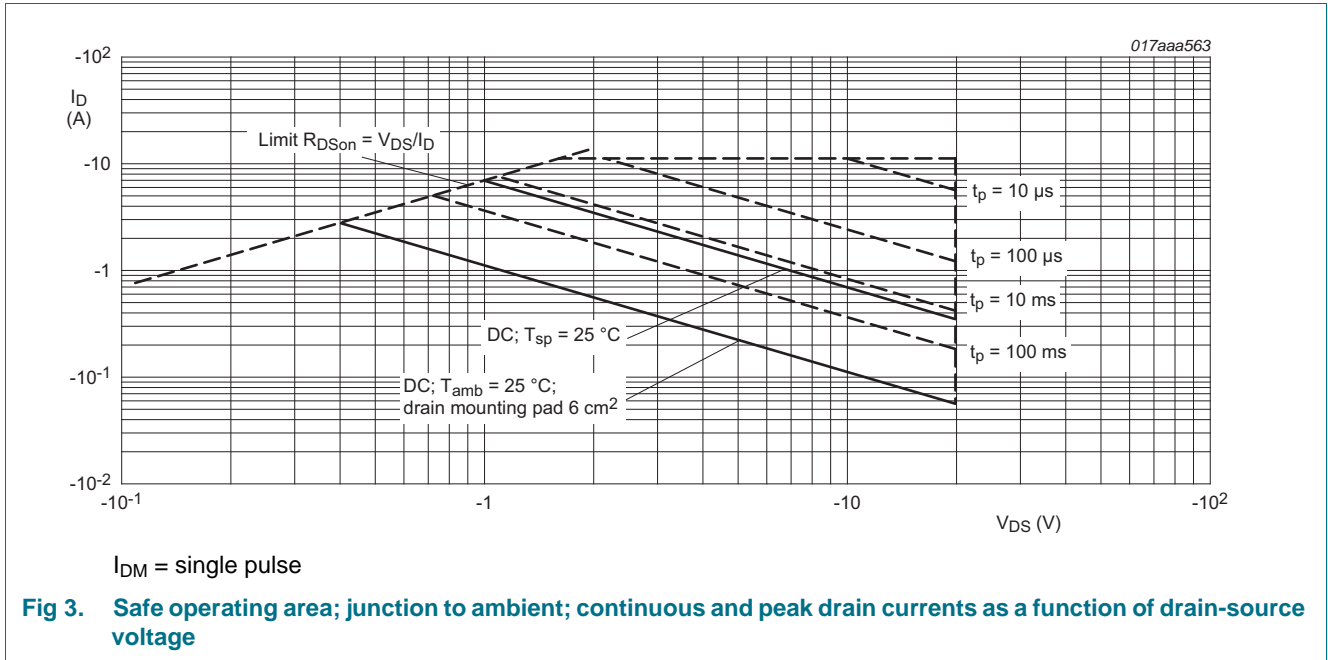
$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ\text{C})}} \times 100\%$$

**Fig 1. Normalized total power dissipation as a function of junction temperature**



$$I_{der} = \frac{I_D}{I_{D(25^\circ\text{C})}} \times 100\%$$

**Fig 2. Normalized continuous drain current as a function of junction temperature**



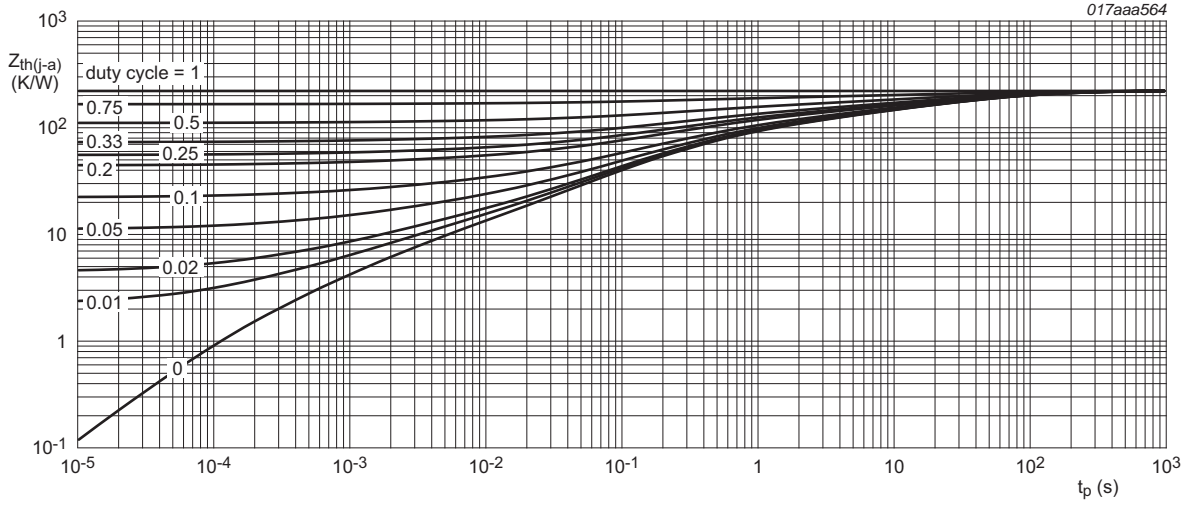
## 6. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
<b>Per transistor</b>							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	225	260	K/W
			[2]	-	99	115	K/W
		in free air; $t \leq 5$ s	[2]	-	54	62	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point	in free air	-	16	20	K/W	

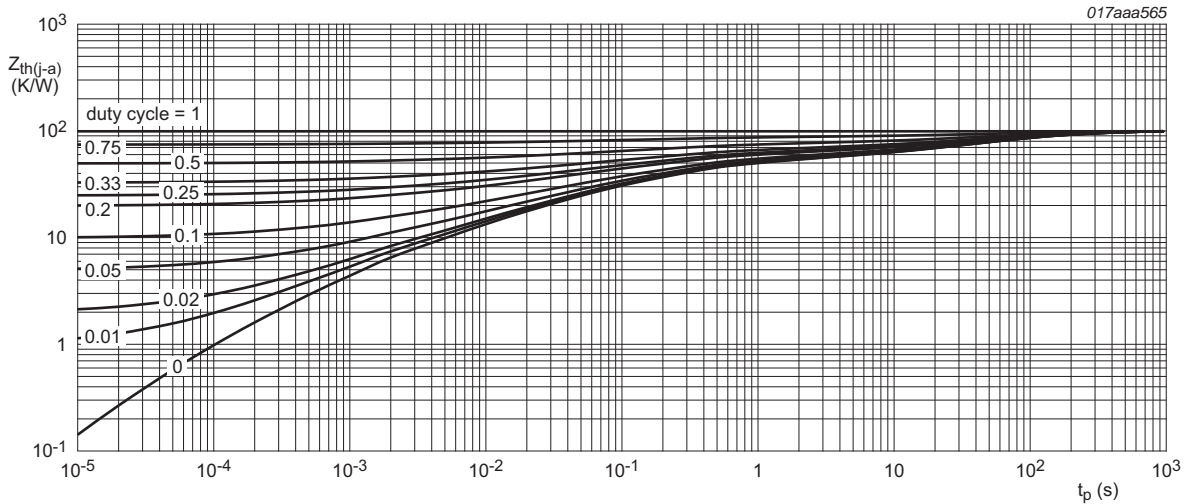
[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 6 cm<sup>2</sup>.



FR4 PCB, standard footprint

Fig 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



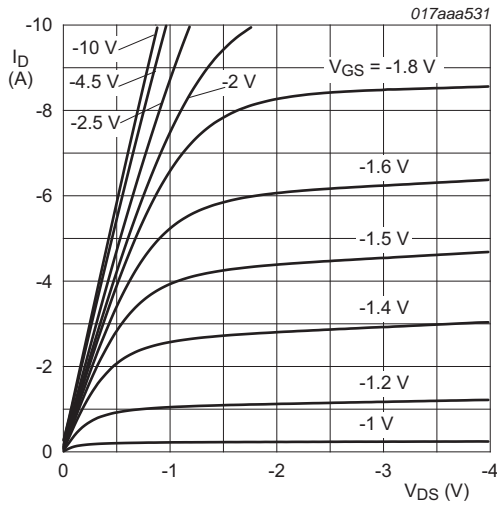
FR4 PCB, mounting pad for drain 6 cm<sup>2</sup>

Fig 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

## 7. Characteristics

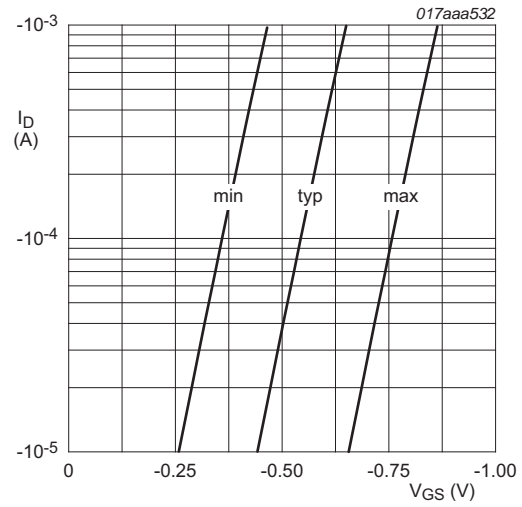
Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics (per transistor)</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = -250 \mu\text{A}$ ; $V_{GS} = 0 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-20	-	-	V
$V_{GSth}$	gate-source threshold voltage	$I_D = -250 \mu\text{A}$ ; $V_{DS} = V_{GS}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-0.4	-0.6	-1	V
$I_{DSS}$	drain leakage current	$V_{DS} = -20 \text{ V}$ ; $V_{GS} = 0 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	-	-1	$\mu\text{A}$
		$V_{DS} = -20 \text{ V}$ ; $V_{GS} = 0 \text{ V}$ ; $T_j = 150 \text{ }^\circ\text{C}$	-	-	-10	$\mu\text{A}$
$I_{GSS}$	gate leakage current	$V_{GS} = 12 \text{ V}$ ; $V_{DS} = 0 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	-	100	nA
		$V_{GS} = -12 \text{ V}$ ; $V_{DS} = 0 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	-	100	nA
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = -4.5 \text{ V}$ ; $I_D = -2.7 \text{ A}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	80	102	m $\Omega$
		$V_{GS} = -4.5 \text{ V}$ ; $I_D = -2.7 \text{ A}$ ; $T_j = 150 \text{ }^\circ\text{C}$	-	116	148	m $\Omega$
		$V_{GS} = -2.5 \text{ V}$ ; $I_D = -2.5 \text{ A}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	95	125	m $\Omega$
		$V_{GS} = -1.8 \text{ V}$ ; $I_D = -1.1 \text{ A}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	120	156	m $\Omega$
$g_{fs}$	forward transconductance	$V_{DS} = -10 \text{ V}$ ; $I_D = -2.7 \text{ A}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	15	-	S
<b>Dynamic characteristics (per transistor)</b>						
$Q_{G(tot)}$	total gate charge	$V_{DS} = -10 \text{ V}$ ; $I_D = -2.7 \text{ A}$ ; $V_{GS} = -4.5 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	5.7	8.6	nC
$Q_{GS}$	gate-source charge		-	0.7	-	nC
$Q_{GD}$	gate-drain charge		-	0.96	-	nC
$C_{iss}$	input capacitance	$V_{DS} = -10 \text{ V}$ ; $f = 1 \text{ MHz}$ ; $V_{GS} = 0 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	550	-	pF
$C_{oss}$	output capacitance		-	63	-	pF
$C_{rss}$	reverse transfer capacitance		-	53	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = -10 \text{ V}$ ; $I_D = -2.7 \text{ A}$ ; $V_{GS} = -4.5 \text{ V}$ ; $R_{G(ext)} = 6 \Omega$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	6	-	ns
$t_r$	rise time		-	14	-	ns
$t_{d(off)}$	turn-off delay time		-	120	-	ns
$t_f$	fall time		-	50	-	ns
<b>Source-drain diode (per transistor)</b>						
$V_{SD}$	source-drain voltage	$I_S = -1.1 \text{ A}$ ; $V_{GS} = 0 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	-0.8	-1.2	V



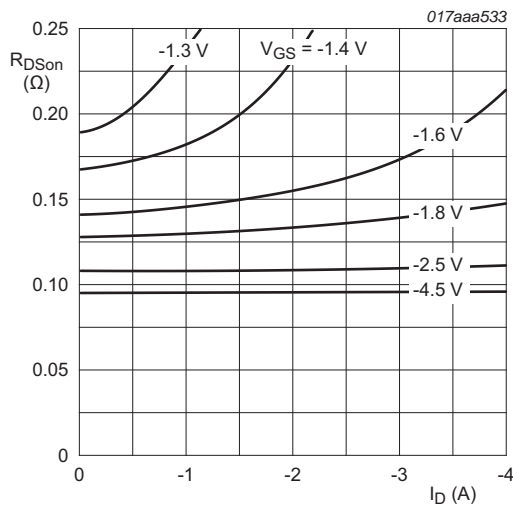
$T_j = 25\text{ }^\circ\text{C}$

**Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values**



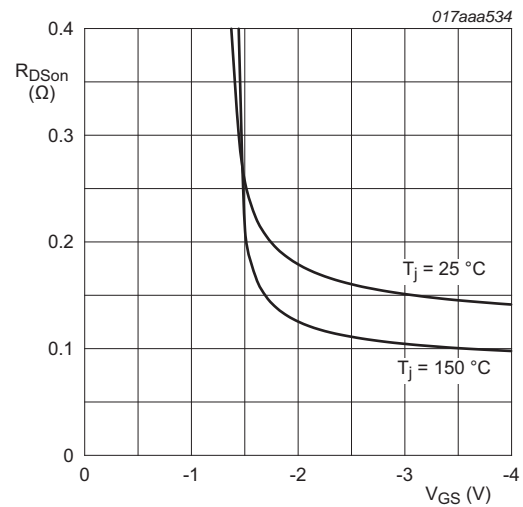
$T_j = 25\text{ }^\circ\text{C}; V_{DS} = -5\text{ V}$

**Fig. 7. Sub-threshold drain current as a function of gate-source voltage**



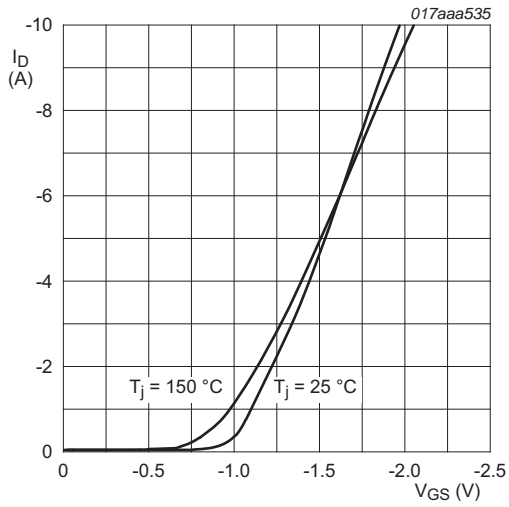
$T_j = 25\text{ }^\circ\text{C}$

**Fig. 8. Drain-source on-state resistance as a function of drain current; typical values**



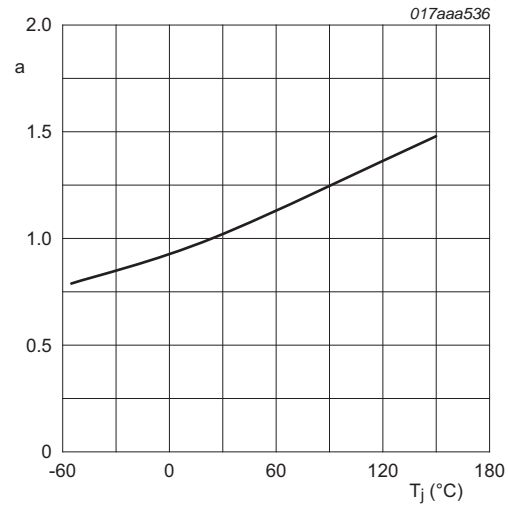
$I_D = -3\text{ A}$

**Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values**



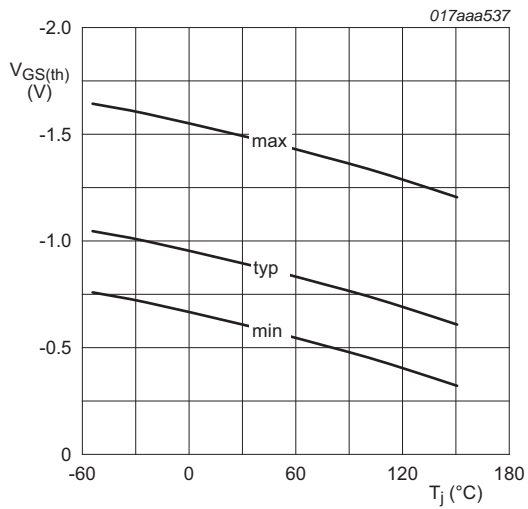
$$V_{DS} > I_D \times R_{DSon}$$

**Fig 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values**



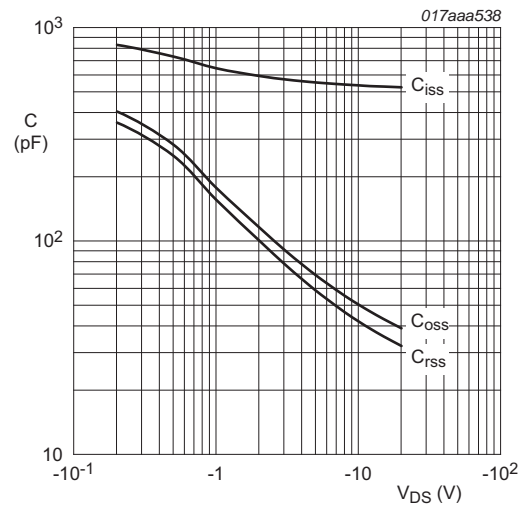
$$a = \frac{R_{DSon}}{R_{DSon(25^\circ C)}}$$

**Fig 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values**



$$I_D = -0.25 \text{ mA}; V_{DS} = V_{GS}$$

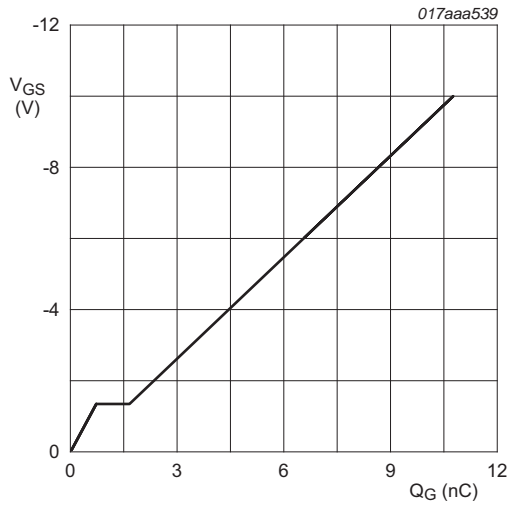
**Fig 12. Gate-source threshold voltage as a function of junction temperature**



$$f = 1 \text{ MHz}; V_{GS} = 0 \text{ V}$$

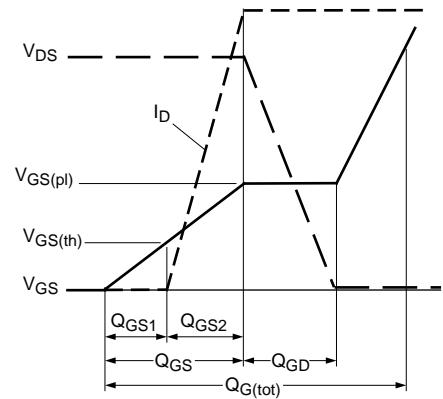
**Fig 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**



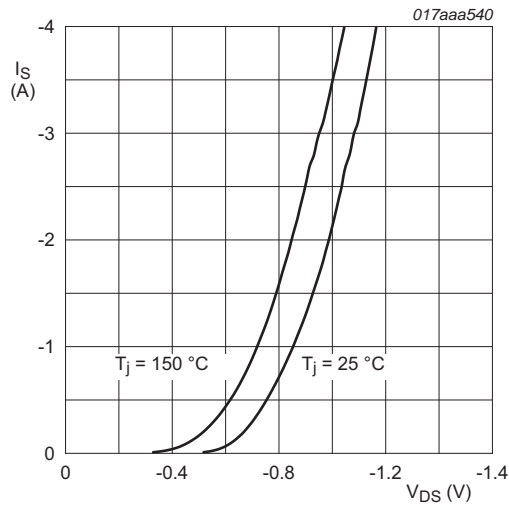


$I_D = -3\text{ A}$ ;  $V_{DS} = -10\text{ V}$ ;  $T_{amb} = 25\text{ }^\circ\text{C}$

**Fig 14. Gate-source voltage as a function of gate charge; typical values**



**Fig 15. Gate charge waveform definitions**



$V_{GS} = 0\text{ V}$

**Fig 16. Source current as a function of source-drain voltage; typical values**

## 8. Test information

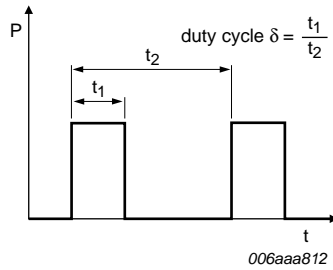


Fig 17. Duty cycle definition

## 9. Package outline

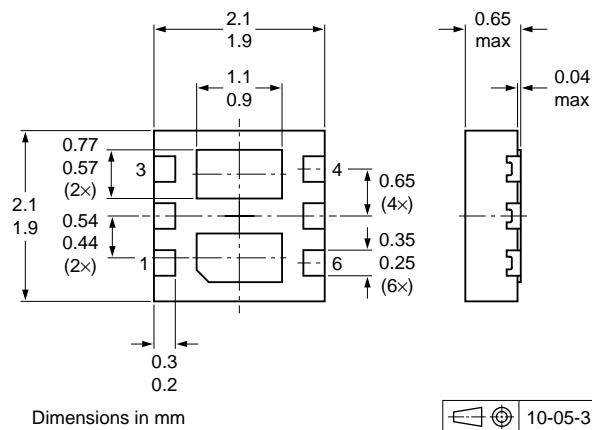
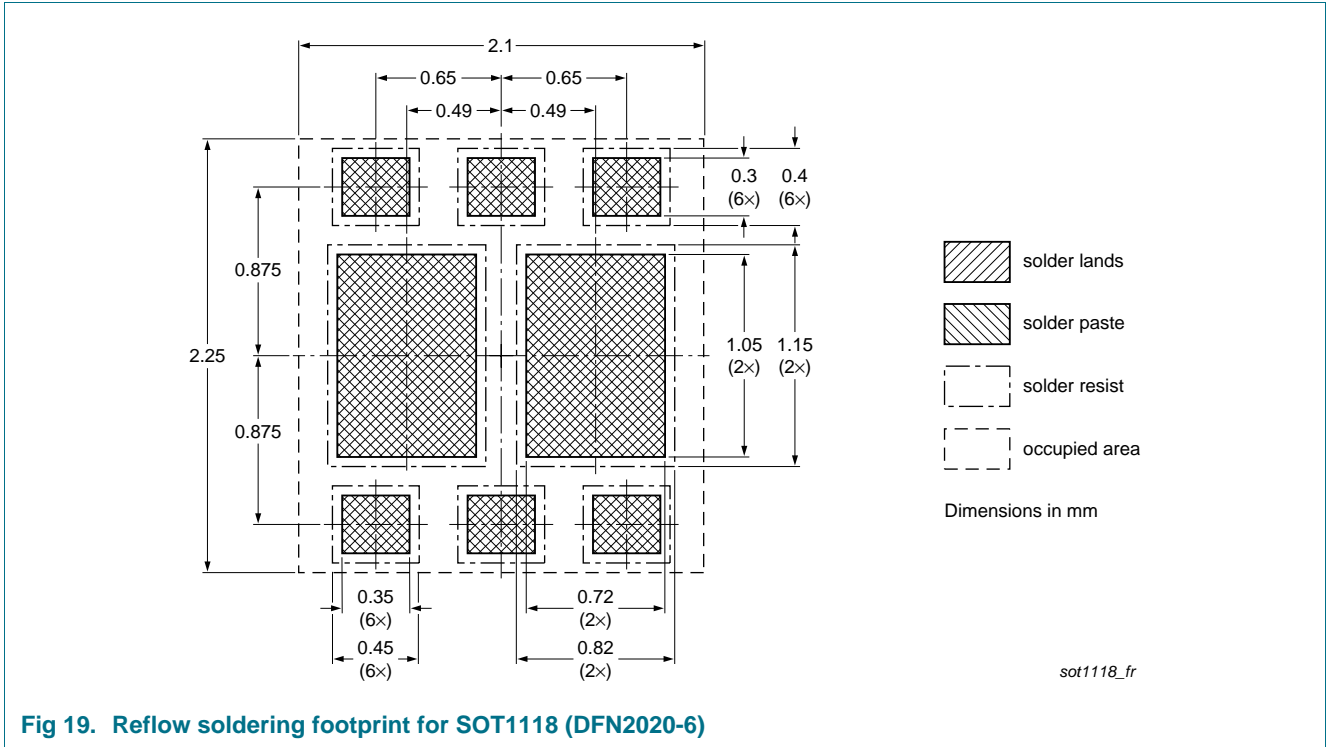


Fig 18. Package outline SOT1118 (DFN2020-6)

**10. Soldering**



**Fig 19. Reflow soldering footprint for SOT1118 (DFN2020-6)**

## 11. Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PMDPB80XP v.1	20120530	Product data sheet	-	-

## 12. Legal information

### 12.1 Data sheet status

Document status <sup>[1]</sup> [2]	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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## 14. Contents

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<b>1</b>	<b>Product profile</b> . . . . .	<b>1</b>
1.1	General description . . . . .	1
1.2	Features and benefits . . . . .	1
1.3	Applications . . . . .	1
1.4	Quick reference data . . . . .	1
<b>2</b>	<b>Pinning information</b> . . . . .	<b>2</b>
<b>3</b>	<b>Ordering information</b> . . . . .	<b>2</b>
<b>4</b>	<b>Marking</b> . . . . .	<b>2</b>
<b>5</b>	<b>Limiting values</b> . . . . .	<b>3</b>
<b>6</b>	<b>Thermal characteristics</b> . . . . .	<b>4</b>
<b>7</b>	<b>Characteristics</b> . . . . .	<b>6</b>
<b>8</b>	<b>Test information</b> . . . . .	<b>10</b>
<b>9</b>	<b>Package outline</b> . . . . .	<b>10</b>
<b>10</b>	<b>Soldering</b> . . . . .	<b>11</b>
<b>11</b>	<b>Revision history</b> . . . . .	<b>12</b>
<b>12</b>	<b>Legal information</b> . . . . .	<b>13</b>
12.1	Data sheet status . . . . .	13
12.2	Definitions . . . . .	13
12.3	Disclaimers . . . . .	13
12.4	Trademarks . . . . .	14
<b>13</b>	<b>Contact information</b> . . . . .	<b>14</b>