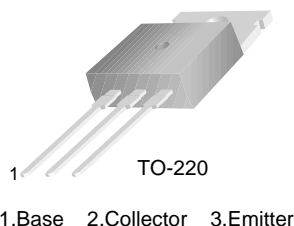


BDW94/C

PNP Epitaxial Silicon Transistor

Power Linear and Switching Application

- Power Darlington TR
- Complement to BDW93 and BDW93C Respectively



Absolute Maximum Ratings T_a = 25°C unless otherwise noted

Symbol	Parameter	Value	Units
V _{CBO}	Collector-Base Voltage		
	: BDW94	-45	V
	: BDW94C	-100	V
V _{CEO}	Collector-Emitter Voltage		
	: BDW94	-45	V
	: BDW94C	-100	V
I _C	Collector Current (DC)	-12	A
I _{CP}	Collector Current (Pulse) *	-15	A
I _B	Base Current	-0.2	A
P _C	Collector Dissipation (T _C = 25°C)	80	W
T _J	Junction Temperature	150	°C
T _{STG}	Storage Temperature	-65 ~ 150	°C

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Conditions	Min.	Typ.	Max	Units
$V_{CE(sus)}$	Collector-Emitter Sustaining Voltage : BDW94 : BDW94C	$I_C = -100\text{mA}, I_B = 0$	-45 -100			V V
I_{CBO}	Collector Cut-off Current : BDW94 : BDW94C	$V_{CB} = -45\text{V}, I_E = 0$ $V_{CB} = -100\text{V}, I_E = 0$			-100 -100	μA μA
I_{CEO}	Collector Cut-off Current : BDW94 : BDW94C	$V_{EB} = -45\text{V}, I_B = 0$ $V_{CE} = -100\text{V}, I_B = 0$			-1 -1	mA mA
I_{EBO}	Emitter Cut-off Current	$V_{EB} = -5\text{V}, I_C = 0$			-2	mA
h_{FE}	DC Current Gain *	$V_{CE} = -3\text{V}, I_C = -3\text{A}$ $V_{CE} = -3\text{V}, I_C = -5\text{A}$ $V_{CE} = -3\text{V}, I_C = -10\text{A}$	1000 750 100		20000	
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage *	$I_C = -5\text{A}, I_B = -20\text{mA}$ $I_C = -10\text{A}, I_B = -100\text{mA}$			-2 -3	V V
$V_{BE(sat)}$	Base-Emitter Saturation Voltage *	$I_C = -5\text{A}, I_B = -20\text{mA}$ $I_C = -10\text{A}, I_B = -100\text{mA}$			-2.5 -4	V V
V_F	Parallel Diode Forward Voltage *	$I_F = -5\text{A}$ $I_F = -10\text{A}$		-1.3 -1.8	-2 -4	V V

* Pulse Test: PW = 300 μs , Duty Cycle = 1.5% Pulsed

Typical Performance Characteristics

Figure 1. DC Current Gain

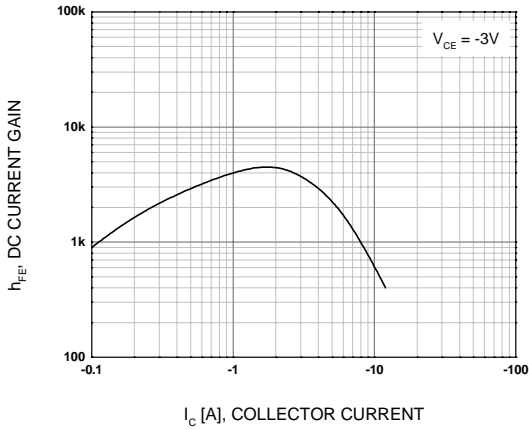


Figure 2. Collector-Emitter Saturation Voltage

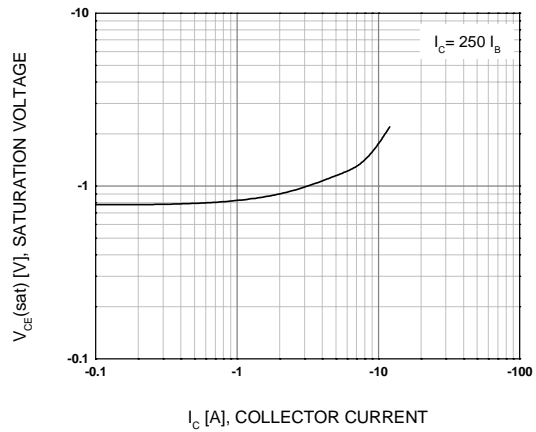


Figure 3. Base-Emitter On Voltage

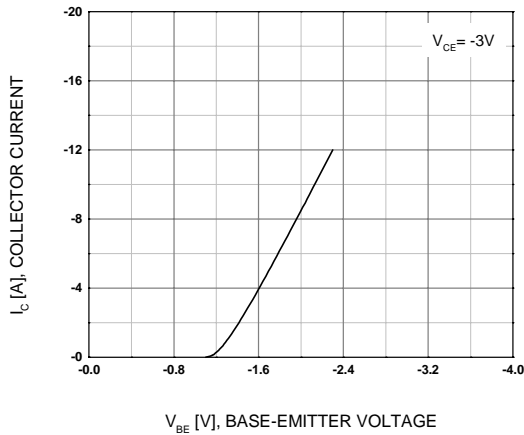


Figure 4. Output Capacitance

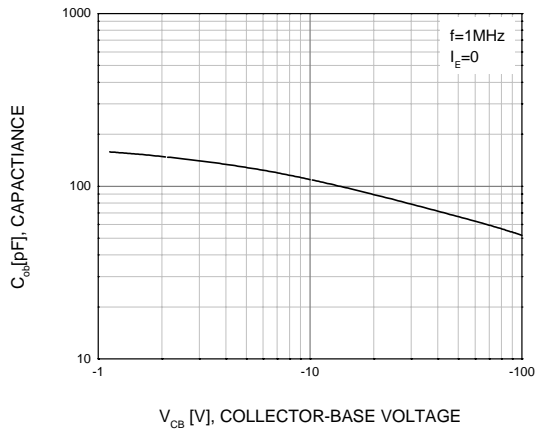


Figure 5. Safe Operating Area

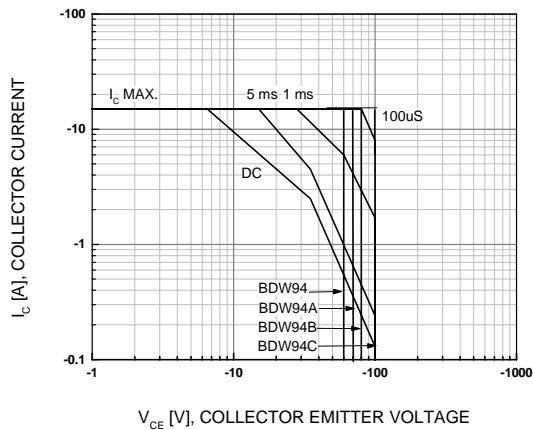
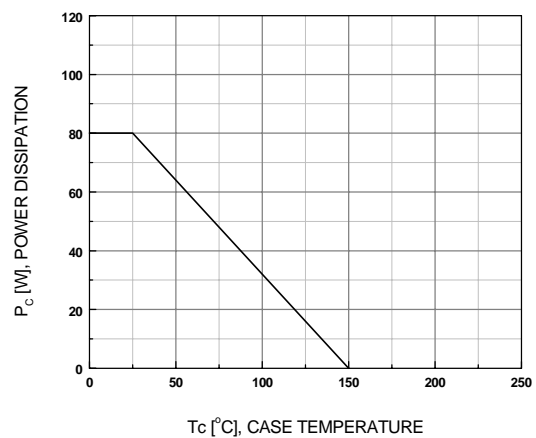


Figure 6. Power Derating



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