



## TE0820 TRM

Revision v.91

Exported on 2020-06-08

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<https://wiki.trenz-electronic.de/display/PD/TE0820+TRM>

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## 4 Overview

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The Trenz Electronic TE0820 is an industrial-grade 4 x 5 cm MPSoC SoM (System on Module) module integrating a Xilinx Zynq UltraScale+ with up to 4 GByte 32-Bit DDR4 SDRAM, max. 128 MByte SPI Boot Flash memory for configuration and operation and powerful switch-mode power supplies for all on-board voltages. A large number of configurable I/Os is provided via rugged high-speed stacking strips. All Trenz Electronic SoMs in 4 x 5 cm form factor are mechanically compatible.

Refer to <http://trenz.org/te0820-info> for the current online version of this manual and other available documentation.

### 4.1 Key Features

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- Xilinx Zynq UltraScale+ MPSoC (XCZU2CG / XCZU2EG, XCZU3CG / XCZU3EG or XCZU4CG / XCZU4EV)
  - Quad-core or dual-core Cortex-A53 64-bit ARM v8 application processing unit (APU) (depends on assembly variant CG,EG,EV)
  - Dual Cortex-R5 32-bit ARM v7 real-time processing unit (RPU)
  - Four high-speed serial I/O (HSSIO) interfaces supporting following protocols:
    - PCI Express® interface version 2.1 compliant
    - SATA 3.1 specification compliant interface
    - DisplayPort source-only interface with video resolution up to 4k x 2k
    - USB 3.0 specification compliant interface implementing a 5 Gbit/s line rate
    - 1 GB/s serial GMII interface
  - 132 x HP PL I/Os (3 banks)
  - 14 x PS MIOs (6 of the MIOs intended for SD card interface in default configuration)
  - 4 x serial PS GTR transceivers
- 2 GByte DDR4 SDRAM, 32bit databus-width
- 128 MByte QSPI boot Flash in dual parallel mode
- 8 GByte eMMC
- Programmable quad PLL clock generator PLL for PS GTR clocks (optional external reference)
- Gigabit Ethernet transceiver PHY (Marvell Alaska 88E1512)
- MAC address serial EEPROM with EUJ-48™ node identity (Microchip 24AA025E48)
- Hi-speed USB2 ULPI transceiver with full OTG support (Microchip USB3320C)
- Plug-on module with 2 x 100-pin and 1 x 60-pin high-speed hermaphroditic strips
- All power supplies on board
- Size: 50 x 40 mm

Additional assembly options are available for cost or performance optimization upon request.

### 4.2 Block Diagram

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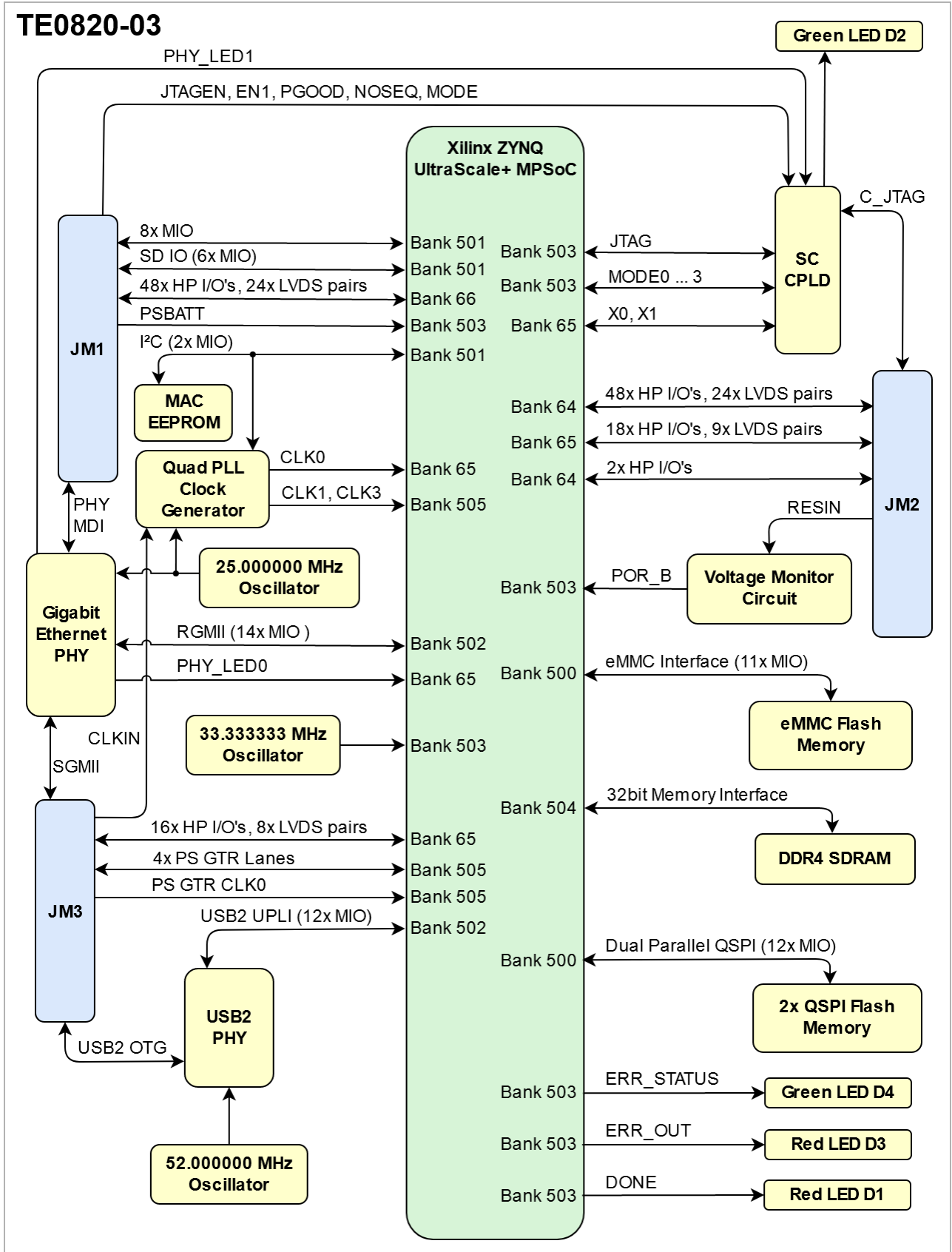
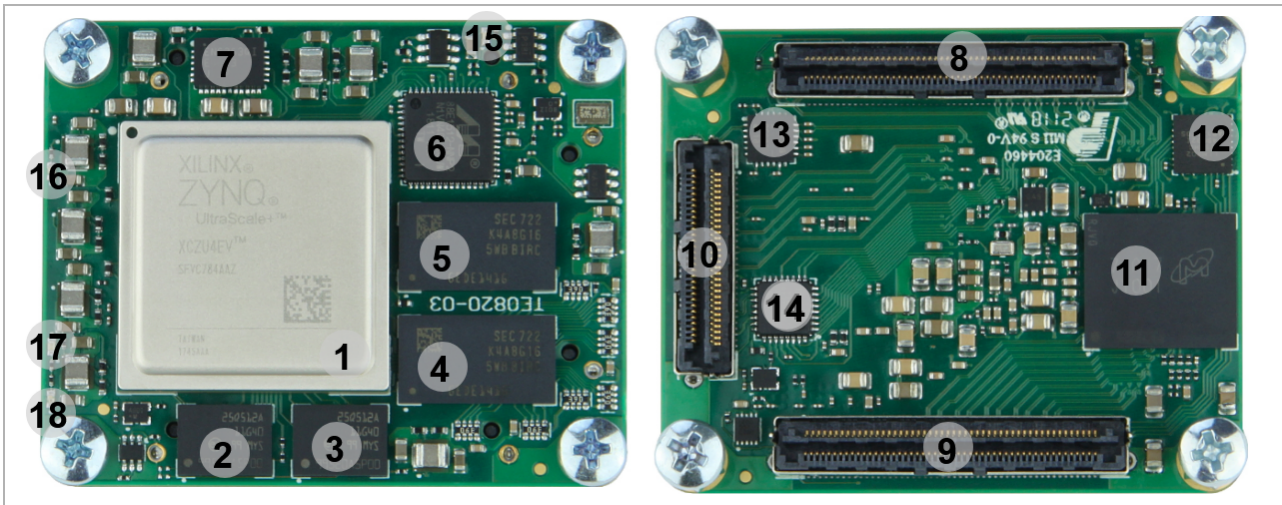


Figure 1: Figure 1: TE0820-03 block diagram

### 4.3 Main Components



**Figure 2: Figure 2: TE0820-03 main components**

1. Xilinx Zynq UltraScale+ MPSoC, U1
2. 1.8V, 512 Mbit QSPI flash memory, U7
3. 1.8V, 512 Mbit QSPI flash memory, U17
4. 8 Gbit (512 x 16) DDR4 SDRAM, U2
5. 8 Gbit (512 x 16) DDR4 SDRAM, U3
6. Marvell Alaska 88E1512 integrated 10/100/1000 Mbps energy efficient ethernet transceiver, U8
7. 6A PowerSoC DC-DC converter (PL\_VCCINT, 0.85V), U5
8. B2B connector Samtec Razor Beam™ LSHM-150, JM1
9. B2B connector Samtec Razor Beam™ LSHM-150, JM2
10. B2B connector Samtec Razor Beam™ LSHM-130, JM3
11. 8 GByte eMMC memory, U6
12. Lattice Semiconductor MachXO2 System Controller CPLD, U21
13. I2C programmable, any frequency , any output quad clock generator, U10
14. Highly integrated full featured hi-speed USB 2.0 ULPI transceiver, U18
15. LED D1(Red) Done Pin
16. LED D2 (Green) CPLD Status, User LED
17. LED D3 (Red) PS Error
18. LED D4 (Green) PS Error Status

### 4.4 Initial Delivery State

Storage Device Name	Content	Notes
SPI Flash OTP Area	Empty, not programmed	Except serial number programmed by flash vendor.
SPI Flash Quad Enable bit	Programmed	-



Storage Device Name	Content	Notes
SPI Flash main array	Not programmed	-
eFUSE USER	Not programmed	-
eFUSE Security	Not programmed	-
Si5338 OTP NVM	Not programmed	-
CPLD (LCMXO2-256HC)	SC0820-02 QSPI Firmware	See <a href="#">Boot Process</a> (see page 10) section.

**Table 1:** Initial delivery state of programmable devices on the module

## 5 Boot Process

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Two different firmware versions are available, one with the QSPI boot option and other with the SD Card boot option.

<b>B2B JM1 MODE Pin</b>	<b>Default CPLD Firmware</b>	<b>QSPI Firmware Version</b>	<b>SD Card Firmware Version</b>
Low	SD	JTAG	Boot from SD Card
High	Flash	Boot from Flash	JTAG

**Table 2:** Boot mode pin description

For more information refer to the [TE0820 CPLD - BootMode<sup>1</sup>](#) section.

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<sup>1</sup> [https://wiki.trenz-electronic.de/display/PD/TE0820-REV01\\_REV02+CPLD#TE0820-REV01\\_REV02CPLD-BootMode](https://wiki.trenz-electronic.de/display/PD/TE0820-REV01_REV02+CPLD#TE0820-REV01_REV02CPLD-BootMode)

## 6 Signals, Interfaces and Pins

### 6.1 Board to Board (B2B) I/Os

Zynq MPSoC's I/O banks signals connected to the B2B connectors:

Bank	Type	B2B Connector	I/O Signal Count	Voltage	Notes
64	HP	JM2	48	User	Max voltage 1.8V
64	HP	JM2	2	User	Max voltage 1.8V
65	HP	JM2	18	User	Max voltage 1.8V
65	HP	JM3	16	User	Max voltage 1.8V
66	HP	JM1	48	User	Max voltage 1.8V
500	MIO	JM1	8	1.8V	-
501	MIO	JM1	6	3.3V	-
505	GTR	JM3	4 lanes	-	-
505	GTR CLK	JM3	1 differential input	-	-

**Table 3:** General overview of board to board I/O signals

For detailed information about the pin-out, please refer to the [Pin-out table](#)<sup>2</sup>.

### 6.2 MGT Lanes

The Xilinx Zynq UltraScale+ device used on the TE0820 module has 4 GTR transceivers. All 4 are wired directly to B2B connector JM3. MGT (Multi Gigabit Transceiver) lane consists of one transmit and one receive (TX/RX) differential pairs, four signals total per one MGT lane. Following table lists lane number, FPGA bank number, transceiver type, signal schematic name, board-to-board pin connection and FPGA pins connection:

<sup>2</sup> [https://shop.trenz-electronic.de/Download/?path=Trenz\\_Electronic/Pinout](https://shop.trenz-electronic.de/Download/?path=Trenz_Electronic/Pinout)

Lane	Bank	Type	Signal Name	B2B Pin	FPGA Pin
0	505	GTR	<ul style="list-style-type: none"> <li>B505_RX0_P</li> <li>B505_RX0_N</li> <li>B505_TX0_P</li> <li>B505_TX0_N</li> </ul>	<ul style="list-style-type: none"> <li>JM3-26</li> <li>JM3-28</li> <li>JM3-25</li> <li>JM3-27</li> </ul>	<ul style="list-style-type: none"> <li>PS_MGTRRX0_505, F27</li> <li>PS_MGTRRXN0_505, F28</li> <li>PS_MGTRTX0_505, E25</li> <li>PS_MGTRTXN0_505, E26</li> </ul>
1	505	GTR	<ul style="list-style-type: none"> <li>B505_RX1_P</li> <li>B505_RX1_N</li> <li>B505_TX1_P</li> <li>B505_TX1_N</li> </ul>	<ul style="list-style-type: none"> <li>JM3-20</li> <li>JM3-22</li> <li>JM3-19</li> <li>JM3-21</li> </ul>	<ul style="list-style-type: none"> <li>PS_MGTRRX1_505, D27</li> <li>PS_MGTRRXN1_505, D28</li> <li>PS_MGTRTX1_505, D23</li> <li>PS_MGTRTXN1_505, D24</li> </ul>
2	505	GTR	<ul style="list-style-type: none"> <li>B505_RX2_P</li> <li>B505_RX2_N</li> <li>B505_TX2_P</li> <li>B505_TX2_N</li> </ul>	<ul style="list-style-type: none"> <li>JM3-14</li> <li>JM3-16</li> <li>JM3-13</li> <li>JM3-15</li> </ul>	<ul style="list-style-type: none"> <li>PS_MGTRRX0_505, B27</li> <li>PS_MGTRRXN0_505, B28</li> <li>PS_MGTRTX0_505, C25</li> <li>PS_MGTRTXN0_505, C26</li> </ul>
3	505	GTR	<ul style="list-style-type: none"> <li>B505_RX3_P</li> <li>B505_RX3_N</li> <li>B505_TX3_P</li> <li>B505_TX3_N</li> </ul>	<ul style="list-style-type: none"> <li>JM3-8</li> <li>JM3-10</li> <li>JM3-7</li> <li>JM3-9</li> </ul>	<ul style="list-style-type: none"> <li>PS_MGTRRX1_505, A25</li> <li>PS_MGTRRXN1_505, A26</li> <li>PS_MGTRTX1_505, B23</li> <li>PS_MGTRTXN1_505, B24</li> </ul>

**Table 4:** MGT lanes

There are 3 clock sources for the GTR transceivers. B505\_CLK0 is connected directly to B2B connector JM3, so the clock can be provided by the carrier board. Clocks B505\_CLK1 and B505\_CLK3 are provided by the on-board clock generator (U10). As there are no capacitive coupling of the data and clock lines that are connected to the connectors, these may be required on the user's PCB depending on the application.

Clock signal	Bank	Source	FPGA Pin	Notes
B505_CLK0_P	505	B2B, JM3-31	PS_MGTREFCLK0P_505, F23	Supplied by the carrier board

Clock signal	Bank	Source	FPGA Pin	Notes
B505_CLK0_N	505	B2B, JM3-33	PS_MGTREFCLK0N_505, F24	Supplied by the carrier board
B505_CLK1_P	505	U10, CLK2A	PS_MGTREFCLK1P_505, E21	On-board Si5338A
B505_CLK1_N	505	U10, CLK2B	PS_MGTREFCLK1N_505, E22	On-board Si5338A
B505_CLK2_P	505	N/A	PS_MGTREFCLK2P_505, C21	Not connected
B505_CLK2_N	505	N/A	PS_MGTREFCLK2N_505, C22	Not connected
B505_CLK3_P	505	U10, CLK1A	PS_MGTREFCLK3P_505, A21	On-board Si5338A
B505_CLK3_N	505	U10, CLK1B	PS_MGTREFCLK3N_505, A22	On-board Si5338A

**Table 5:** MGT reference clock sources

## 6.3 JTAG Interface

JTAG access to the Xilinx Zynq-7000 is provided through B2B connector JM2.

JTAG Signal	B2B Connector Pin
TMS	JM2-93
TDI	JM2-95
TDO	JM2-97
TCK	JM2-99

**Table 6:** JTAG interface signals

Pin 89 JTAGEN of B2B connector JM1 is used to control which device is accessible via JTAG. If set to low or grounded, JTAG interface will be routed to the Xilinx Zynq MPSoC. If pulled high, JTAG interface will be routed to the System Controller CPLD.

## 6.4 System Controller CPLD I/O Pins

Special purpose pins are connected to System Controller CPLD and have following default configuration:

Pin Name	Mode	Function	Default Configuration
EN1	Input	Power Enable	No hard wired function on PCB. When forced low, PGOOD goes low without effect on power management
PGOOD	Output	Power Good	Only indirect used for power status, see CPLD description
NOSEQ	-	-	No used for Power sequencing, see CPLD description
RESIN	Input	Reset	Active low reset, gated to POR_B
JTAGEN	Input	JTAG Select	Low for normal operation, high for CPLD JTAG access

**Table 7:** System Controller CPLD special purpose pins.

See also

- [4 x 5 SoM Integration Guide](#)<sup>3</sup>
- [TE0820 CPLD](#)<sup>4</sup>
- [TE0820-REV01\\_REV02 CPLD](#)<sup>5</sup>

## 6.5 Default PS MIO Mapping

PS MIO	Function	B2B Pin	Connected to	PS MIO	Function	B2B Pin	Connected to
<b>0</b>	SPI0	-	U7-B2, CLK	<b>40..45</b>	-	-	Not connected
<b>1</b>	SPI0	-	U7-D2, DO/IO1	<b>46</b>	SD	JM1-17	B2B, SD_DAT3
<b>2</b>	SPI0	-	U7-C4, WP/IO2	<b>47</b>	SD	JM1-19	B2B, SD_DAT2

<sup>3</sup> <https://wiki.trenz-electronic.de/display/PD/4+x+5+SoM+Integration+Guide#id-4x5SoMIntegrationGuide-4x5SoMIntegrationGuide-4x5ModuleControllerIOs>

<sup>4</sup> <https://wiki.trenz-electronic.de/display/PD/TE0820+CPLD>

<sup>5</sup> [https://wiki.trenz-electronic.de/display/PD/TE0820-REV01\\_REV02+CPLD](https://wiki.trenz-electronic.de/display/PD/TE0820-REV01_REV02+CPLD)

<b>3</b>	SPI0	-	U7-D4, HOLD/ IO3	<b>48</b>	SD	JM1-21	B2B, SD_DAT1
<b>4</b>	SPI0	-	U7-D3, DI/IO0	<b>49</b>	SD	JM1-23	B2B, SD_DAT0
<b>5</b>	SPI0	-	U7-C2, CS	<b>50</b>	SD	JM1-25	B2B, SD_CMD
<b>6</b>	N/A	-	Not connected	<b>51</b>	SD	JM1-27	B2B, SD_CLK
<b>7</b>	SPI1	-	U17-C2, CS	<b>52</b>	USB_PH Y	-	U18-31, OTG- DIR
<b>8</b>	SPI1	-	U17-D3, DI/IO0	<b>53</b>	USB_PH Y	-	U18-31, OTG- DIR
<b>9</b>	SPI1	-	U17-D2, DO/ IO1	<b>54</b>	USB_PH Y	-	U18-5, OTG- DATA2
<b>10</b>	SPI1	-	U17-C4, WP/ IO2	<b>55</b>	USB_PH Y	-	U18-2, OTG- NXT
<b>11</b>	SPI1	-	U17-D4, HOLD/ IO3	<b>56</b>	USB_PH Y	-	U18-3, OTG- DATA0
<b>12</b>	SPI1	-	U17-B2, CLK	<b>57</b>	USB_PH Y	-	U18-4, OTG- DATA1
<b>13..20</b>	eMMC	-	U6, MMC- D0..D7	<b>58</b>	USB_PH Y	-	U18-29, OTG- STP
<b>21</b>	eMMC	-	U6, MMC-CMD	<b>59</b>	USB_PH Y	-	U18-6, OTG- DATA3
<b>22</b>	eMMC	-	U6, MMC-CLKR	<b>60</b>	USB_PH Y	-	U18-7, OTG- DATA4
<b>23</b>	eMMC	-	U6, MMC-RST	<b>61</b>	USB_PH Y	-	U18-9, OTG- DATA5
<b>24</b>	ETH	-	U8, ETH-RST	<b>62</b>	USB_PH Y	-	U18-10, OTG- DATA6
<b>25</b>	USB_PH Y	-	U18, OTG-RST	<b>63</b>	USB_PH Y	-	U18-13, OTG- DATA7
<b>26</b>	MIO	JM1-95	B2B, as PJTAG MIO possible	<b>64</b>	ETH	-	U8-53, ETH- TXCK

<b>27</b>	MIO	JM1-93	B2B, as PJTAG MIO possible	<b>65..66</b>	ETH	-	U8-50..51, ETH-TXD0..1
<b>28</b>	MIO	JM1-99	B2B, as PJTAG MIO possible	<b>67..68</b>	ETH	-	U8-54..55, ETH-TXD2..3
<b>29</b>	MIO	JM1-97	B2B, as PJTAG MIO possible	<b>69</b>	ETH	-	U8-56, ETH- TXCTL
<b>30</b>	MIO	JM1-92	B2B (UART RX)	<b>70</b>	ETH	-	U8-46, ETH- RXCK
<b>31</b>	MIO	JM1-85	B2B (UART TX)	<b>71..72</b>	ETH	-	U8-44..45, ETH-RXD0..1
<b>32</b>	MIO	JM1-91	B2B	<b>73..74</b>	ETH	-	U8-47..48, ETH-RXD2..3
<b>33</b>	MIO	JM1-87	B2B	<b>75</b>	ETH	-	U8-43, ETH- RXCTL
<b>34..37</b>	-	-	Not connected	<b>76</b>	ETH	-	U8-7, ETH- MDC
<b>38</b>	I <sup>2</sup> C	-	U10-12, SCL	<b>77</b>	ETH	-	U8-8, ETH- MDIO
<b>39</b>	I <sup>2</sup> C	-	U10-19, SDA	-	-	-	-

**Table 8:** TE0820-03 PS MIO mapping

## 6.6 Gigabit Ethernet

On-board Gigabit Ethernet PHY is provided with Marvell Alaska 88E1512 chip. The Ethernet PHY RGMII interface is connected to the Zynq Ethernet0 PS GEM0. I/O voltage is fixed at 1.8V for HSTL signaling. SGMII (SFP copper or fiber) can be used directly with the Ethernet PHY, as the SGMII pins are available on the B2B connector JM3. The reference clock input of the PHY is supplied from an on-board 25MHz oscillator (U11), the 125MHz output clock is left unconnected.

### Ethernet PHY connection

PHY Pin	ZYNQ PS	ZYNQ PL	Notes
MDC/MDIO	MIO76, MIO77	-	-
LED0	-	K8	Can be routed via PL to any free PL I/O pin in B2B connector.



PHY Pin	ZYNQ PS	ZYNQ PL	Notes
LED1	-	-	CPLD pin 17.
LED2	-	-	Not connected.
CONFIG	-	-	Wired to the 1.8V.
RESETn	MIO24	-	-
RGMII	MIO64..MIO75	-	-
SGMII	-	-	Routed to the B2B connector JM3.

**Table 9:** General overview of the Gigabit Ethernet PHY signals

## 6.7 USB Interface

USB PHY is provided by Microchip USB3320. The ULPI interface is connected to the Zynq PS USB0. I/O voltage is fixed at 1.8V. Reference clock input for the USB PHY is supplied by the on-board 52.000000 MHz oscillator (U14).

### USB PHY connection

PHY Pin	ZYNQ Pin	B2B Name	Notes
ULPI	MIO52..63	-	Zynq USB0 MIO pins are connected to the USB PHY.
REFCLK	-	-	52.000000 MHz from on-board oscillator (U14).
REFSEL[0..2]	-	-	Reference clock frequency select, all set to GND selects 52.000000 MHz.
RESETB	MIO25	-	Active low reset.
CLKOUT	MIO52	-	Connected to 1.8V, selects reference clock operation mode.
DP, DM	-	OTG_D_P, OTG_D_N	USB data lines routed to B2B connector JM3 pins 47 and 49.
CPEN	-	VBUS_V_EN	External USB power switch active high enable signal, routed to JM3 pin 17.

PHY Pin	ZYNQ Pin	B2B Name	Notes
VBUS	-	USB_VBUS	Connect to USB VBUS via a series of resistors, see reference schematics, routed to JM3 pin 55.
ID	-	OTG_ID	For an A-device connect to ground, for a B-device left floating. routed from JM3 pin 23.

**Table 10:** General overview of the USB PHY signals.

## 6.8 I<sup>2</sup>C Interface

On-board I<sup>2</sup>C devices are connected to MIO38 (SCL) and MIO39 (SDA) which are configured as I<sup>2</sup>C0 by default. Addresses for on-board I<sup>2</sup>C slave devices are listed in the table below:

I <sup>2</sup> C Device	I <sup>2</sup> C Address	Notes
Si5338A PLL	0x70	-
EEPROM	0x50	-

**Table 11:** Address table of the I<sup>2</sup>C bus slave devices.

## 7 On-board Peripherals

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### 7.1 System Controller CPLD

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The System Controller CPLD (U21) is provided by Lattice Semiconductor LCMXO2-256HC (MachXO2 product family). It is the central system management unit with module specific firmware installed to monitor and control various signals of the FPGA, on-board peripherals, I/O interfaces and module as a whole.

See also TE0820 System Controller [CPLD page](#)<sup>6</sup>.

### 7.2 eMMC Flash Memory

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eMMC Flash memory device(U6) is connected to the ZynqMP PS MIO bank 500 pins MIO13..MIO23. eMMC chips IS21ES08G-JCLI (FLASH - NAND Speicher-IC (64 Gb x 1) MMC ) is used.

### 7.3 DDR4 Memory

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By default TE0820-03 module has two 16-bit wide Samsung K4A8G165WB DDR4 SDRAM chips arranged into 32-bit wide memory bus providing total of 2 GBytes of on-board RAM. Different memory sizes are available optionally.

### 7.4 Quad SPI Flash Memory

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Two quad SPI compatible serial bus flash MT25QU512ABB8E12-0SIT memory chips are provided for FPGA configuration file storage. After configuration completes the remaining free memory can be used for application data storage. All four SPI data lines are connected to the FPGA allowing x1, x2 or x4 data bus widths to be used. The maximum data transfer rate depends on the bus width and clock frequency.

### 7.5 Gigabit Ethernet PHY

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On-board Gigabit Ethernet PHY (U8) is provided with Marvell Alaska 88E1512 IC (U8). The Ethernet PHY RGMII interface is connected to the ZynqMP Ethernet3 PS GEM3. I/O voltage is fixed at 1.8V for HSTL signaling. The reference clock input of the PHY is supplied from an on-board 25.000000 MHz oscillator (U11).

### 7.6 High-speed USB ULPI PHY

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Hi-speed USB ULPI PHY (U18) is provided with USB3320 from Microchip. The ULPI interface is connected to the Zynq PS USB0 via MIO52..63, bank 502. The I/O voltage is fixed at 1.8V and PHY reference clock input is supplied from the on-board 52.000000 MHz oscillator (U14).

### 7.7 MAC Address EEPROM

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A Microchip 24AA025E48 serial EEPROM (U25) contains a globally unique 48-bit node address, which is compatible with EUI-48(TM) specification. The device is organized as two blocks of 128 x 8-bit memory. One of the blocks stores

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<sup>6</sup> <https://wiki.trenz-electronic.de/display/PD/TE0820+CPLD>

the 48-bit node address and is write protected, the other block is available for application use. It is accessible over I<sup>2</sup>C bus with slave device address 0x50.

## 7.8 Programmable Clock Generator

There is a Silicon Labs I<sup>2</sup>C programmable clock generator Si5338A (U10) chip on the module. It's output frequencies can be programmed using the I<sup>2</sup>C bus address 0x70 or 0x71. Default address is 0x70, IN4/I2C\_LSB pin must be set to high for address 0x71.

A 25.000000 MHz oscillator is connected to the pin IN3 and is used to generate the output clocks. The oscillator has its output enable pin permanently connected to 1.8V power rail, thus making output frequency available as soon as 1.8V is present. Three of the Si5338 clock outputs are connected to the FPGA. One is connected to a logic bank and the other two are connected to the GTR banks.

Once running, the frequency and other parameters can be changed by programming the device using the I<sup>2</sup>C bus connected between the FPGA (master) and clock generator (slave). For this, proper I<sup>2</sup>C bus logic has to be implemented in FPGA.

Signal	Frequency	Notes
IN1/IN2	user	External clock signal supply from B2B connector JM3, pins JM3-32/JM3-34
IN3	25.000000 MHz	Fixed input clock signal from reference clock generator SiT8008BI-73-18S-25.000000E (U11)
IN4	-	LSB of the default I <sup>2</sup> C address, wired to ground mean address is 0x70
IN5	-	Not connected
IN6	-	Wired to ground
CLK0 A/B	-	Bank 65 clock input, pins K9 and J9
CLK1 A/B	-	MGT reference clock 3 to FPGA Bank 505 PS GTR
CLK2 A/B	-	MGT reference clock 1 to FPGA Bank 505 PS GTR

Signal	Frequency	Notes
CLK3 A/B	-	Not connected

**Table 12:** General overview of the on-board quad clock generator I/O signals

## 7.9 Oscillators

The module has following reference clock signals provided by on-board oscillators and external source from carrier board:

Clock Source	Schematic Name	Frequency	Clock Destination
SiTime SiT8008BI oscillator, U32	PS_CLK	33.333333 MHz	Zynq MPSoC U1, pin R16
SiTime SiT8008BI oscillator, U11	-	25.000000 MHz	Quad PLL clock generator U10, pin 3, and Ethernet PHY U8, pin 34
SiT8008AI-73-XXS oscillator, U14	-	52.000000 MHz	USB PHY U18, Pin 26

**Table 13:** Reference clock signals

## 7.10 On-board LEDs

LED	Color	Connected to	Description and Notes
D1	Red	PS Config bank 503	Reflects inverted DONE signal when FPGA configuration is completed
D2	Green	System Controller CPLD, bank 3	Exact function is defined by SC CPLD firmware
D3	Red	PS Config bank 503	Reflects Zynq MPSoC control signal 'ERR_OUT'
D4	Green	PS Config bank 503	Reflects Zynq MPSoC control signal 'ERR_STATUS'

**Table 14:** On-board LEDs

## 8 Power and Power-on Sequence

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### 8.1 Power Supply

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Power supply with minimum current capability of 3A for system startup is recommended.

### 8.2 Power Consumption

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Power Input	Typical Current
VIN	TBD*
3.3VIN	TBD*

**Table 15:** Power consumption

\* TBD - To Be Determined soon with reference design setup.

Single 3.3V power supply with minimum current capability of 4A for system startup is recommended.

For the lowest power consumption and highest efficiency of the on-board DC-DC regulators it is recommended to power the module from one single 3.3V supply. All input power supplies should have a nominal value of 3.3V. Although the input power supplies can be powered up in any order, it is recommended to power them up simultaneously.

 To avoid any damage to the module, check for stabilized on-board voltages should be carried out (i.e. power good and enable signals) before powering up any Zynq's I/O bank voltages VCCO\_x. All I/Os should be tri-stated during power-on sequence.

### 8.3 Power Distribution Dependencies

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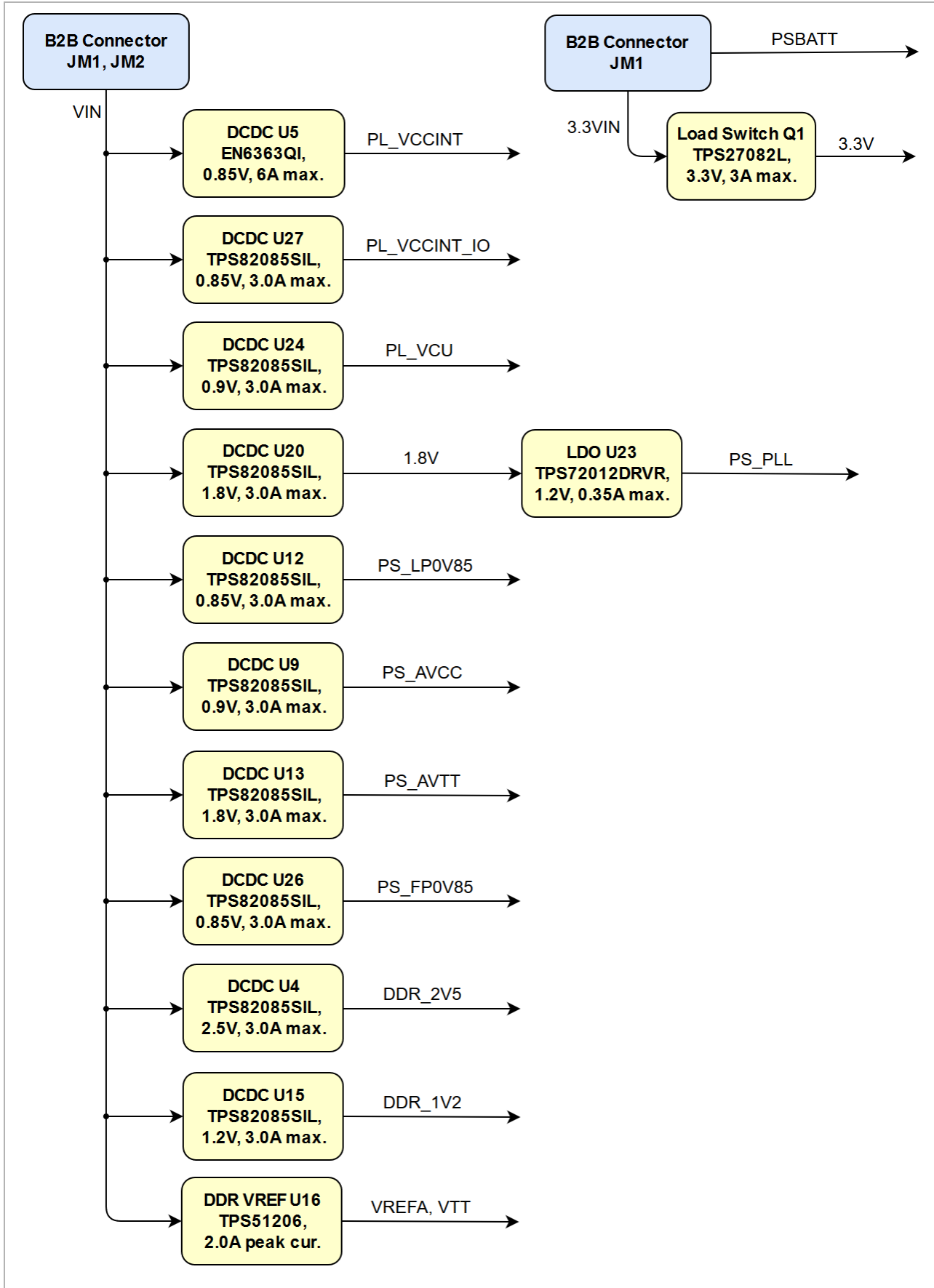


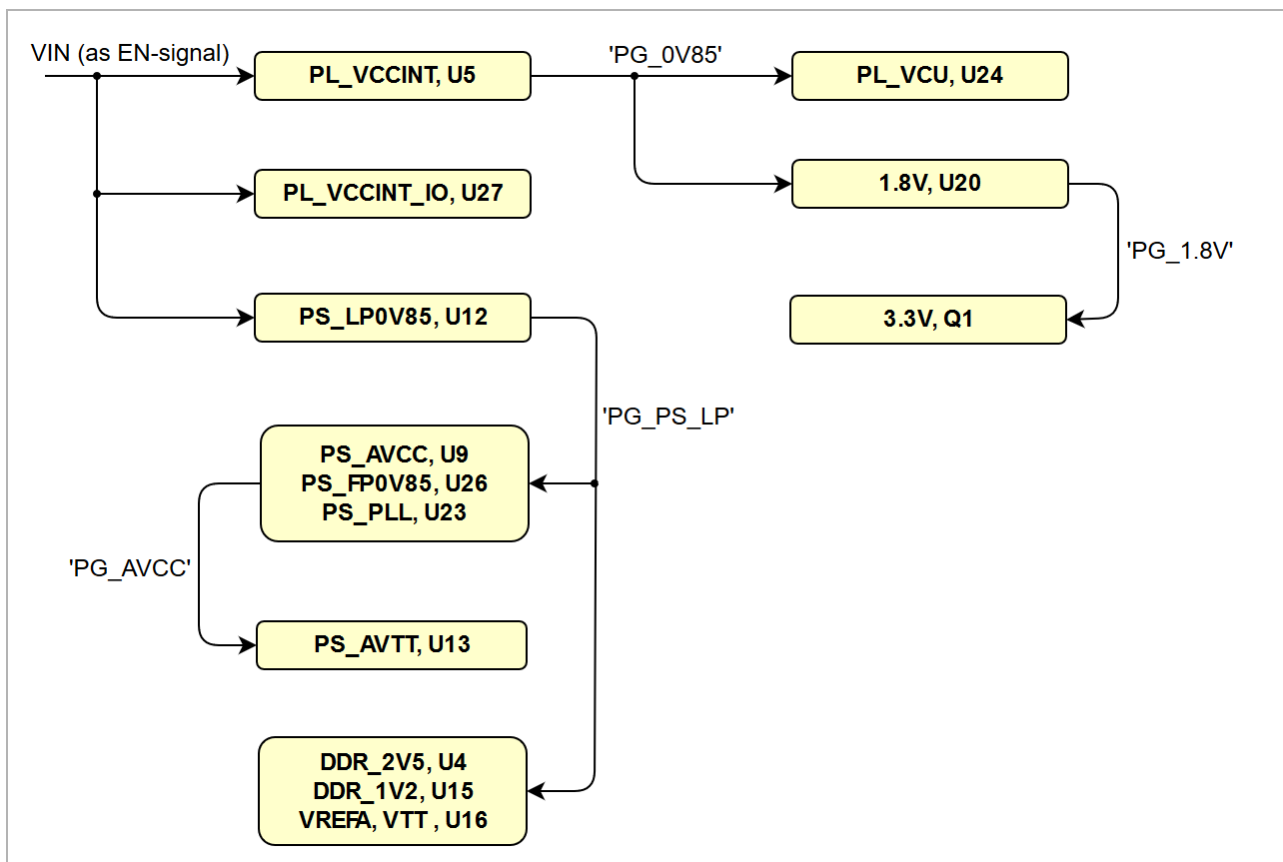
Figure 3: Figure 3: TE0820-03 Power Distribution Diagram

See also Xilinx datasheet DS925 for additional information. User should also check related base board documentation when intending base board design for TE0820 module.

## 8.4 Power-On Sequence

The TE0820 SoM meets the recommended criteria to power up the Xilinx Zynq chip properly by keeping a specific sequence of enabling the on-board DC-DC converters dedicated to the particular functional units of the Zynq chip and powering up the on-board voltages.

Following diagram clarifies the sequence of enabling the particular on-board voltages, which will power-up in descending order as listed in the blocks of the diagram:



**Figure 4: Figure 4: TE0820-03 Power-on Sequence Diagram**

For highest efficiency of the on-board DC-DC regulators, it is recommended to use one 3.3V power source for both VIN and 3.3VIN power rails. Although VIN and 3.3VIN can be powered up in any order, it is recommended to power them up simultaneously.

It is important that all carrier board I/Os are 3-stated at power-on until System Controller CPLD sets PGOOD signal high (B2B connector JM1, pin 30), or 3.3V is present on B2B connector JM2 pins 10 and 12, indicating that all on-module voltages have become stable and module is properly powered up.

See Xilinx datasheet DS925 for additional information. User should also check related carrier board documentation when choosing carrier board design for TE0715 module.



## 8.5 Power Rails

Power Rail Name on B2B Connector	JM1 Pins	JM2 Pins	Direction	Notes
VIN	1, 3, 5	2, 4, 6, 8	Input	Supply voltage from the carrier board
3.3V	-	10, 12	Output	Internal 3.3V voltage level
3.3VIN	13, 15	-	Input	Supply voltage from the carrier board
1.8V	39	-	Output	Internal 1.8V voltage level
JTAG VREF	-	91	Output	JTAG reference voltage. Attention: Net name on schematic is "3.3VIN"
VCCO_64	-	7, 9	Input	High performance I/O bank voltage
VCCO_65	-	5	Input	High performance I/O bank voltage
VCCO_66	9, 11	-	Input	High performance I/O bank voltage

**Table 16:** TE0820-03 power rails

## 8.6 Bank Voltages

Bank	Name on Schematic	Voltage	Range
64 HP	VCCO_64	User	HP: 1.0V to 1.8V
65 HP	VCCO_65	User	HP: 1.0V to 1.8V
66 HP	VCCO_66	User	HP: 1.0V to 1.8V
500 PSMIO	VCCO_PSI00_500	1.8V	-

Bank	Name on Schematic	Voltage	Range
501 PSMIO	VCCO_PSIO1_501	3.3V	-
502 PSMIO	VCCO_PSIO2_502	1.8V	-
503 PSCONFIG	VCCO_PSIO3_503	1.8V	-
504 PSDDR	VCCO_PSDDR_504	1.2V	-

**Table 17:** TE0820-03 I/O bank voltages

See Xilinx Zynq UltraScale+ datasheet DS925 for the voltage ranges allowed.

## 9 Board to Board Connectors

⚠ These connectors are hermaphroditic. Odd pin numbers on the module are connected to even pin numbers on the baseboard and vice versa.

4 x 5 modules use two or three [Samtec Razor Beam LSHM connectors](#)<sup>7</sup> on the bottom side.

- 2 x REF-189016-02 (compatible to LSHM-150-04.0-L-DV-A-S-K-TR), (100 pins, "50" per row)
- 1 x REF-189017-02 (compatible to LSHM-130-04.0-L-DV-A-S-K-TR), (60 pins, "30" per row) (depending on module)

### 9.1 Connector Mating height

When using the same type on baseboard, the mating height is 8mm. Other mating heights are possible by using connectors with a different height

Order number	Connector on baseboard	compatible to	Mating height
23836	REF-189016-01	LSHM-150-02.5-L-DV-A-S-K-TR	6.5 mm
	LSHM-150-03.0-L-DV-A-S-K-TR	LSHM-150-03.0-L-DV-A-S-K-TR	7.0 mm
23838	REF-189016-02	LSHM-150-04.0-L-DV-A-S-K-TR	8.0 mm
	LSHM-150-06.0-L-DV-A-S-K-TR	LSHM-150-06.0-L-DV-A-S-K-TR	10.0mm
26125	REF-189017-01	LSHM-130-02.5-L-DV-A-S-K-TR	6.5 mm
	LSHM-130-03.0-L-DV-A-S-K-TR	LSHM-130-03.0-L-DV-A-S-K-TR	7.0 mm
24903	REF-189017-02	LSHM-130-04.0-L-DV-A-S-K-TR	8.0 mm
	LSHM-130-06.0-L-DV-A-S-K-TR	LSHM-130-06.0-L-DV-A-S-K-TR	10.0mm

**Table 1: Connectors.**

The module can be manufactured using other connectors upon request.

<sup>7</sup> <https://www.samtec.com/technical-specifications/Default.aspx?SeriesMaster=LSHM>

## 9.2 Connector Speed Ratings

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The LSHM connector speed rating depends on the stacking height; please see the following table:

Stacking height	Speed rating
12 mm, Single-Ended	7.5 GHz / 15 Gbps
12 mm, Differential	6.5 GHz / 13 Gbps
5 mm, Single-Ended	11.5 GHz / 23 Gbps
5 mm, Differential	7.0 GHz / 14 Gbps

**Table 2: Speed rating.**

## 9.3 Current Rating

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Current rating of Samtec Razor Beam™ LSHM B2B connectors is 2.0A per pin (2 adjacent pins powered).

## 9.4 Connector Mechanical Ratings

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- Shock: 100G, 6 ms Sine
- Vibration: 7.5G random, 2 hours per axis, 3 axes total

## 10 Variants Currently In Production

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Trenz shop TE0820 overview page	
<a href="#">English page<sup>8</sup></a>	<a href="#">German page<sup>9</sup></a>

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<sup>8</sup> <https://shop.trenz-electronic.de/en/Products/Trenz-Electronic/TE08XX-Zynq-UltraScale/TE0820-Zynq-UltraScale/>

<sup>9</sup> <https://shop.trenz-electronic.de/de/Produkte/Trenz-Electronic/TE08XX-Zynq-UltraScale/TE0820-Zynq-UltraScale/>

## 11 Technical Specifications

### 11.1 Absolute Maximum Ratings

Parameter	Min	Max	Units	Notes
VIN supply voltage	-0.3	7	V	See EN6347QI and TPS82085SIL datasheets
3.3VIN supply voltage	-0.1	3.630	V	Xilinx DS925 and TPS27082L datasheet
PS I/O supply voltage, VCCO_PSIO	-0.5	3.630	V	Xilinx document DS925
PS I/O input voltage	-0.5	VCCO_PSIO + 0.55	V	Xilinx document DS925
HP I/O bank supply voltage, VCCO	-0.5	2.0	V	Xilinx document DS925
HP I/O bank input voltage	-0.55	VCCO + 0.55	V	Xilinx document DS925
PS GTR reference clocks absolute input voltage	-0.5	1.1	V	Xilinx document DS925
PS GTR absolute input voltage	-0.5	1.1	V	Xilinx document DS925
Voltage on SC CPLD pins	-0.5	3.75	V	Lattice Semiconductor MachXO2 datasheet
Storage temperature	-40	+85	°C	See eMMC datasheet

**Table 18:** Module absolute maximum ratings


### 11.2 Recommended Operating Conditions

Parameter	Min	Max	Units	Notes
VIN supply voltage	3.3	6	V	See TPS82085S datasheet

Parameter	Min	Max	Units	Notes
3.3VIN supply voltage	3.3	3.465	V	See LCMXO2-256HC, Xilinx DS925 datasheet
PS I/O supply voltage, VCCO_PSIO	1.710	3.465	V	Xilinx document DS925
PS I/O input voltage	-0.20	VCCO_PSIO + 0.20	V	Xilinx document DS925
HP I/O banks supply voltage, VCCO	0.950	1.9	V	Xilinx document DS925
HP I/O banks input voltage	-0.20	VCCO + 0.20	V	Xilinx document DS925
Voltage on SC CPLD pins	-0.3	3.6	V	Lattice Semiconductor MachXO2 datasheet
Operating Temperature Range	0	85	°C	Xilinx document DS925, extended grade Zynq temperature range

**Table 19:** Recommended operating conditions

Module operating temperature range depends also on customer design and cooling solution. Please contact us for options.

 See Xilinx datasheet DS925 for more information about absolute maximum and recommended operating ratings for the Zynq UltraScale+ chips.

## 11.3 Physical Dimensions

- Module size: 50 mm × 40 mm. Please download the assembly diagram for exact numbers.
- Mating height with standard connectors: 8 mm
- PCB thickness: 1.6 mm
- Highest part on PCB: approximately 5 mm. Please download the step model for exact numbers.

All dimensions are shown in millimeters.

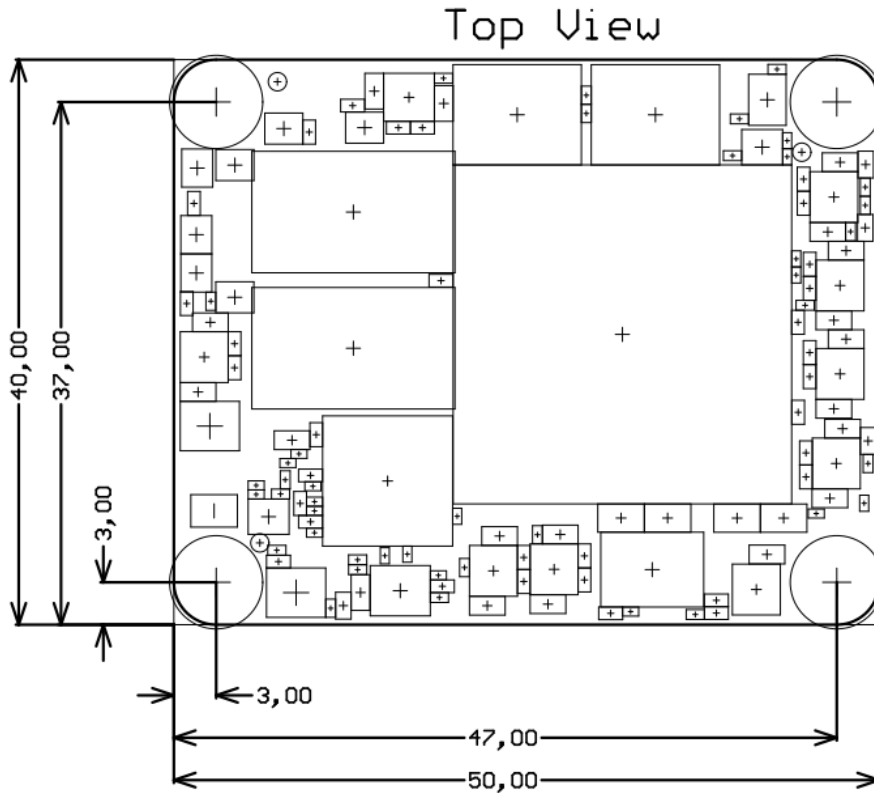
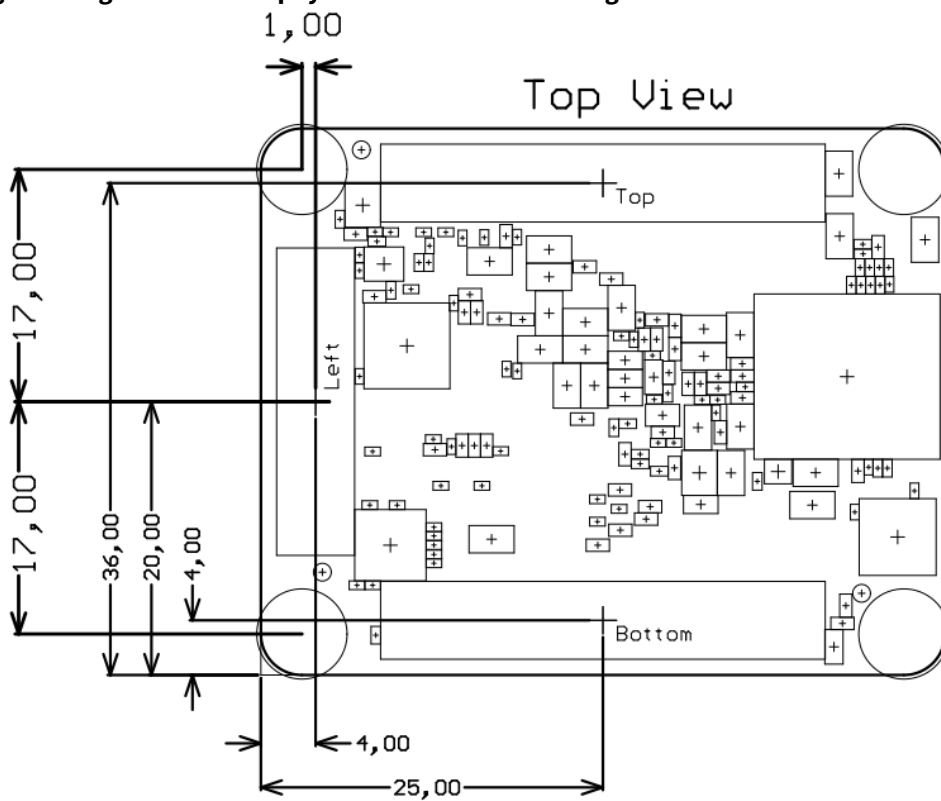


Figure 5: Figure 5: Module physical dimensions drawing





## 12 Revision History

### 12.1 Hardware Revision History


Date	Revision	Notes	PCN Link	Documentation Link
-	03	current available module revision	-	<a href="#">TE0820-03<sup>10</sup></a>
2017-08-17	02	--	<a href="#">PCN-20171117<sup>11</sup></a>	<a href="#">TE0820-02<sup>12</sup></a>
2016-12-23	01	Prototype only	-	<a href="#">TE0820-01<sup>13</sup></a>

**Table 20:** Hardware revision history table



**Figure 6:** Figure 6: Module hardware revision number

### 12.2 Document Change History

Date	Revision	Contributors	Description
 2020-06-08	<a href="#">v.91(see page 6)</a>	<a href="#">John Hartfiel<sup>14</sup></a>	<ul style="list-style-type: none"> <li>typo correction</li> </ul>

<sup>10</sup> [https://shop.trenz-electronic.de/Download/?path=Trenz\\_Electronic/Modules\\_and\\_Module\\_Carriers/4x5/TE0820/REV03](https://shop.trenz-electronic.de/Download/?path=Trenz_Electronic/Modules_and_Module_Carriers/4x5/TE0820/REV03)

<sup>11</sup> <https://wiki.trenz-electronic.de/display/PD/PCN-20171117+TE0820-02+SPI+Flash+Change>

<sup>12</sup> [https://shop.trenz-electronic.de/Download/?path=Trenz\\_Electronic/Modules\\_and\\_Module\\_Carriers/4x5/TE0820/REV02](https://shop.trenz-electronic.de/Download/?path=Trenz_Electronic/Modules_and_Module_Carriers/4x5/TE0820/REV02)

<sup>13</sup> [https://shop.trenz-electronic.de/Download/?path=Trenz\\_Electronic/Modules\\_and\\_Module\\_Carriers/4x5/TE0820/REV01](https://shop.trenz-electronic.de/Download/?path=Trenz_Electronic/Modules_and_Module_Carriers/4x5/TE0820/REV01)

<sup>14</sup> <https://wiki.trenz-electronic.de/display/~j.hartfiel>

Date	Revision	Contributors	Description
2020-03-16	b.87	John Hartfiel	<ul style="list-style-type: none"> <li>Corrected PLL section</li> <li>Corrected Designators USB, ETH PHY, CLK section</li> </ul>
2020-02-03	v.85	Martin Rohrmüller	<ul style="list-style-type: none"> <li>Corrected #MIOs for QSPI and USB in block diagram</li> </ul>
2019-11-28	v.81	Martin Rohrmüller	<ul style="list-style-type: none"> <li>typo and designator in section USB interface corrected</li> </ul>
2019-10-30	v.80	John Hartfiel	<ul style="list-style-type: none"> <li>typo correction</li> </ul>
2019-09-17	v79	Martin Rohrmüller	<ul style="list-style-type: none"> <li>Updated according to PCN-20190110: eMMC, QSPI-Flash</li> </ul>
2019-07-17	v.78	Martin Rohrmüller	<ul style="list-style-type: none"> <li>Corrected PJTAG Mio Pin29 in table 8</li> </ul>
2019-05-08	v.77	John Hartfiel	<ul style="list-style-type: none"> <li>Corrected EEPROM I2C Address</li> <li>Correction USB PHY connection</li> </ul>
2018-11-12	v.74	John Hartfiel	<ul style="list-style-type: none"> <li>update boot section</li> </ul>
2018-08-30	v.73	John Hartfiel	<ul style="list-style-type: none"> <li>typo correction</li> <li>update CPLD section</li> <li>add LEDs to component list</li> <li>add 3D picture of REV03 instead of REV01 picture</li> </ul>
2018-07-12	v.69	Ali Naseri	<ul style="list-style-type: none"> <li>Update PCB Rev03</li> </ul>
2018-06-11	v.61	John Hartfiel	<ul style="list-style-type: none"> <li>Rework chapter currently available products</li> <li>add PJTAG note to MIOtable</li> </ul>
2018-03-12	v.54		<ul style="list-style-type: none"> <li>Correction Power Rail Section</li> </ul>
2017-11-20	v.51	John Hartfiel	<ul style="list-style-type: none"> <li>Correction Default MIO Configuration Table</li> </ul>
2017-11-10	v.50	John Hartfiel	<ul style="list-style-type: none"> <li>Replace B2B connector section</li> </ul>

Date	Revision	Contributors	Description
2017-10-18	v.49	John Hartfiel	<ul style="list-style-type: none"> <li>add eMMC section</li> </ul>
2017-09-25	v.48	John Hartfiel	<ul style="list-style-type: none"> <li>Correction in the "Board to Board (B2B) I/Os" section</li> <li>Update in the "Variants Currently In Production" section</li> </ul>
2017-09-18	v.47	John Hartfiel	<ul style="list-style-type: none"> <li>Update PS MIO table</li> </ul>
2017-08-30	v.46	Jan Kumann	<ul style="list-style-type: none"> <li>MGT lanes section added.</li> </ul>
2017-08-24	v.36	John Hartfiel	<ul style="list-style-type: none"> <li>Correction in the "Key Features" section.</li> </ul>
2017-08-21	v.34	John Hartfiel	<ul style="list-style-type: none"> <li>"Initial delivery state" section updated.</li> </ul>
2017-08-21	v.33	Jan Kumann	<ul style="list-style-type: none"> <li>HW revision 02 block diagram added.</li> <li>Power distribution and power-on sequence diagram added.</li> <li>System Controller CPLD and DDR4 SDRAM sections added.</li> <li>TRM update to the template revision 1.6</li> <li>Weight section removed.</li> <li>Few minor corrections.</li> </ul>
2017-08-18	v.7	John Hartfiel	<ul style="list-style-type: none"> <li>Style changes</li> <li>Updated "Boot Mode", "HW Revision History", "Variants Currently In Production" sections</li> <li>Correction of MIO SD Pin-out, System Controller chapter</li> <li>Update and new sub-sections on "On Board Peripherals and Interfaces" sections</li> </ul>
2017-08-07	v.5	Jan Kumann	<ul style="list-style-type: none"> <li>Initial version</li> </ul>
--	all	<a href="#">Pedram Babakhani<sup>15</sup></a> , <a href="#">Ali Naseri<sup>16</sup></a> , <a href="#">Antti Lukats<sup>17</sup></a> , <a href="#">John</a>	<ul style="list-style-type: none"> <li>---</li> </ul>

<sup>15</sup> <https://wiki.trenz-electronic.de/display/~P.Babakhani>

<sup>16</sup> <https://wiki.trenz-electronic.de/display/~a.naseri>

Date	Revision	Contributors	Description
		Hartfiel <sup>18</sup> , Jan Kumann <sup>19</sup> , Martin Rohrmüller <sup>20</sup> , Susanne Kunath <sup>21</sup>	

**Table 21:** Document change history

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18 <https://wiki.trenz-electronic.de/display/~j.hartfiel>

19 <https://wiki.trenz-electronic.de/display/~j.kumann>

20 <https://wiki.trenz-electronic.de/display/~m.rohrmueller>

21 <https://wiki.trenz-electronic.de/display/~s.kunath>

## 13 Disclaimer

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## 13.7 REACH, RoHS and WEEE

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Trenz Electronic is registered under WEEE-Reg.-Nr. DE97922676.

 2019-06-07

 02.09.2017

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<sup>22</sup> <http://guidance.echa.europa.eu/>

<sup>23</sup> <https://echa.europa.eu/candidate-list-table>

<sup>24</sup> <http://www.echa.europa.eu/>