

Evaluating the ADPA7002 GaAs, pHEMT, MMIC, 1/2 W, 18 GHz to 44 GHz, Power Amplifier

FEATURES

- 2-layer Rogers 4350 evaluation board with heat sink
- End launch, 2.9 mm, RF connectors
- Through calibration path

EQUIPMENT NEEDED

- RF signal generator
- RF spectrum analyzer
- RF network analyzer
- 5 V, 1 A power supply
- 1.5 V/100 mA power supply

EVALUATION KIT CONTENTS

- 2-layer Rogers 4350 evaluation board with heat sink

GENERAL DESCRIPTION

The ADPA7002-EVALZ evaluation board consists of a two-layer printed circuit board (PCB) fabricated from 10 mil thick, Rogers 4350 copper clad mounted to an aluminum heat sink. The heat sink assists in providing thermal relief to the device, as well as mechanical support to the PCB. Mounting holes on the heat sink allow attachment to larger heat sinks for improved thermal management. The RFIN and RFOUT ports are populated by 2.9 mm, female coaxial connectors and their respective RF traces are of 50 Ω characteristic impedance. The board is populated with components suitable for use over the entire operating temperature range of the device. To calibrate out board trace losses, a through calibration path is provided between J3 and J4. J3 and J4 must be populated with RF connectors to use the through calibration path. Power, ground, gate control voltages, and the detector output voltages are accessed through two 8-pin headers (see Table 1 for header pinout).

The RF traces are 50 Ω , grounded coplanar waveguide. The package ground leads and the exposed paddle directly connect to the ground plane. Multiple vias are used to connect the top and bottom ground planes, with particular focus on the area directly beneath the ground paddle, in order to provide adequate electrical conduction and thermal conduction to the heat sink.

The power supply decoupling capacitors on the evaluation board represent the configuration used to characterize and qualify the device. There can be scope to reduce the number of capacitors, but this varies from system to system. It is recommended to remove or combine the largest capacitors that are farthest from the device first.

EVALUATION BOARD PHOTOGRAPHS

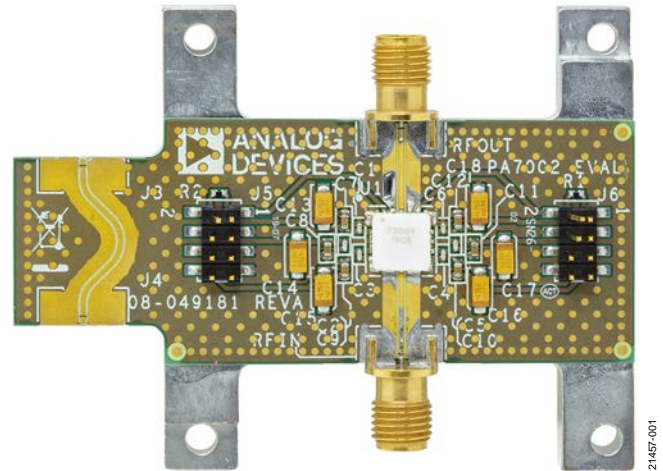


Figure 1. ADPA7002-EVALZ Top Side

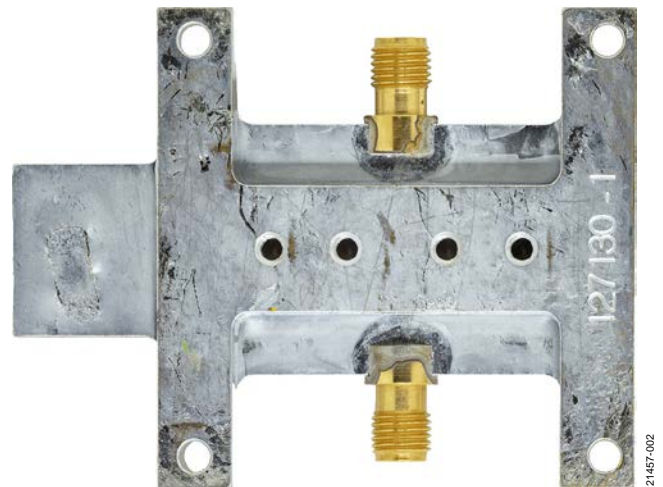


Figure 2. ADPA7002-EVALZ Bottom Side

For full details on the ADPA7002, see the ADPA7002 data sheet, which should be consulted in conjunction with this user guide when using these evaluation boards.

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REVISION HISTORY

12/2019—Rev. 0 to Rev. A

Changed 20 GHz to 44 GHz to 18 GHz to 44 GHz and ADPA7002AEHZ to ADPA7002.....	Throughout
Change to Table 2	4

11/2019—Revision 0: Initial Version

EVALUATION BOARD HARDWARE

OPERATING THE ADPA7002-EVALZ

A 5 V, 1 A power supply is required to provide the main bias to the evaluation board. The 5 V power supply must be connected in parallel to all of the VDDx lines (VDD1, VDD2, VDD3, and VDD4) through the J5 and J6 headers. In addition, a 0 V to -1.5 V, 100 mA power supply is required to provide the required gate control voltage. The -1.5 V power supply must be connected in parallel to the two VGG1 lines through the J5 and J6 headers.

Power-Up

Use the following biasing sequence during power-up:

1. Connect GND to RF and dc ground.
2. Initially, set all of the gate voltages and drain voltages (VGG1, VGG2, VDD1, VDD2, VDD3, and VDD4) to 0 V.
3. Set the VGG1 and VGG2 voltages to -1.5 V.
4. Set all the drain bias voltages, VDDx, to 5 V.
5. Increase the VGG1 and VGG2 voltages to achieve a quiescent drain current (I_{DQ}) of 700 mA.
6. Apply the RF signal.

Power-Down

Use the following biasing sequence during power-down:

1. Turn off the RF signal.
2. Decrease the VGG1 and VGG2 voltages to -1.5 V to achieve $I_{DQ} = 0$ mA (approximately).
3. Decrease all drain bias voltages, VDDx, to 0 V.
4. Decrease the VGG1 and VGG2 voltages to 0 V.

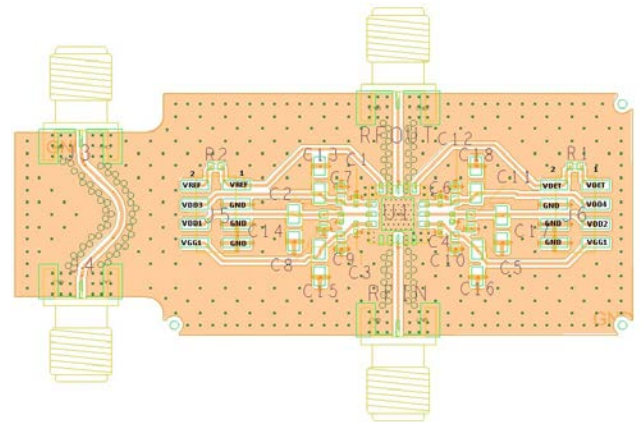


Figure 3. ADPA7002-EVALZ Assembly Drawing (J3 and J4 Not Installed)

Table 1. J5 and J6 Header Connections to ADPA7002

Connector ¹	Header Pin	ADPA7002 Mnemonic
J5	1	V _{REF}
J5	2	V _{REF1} (V _{REF} connected via a 100 kΩ resistor)
J5	3, 5, 7	GND
J5	4	V _{DD3}
J5	6	V _{DD1}
J5	8	V _{GG1}
J6	1	V _{DET1} (V _{REF} connected via a 100 kΩ resistor)
J6	2	V _{DET}
J6	3	V _{DD4}
J6	4, 6, 8	GND
J6	5	V _{DD2}
J6	7	V _{GG1}
J3 to J4		THRU_CAL (through calibration path)

¹ See Figure 5 for details.

THROUGH CALIBRATION PATH

Figure 4 shows the plot of the data in Table 2 of the through calibration path (J3 to J4). See Figure 5 for the evaluation board schematic.

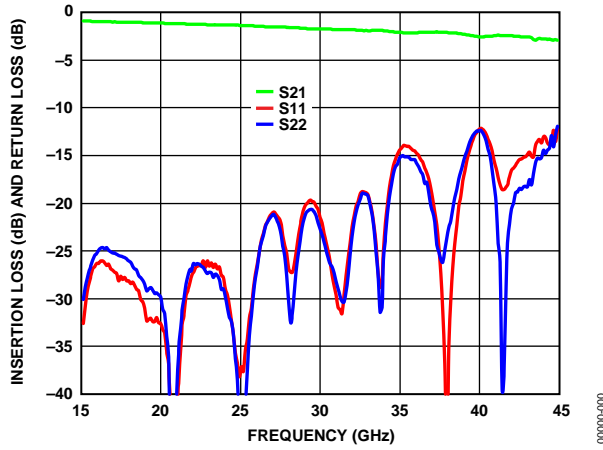


Figure 4. Insertion Loss and Return Loss of Through Calibration Path

Table 2. Insertion Loss and Return Loss of Through Calibration Path

Frequency (GHz)	Insertion Loss (dB)
18	-1.1
20	-1.2
22.5	-1.3
25	-1.4
27.5	-1.6
30	-1.8
32.5	-1.9
35	-2.1
37.5	-2.1
40	-2.6
42.5	-2.5
45	-3

EVALUATION BOARD SCHEMATIC

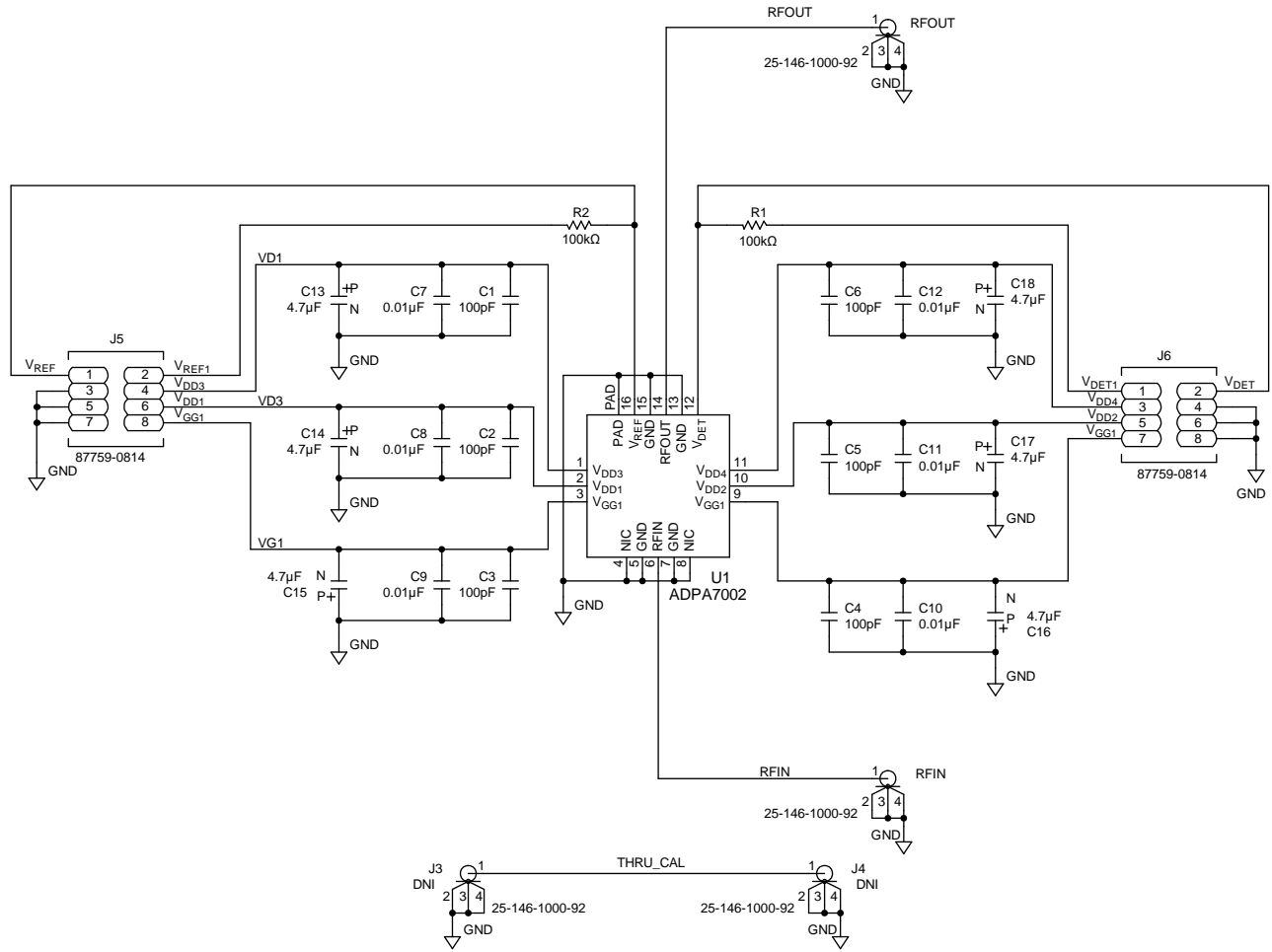


Figure 5. Evaluation Board Schematic

21457-003

ORDERING INFORMATION

BILL OF MATERIALS

Table 3.

Reference Designator	Description	Manufacturer	Device Number
C1 to C6	100 pF capacitors, ceramic	Kemet	C0402C101J5GACT U
C7 to C12	0.01 μ F capacitors, multilayer, ceramic, XR7	Kemet	C0603C103K5RECA UTO
C13 to C18	4.7 μ F capacitors, tantalum	AVX	TAJA475K020RNJ
J3, J4	Connectors, K jack edge, do not insert (DNI)	SRI Connector Gage Co.	25-146-1000-92
J5, J6	Connectors, PCB header, vertical, dual row, 8-position, 2 mm pitch	Molex	87759-0814
R1, R2	100 K resistors, thick film chip	Panasonic	ERJ-2GEJ104X
RFIN, RFOUT	Connectors K jack edge	SRI Connector Gage Co.	25-146-1000-92
U1	GaAs, pHEMPT, MMIC, $\frac{1}{2}$ W, 18 GHz to 44 GHz, power amplifier	Analog Devices	ADPA7002
Not Applicable	Aluminum heat sink (see Figure 2) Dimensions of heat sink: 2.51 inch \times 1.9 inch	Not applicable	Not applicable



ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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