# MC74HC253

# Dual 4-Input Data Selector/ Multiplexer with 3-State Outputs

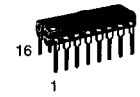
## High–Performance Silicon–Gate CMOS

The MC74HC253 is identical in pinout to the LS253. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

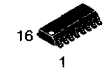
The Address inputs select one of four Data inputs from each multiplexer. Each multiplexer has an active–low Output Enable control and a three–state noninverting output.

The HC253 is similar in function to the HC153 which does not have three–state outputs.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No 7A
- Chip Complexity 108 FETs or 27 Equivalent Gates



**N SUFFIX**
PLASTIC PACKAGE
CASE 648–08

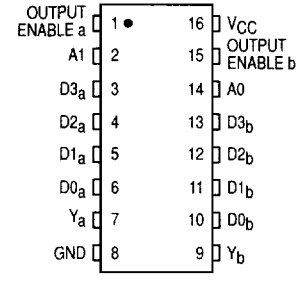


**D SUFFIX**
SOIC PACKAGE
CASE 751B–05

**ORDERING INFORMATION**

| | |
|---|---|
| MC74HCXXXN | Plastic |
| MC74HCXXXD | SOIC |

**PIN ASSIGNMENT**

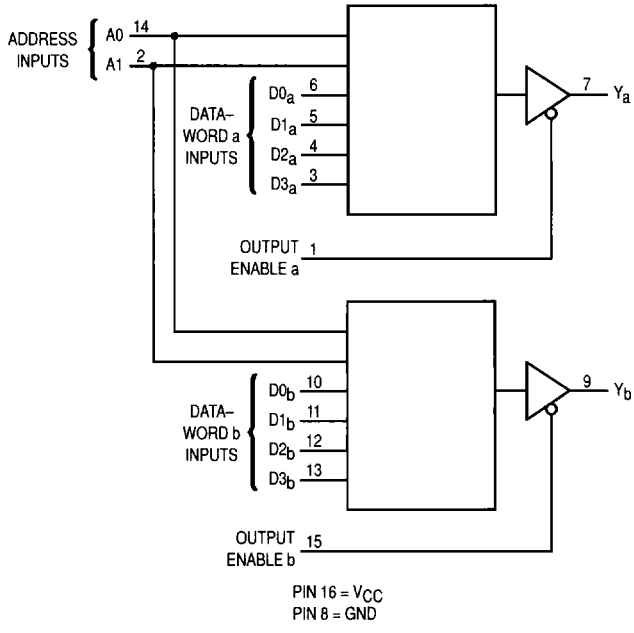



**FUNCTION TABLE**

| Inputs | | | Output |
|---|---|---|---|
| A1 | A0 | Output Enable | Y |
| X | X | H | Z |
| L | L | L | D0 |
| L | H | L | D1 |
| H | L | L | D2 |
| H | H | L | D3 |

D0, D1, D2, and D3 = the level of the respective Data Inputs.
Z = high impedance

**LOGIC DIAGRAM**



## MAXIMUM RATINGS*

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{CC}$ | DC Supply Voltage (Referenced to GND) | – 0.5 to + 7.0 | V |
| $V_{in}$ | DC Input Voltage (Referenced to GND) | – 1.5 to $V_{CC}$ + 1.5 | V |
| $V_{out}$ | DC Output Voltage (Referenced to GND) | – 0.5 to $V_{CC}$ + 0.5 | V |
| $I_{in}$ | DC Input Current, per Pin | ± 20 | mA |
| $I_{out}$ | DC Output Current, per Pin | ± 25 | mA |
| $I_{CC}$ | DC Supply Current, $V_{CC}$ and GND Pins | ± 50 | mA |
| $P_D$ | Power Dissipation in Still Air, Plastic DIP† | 750 | mW |
| | Power Dissipation in Still Air, SOIC Package† | 500 | mW |
| $T_{stg}$ | Storage Temperature | – 65 to + 150 | °C |
| $T_L$ | Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) | 260 | °C |

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: – 10 mW/°C from 65° to 125°C
SOIC Package: – 7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 2.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, $V_{in}$ and $V_{out}$ should be constrained to the range GND ≤ ($V_{in}$ or $V_{out}$) ≤ $V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or $V_{CC}$). Unused outputs must be left open.

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{CC}$ | DC Supply Voltage (Referenced to GND) | 2.0 | 6.0 | V |
| $V_{in}$, $V_{out}$ | DC Input Voltage, Output Voltage (Referenced to GND) | 0 | $V_{CC}$ | V |
| $T_A$ | Operating Temperature, All Package Types | – 55 | + 125 | °C |
| $t_r$, $t_f$ | Input Rise and Fall Time (Figure 1) $V_{CC}$ = 2.0 V | 0 | 1000 | ns |
| | $V_{CC}$ = 4.5 V | 0 | 500 | |
| | $V_{CC}$ = 6.0 V | 0 | 400 | |

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## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

| Symbol | Parameter | Test Conditions | $V_{CC}$ V | Guaranteed Limit – 55 to 25°C | Guaranteed Limit ≤ 85°C | Guaranteed Limit ≤ 125°C | Unit |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Minimum High–Level Input Voltage | $V_{out}$ = 0.1 V or $V_{CC}$ – 0.1 V, $\|I_{out}\|$ ≤ 20 μA | 2.0 | 1.5 | 1.5 | 1.5 | V |
| | | | 4.5 | 3.15 | 3.15 | 3.15 | |
| | | | 6.0 | 4.2 | 4.2 | 4.2 | |
| $V_{IL}$ | Maximum Low–Level Input Voltage | $V_{out}$ = 0.1 V or $V_{CC}$ – 0.1 V, $\|I_{out}\|$ ≤ 20 μA | 2.0 | 0.3 | 0.3 | 0.3 | V |
| | | | 4.5 | 0.9 | 0.9 | 0.9 | |
| | | | 6.0 | 1.2 | 1.2 | 1.2 | |
| $V_{OH}$ | Minimum High–Level Output Voltage | $V_{in}$ = $V_{IH}$ or $V_{IL}$, $\|I_{out}\|$ ≤ 20 μA | 2.0 | 1.9 | 1.9 | 1.9 | V |
| | | | 4.5 | 4.4 | 4.4 | 4.4 | |
| | | | 6.0 | 5.9 | 5.9 | 5.9 | |
| | | $V_{in}$ = $V_{IH}$ or $V_{IL}$, $\|I_{out}\|$ ≤ 4.0 mA | 4.5 | 3.98 | 3.84 | 3.70 | |
| | | $\|I_{out}\|$ ≤ 5.2 mA | 6.0 | 5.48 | 5.34 | 5.20 | |
| $V_{OL}$ | Maximum Low–Level Output Voltage | $V_{in}$ = $V_{IH}$ or $V_{IL}$, $\|I_{out}\|$ ≤ 20 μA | 2.0 | 0.1 | 0.1 | 0.1 | V |
| | | | 4.5 | 0.1 | 0.1 | 0.1 | |
| | | | 6.0 | 0.1 | 0.1 | 0.1 | |
| | | $V_{in}$ = $V_{IH}$ or $V_{IL}$, $\|I_{out}\|$ ≤ 4.0 mA | 4.5 | 0.26 | 0.33 | 0.40 | |
| | | $\|I_{out}\|$ ≤ 5.2 mA | 6.0 | 0.26 | 0.33 | 0.40 | |
| $I_{in}$ | Maximum Input Leakage Current | $V_{in}$ = $V_{CC}$ or GND | 6.0 | ± 0.1 | ± 1.0 | ± 1.0 | μA |
| $I_{OZ}$ | Maximum Three–State Leakage Current | Output in High–Impedance State, $V_{in}$ = $V_{IL}$ or $V_{IH}$, $V_{out}$ = $V_{CC}$ or GND | 6.0 | ± 0.5 | ± 5.0 | ± 10 | μA |
| $I_{CC}$ | Maximum Quiescent Supply Current (per Package) | $V_{in}$ = $V_{CC}$ or GND, $I_{out}$ = 0 μA | 6.0 | 8 | 80 | 160 | μA |

NOTE: Information on typical parametric values can be found in Chapter 2.

**AC ELECTRICAL CHARACTERISTICS** ($C_L$ = 50 pF, Input $t_r = t_f$ = 6 ns)

| Symbol | Parameter | $V_{CC}$ V | Guaranteed Limit | | | Unit |
|---|---|---|---|---|---|---|
| | | | – 55 to 25°C | ≤ 85°C | ≤ 125°C | |
| $t_{PLH}$, $t_{PHL}$ | Maximum Propagation Delay, Data to Output Y (Figures 1 and 3) | 2.0<br>4.5<br>6.0 | 140<br>28<br>24 | 175<br>35<br>30 | 210<br>42<br>36 | ns |
| $t_{PLH}$, $t_{PHL}$ | Maximum Propagation Delay, Address to Output Y (Figures 1 and 3) | 2.0<br>4.5<br>6.0 | 175<br>35<br>30 | 220<br>44<br>37 | 265<br>53<br>45 | ns |
| $t_{PLZ}$, $t_{PHZ}$ | Maximum Propagation Delay, Output Enable to Y (Figures 2 and 4) | 2.0<br>4.5<br>6.0 | 150<br>30<br>26 | 190<br>38<br>33 | 225<br>45<br>38 | ns |
| $t_{PZL}$, $t_{PZH}$ | Maximum Propagation Delay, Output Enable to Y (Figures 2 and 4) | 2.0<br>4.5<br>6.0 | 100<br>20<br>17 | 125<br>25<br>21 | 150<br>30<br>26 | ns |
| $t_{TLH}$, $t_{THL}$ | Maximum Output Transition Time, Any Output (Figures 1 and 3) | 2.0<br>4.5<br>6.0 | 75<br>15<br>13 | 95<br>19<br>16 | 110<br>22<br>19 | ns |
| $C_{in}$ | Maximum Input Capacitance | — | 10 | 10 | 10 | pF |
| $C_{out}$ | Maximum Three–State Output Capacitance (Output in High–Impedance State) | — | 15 | 15 | 15 | pF |

NOTES:
1. For propagation delays with loads other than 50 pF, see Chapter 2.
2. Information on typical parametric values can be found in Chapter 2.

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| | | Typical @ 25°C, $V_{CC}$ = 5.0 V | |
|---|---|---|---|
| $C_{PD}$ | Power Dissipation Capacitance (Per Multiplexer)* | 31 | pF |

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2.

## SWITCHING WAVEFORMS

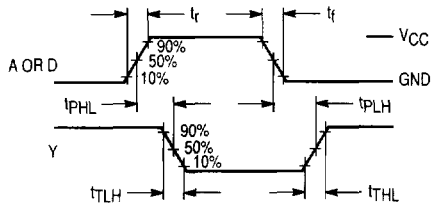



**Figure 1.**

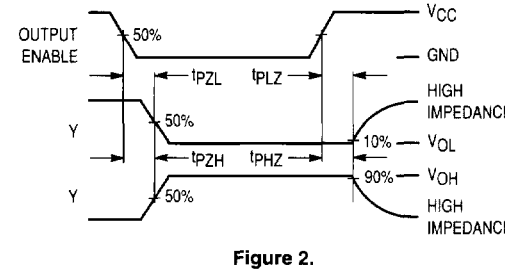
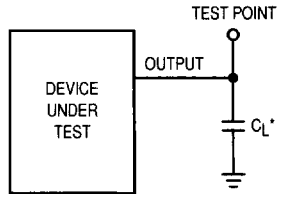


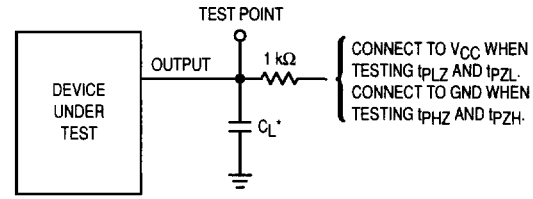

**Figure 2.**

## TEST CIRCUITS




* Includes all probe and jig capacitance

**Figure 3.**




* Includes all probe and jig capacitance

**Figure 4.**

## PIN DESCRIPTIONS

### DATA INPUTS

**$D0_a$ – $D3_a$, $D0_b$ – $D3_b$ (Pins 3, 4, 5, 6, 10, 11, 12, 13)**

Data inputs. When one of these pairs of inputs is selected and the outputs are enabled, the outputs assume the state of the respective inputs.

### CONTROL INPUTS

**A0, A1 (Pins 2, 14)**

Address inputs. These inputs select the pair of Data inputs to appear at the corresponding outputs.

**Output Enable (Pins 1, 15)**

Active–low three–state Output Enable. When a low level is applied to these inputs, the corresponding outputs are enabled. When a high level is applied, the outputs assume the high–impedance state.

### OUTPUTS

**$Y_a$, $Y_b$ (Pins 7, 9)**

Noninverting three–state outputs.

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## LOGIC DETAIL