HARRIS SEMICONDUCTOR

IH5052, IH5053

August 1997

Quad CMOS Analog Switches

Features

- Switches Greater Than 20V_{P-P} Signals with ±15V Supplies
- Quiescent Current ..... <10µA
- Break-Before-Make Switching
  - t_{OFF} (Typ)..... 500ns
  - t_{ON} (Typ)..... 1000ns
- TTL, CMOS Compatible
- IH5052 4 Normally Closed Switches
- IH5053 4 Normally Open Switches
- Low $r_{DS(ON)}$ (Typ) 80Ω

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
IH5052CDE	-0 to 70	16 Ld SBDIP	D16.3
IH5052MDE	-55 to 125	16 Ld SBDIP	D16.3
IH5053CDE	-0 to 70	16 Ld SBDIP	D16.3
IH5053MDE	-55 to 125	16 Ld SBDIP	D16.3

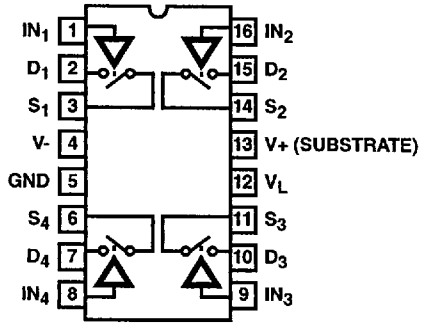
Description

The IH5052, IH5053 analog switches use an improved, high voltage CMOS technology, which provides performance advantages not previously available from solid state switches. Key performance advantages are TTL compatibility and ultra low-power operation. The quiescent current requirement is less than 10µA.

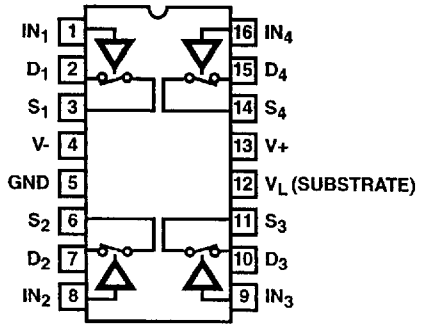
The IH5052, IH5053 also guarantees Break-Before-Make switching. This is accomplished by extending the t_{ON} time (1000ns) such that it exceeds t_{OFF} time (500ns). This insures that an ON channel will be turned OFF before an OFF channel can turn ON, and eliminates the need for external logic required to avoid channel to channel shorting during switching. With a logic "0" (0.8V or less) at its control inputs, the IH5052 switches are closed, while the IH5053 switches are closed with a logic "1" (2.4V or more) at its control inputs.

Pinouts

IH5052 (SBDIP)
TOP VIEW



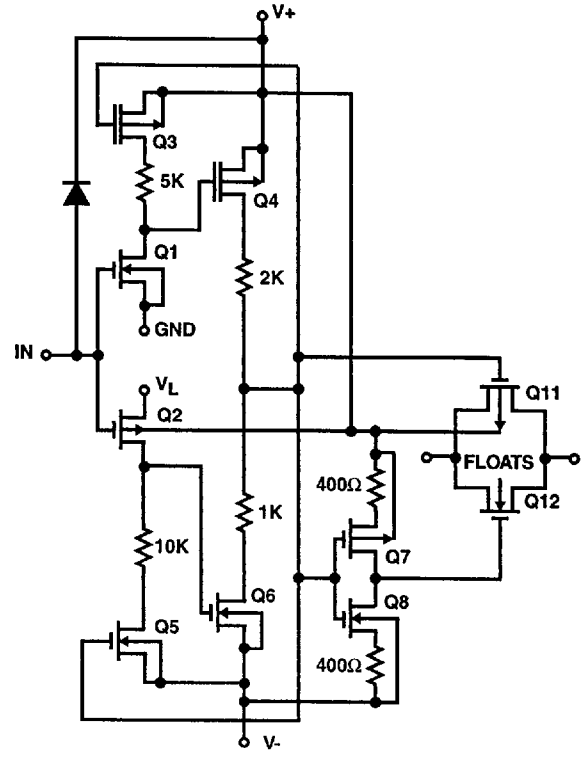
IH5053 (SBDIP)
TOP VIEW



Switch states shown for logic "1" input

Functional Diagram

(1/4 AS SHOWN)



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number 3131.1

Absolute Maximum Ratings

V+ to V- . . . . . <36V
V+ to V_D . . . . . <30V
V_D to V- . . . . . <30V
V_D to V_S . . . . . <±22V
V_L to V- . . . . . <33V
V_L to V_{IN} . . . . . <30V
V_L to GND . . . . . <20V
V_{IN} to GND . . . . . <20V
Continuous Current (S-D) 30mA
Peak Current (S-D) 70mA
(Pulsed at 1ms, 10% Duty Cycle, Max)

Operating Conditions

Temperature Ranges
M Suffix . . . . . -55°C to 125°C
C Suffix . . . . . 0°C to 70°C

Thermal Information

Maximum Junction Temperature (Ceramic Package) . . . . . 175°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications $T_A = 25°C$, V+ = +15V, V- = -15V, V_L = +5V

PER CHANNEL PARAMETER	TEST CONDITIONS	M SUFFIX			C SUFFIX			UNITS
		-55°C	25°C	125°C	0°C	25°C	70°C	
Input Logic Current, $I_{IN(ON)}$	V_{IN} = 2.4V (IH5053) = 0.8V (IH5052)	10	±1	10	-	±10	-	µA
Input Logic Current, $I_{IN(OFF)}$	V_{IN} = 0.8V (IH5053) = 2.4V (IH5052)	10	±1	10	-	±10	-	µA
Drain Source On Resistance, $r_{DS(ON)}$	I_S = 10mA, V_{ANALOG} = -10V to +10V	75	75	100	80	80	100	Ω
Channel to Channel, $r_{DS(ON)}$ Match	(Note 2)	-	25 (Typ)	-	-	30 (Typ)	-	Ω
Minimum Analog Signal Handling Capability, V_{ANALOG}	(Note 2)	-	±11 (Typ)	-	-	±10 (Typ)	-	V
Switch OFF Leakage Current, $I_{D(OFF)}$, $I_{S(OFF)}$	V_{ANALOG} = -10V to +10V	-	±1	100	-	±5	100	nA
Switch On Leakage Current, $I_{D(ON)} + I_{S(ON)}$	$V_D = V_S$ = -10V to +10V	-	±2	200	-	±10	100	nA
Switch "ON" Time, t_{ON}	R_L = 1kΩ, V_{ANALOG} = -10V to +10V See Figure 7	-	500	-	-	1000	-	ns
Switch "OFF" Time, t_{OFF}	R_L = 1kΩ, V_{ANALOG} = -10V to +10V See Figure 7	-	250	-	-	500	-	ns
Charge Injection, Q(INJ)	See Figure 8 (Note 2)	-	15 (Typ)	-	-	20 (Typ)	-	mV
Minimum Off Isolation Rejection Ratio OIRR	f = 1MHz, R_L = 100Ω, $C_L \leq$ 5pF See Figure 4 (Note 2)	-	54 (Typ)	-	-	50 (Typ)	-	dB
+ Power Supply Quiescent Current, I+	V+ = +15V, V- = -15V, V_L = +5V	10	10	100	10	10	100	µA
- Power Supply Quiescent Current, I-	V+ = +15V, V- = -15V, V_L = +5V	10	10	100	10	10	100	µA
+5V Supply Quiescent Current, I_{VL}	V+ = +15V, V- = -15V, V_L = +5V	10	10	100	10	10	100	µA
Minimum Channel to Channel Cross Coupling Rejection Ratio, CCRR	One Channel Off	-	54 (Typ)	-	-	50 (Typ)	-	dB

NOTE:

2. Typical values are for Design Aid only, not guaranteed nor production tested.

Typical Performance Curves

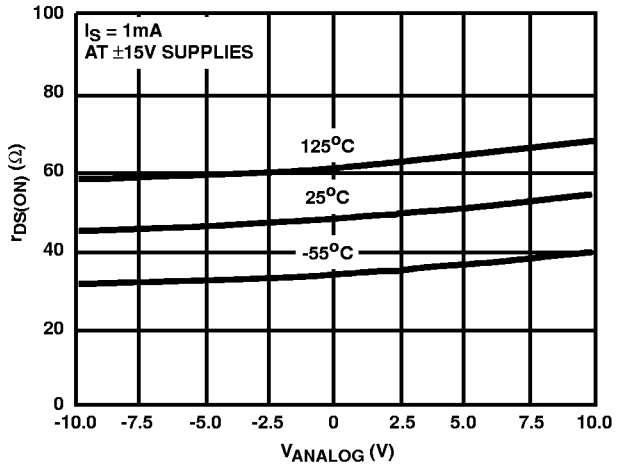


FIGURE 1. $r_{DS(ON)}$ vs V_{ANALOG}

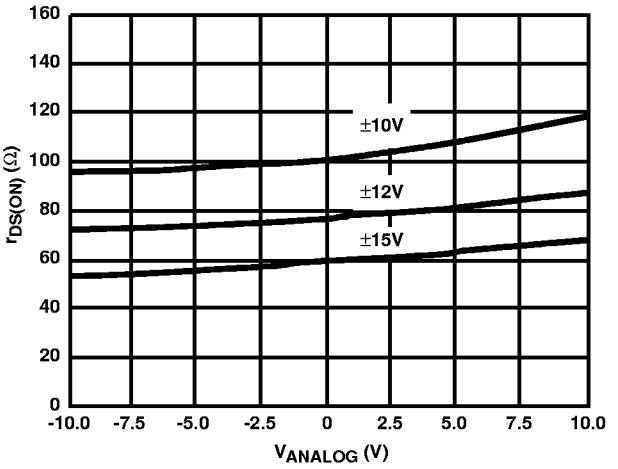


FIGURE 2. $r_{DS(ON)}$ vs POWER SUPPLY VOLTAGE

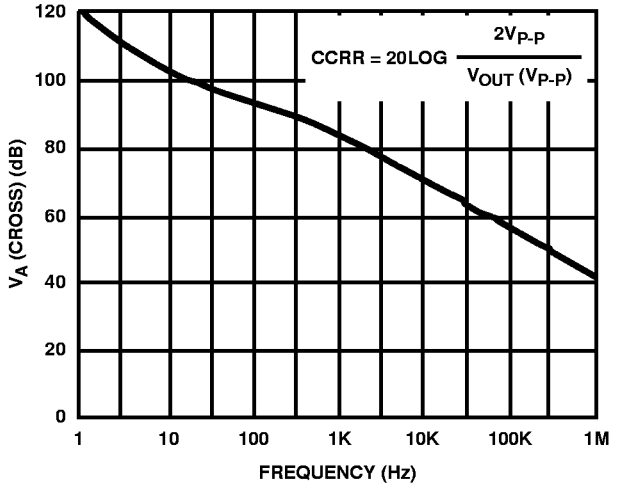


FIGURE 3A.

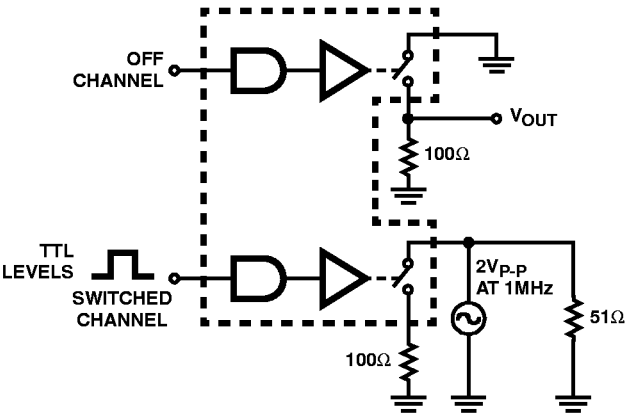


FIGURE 3B.

FIGURE 3. CROSS COUPLING REJECTION vs FREQUENCY

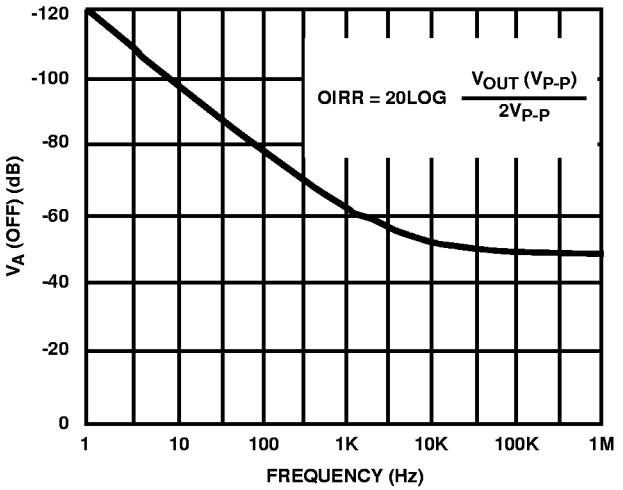


FIGURE 4A.

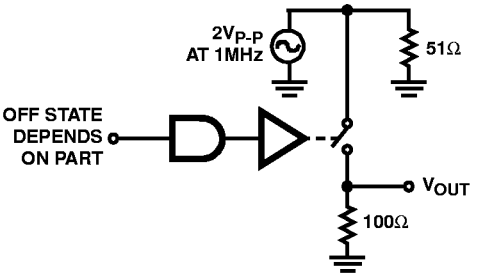


FIGURE 4B.

FIGURE 4. OFF ISOLATION vs FREQUENCY

Typical Performance Curves (Continued)

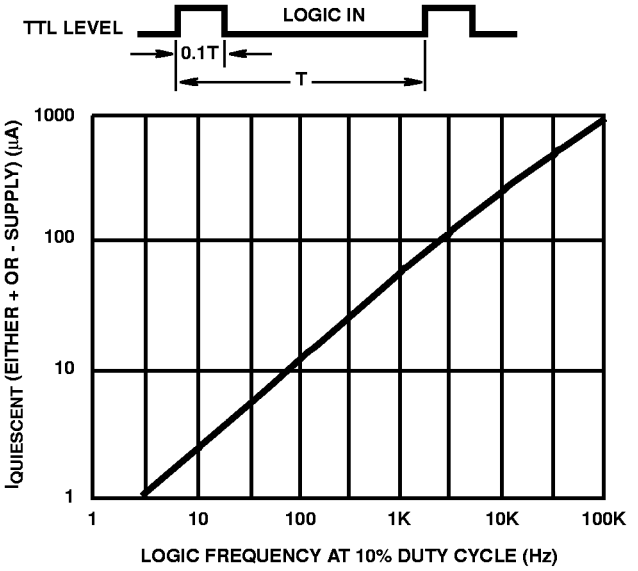


FIGURE 5. POWER SUPPLY QUIESCENT CURRENT vs LOGIC FREQUENCY RATE

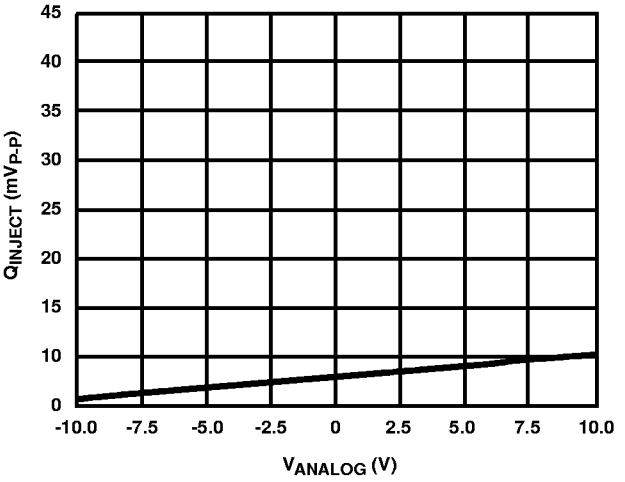


FIGURE 6. CHARGE INJECTION vs V_{ANALOG} (SEE FIGURE 8) C_L = 10,000pF

Test Circuits

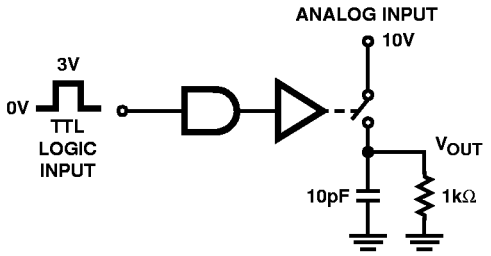


FIGURE 7.

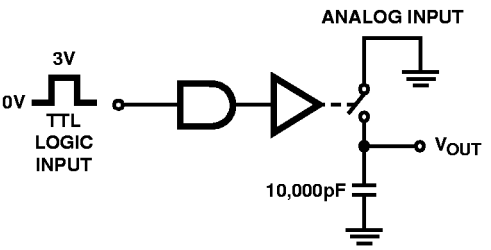


FIGURE 8.

Typical Applications

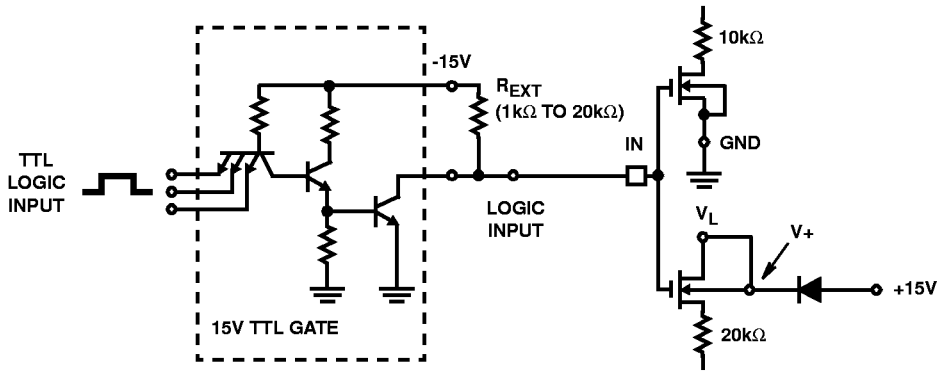


FIGURE 9. +15V OPEN COLLECTOR TTL INTERFACE TO IH5052/IH5053

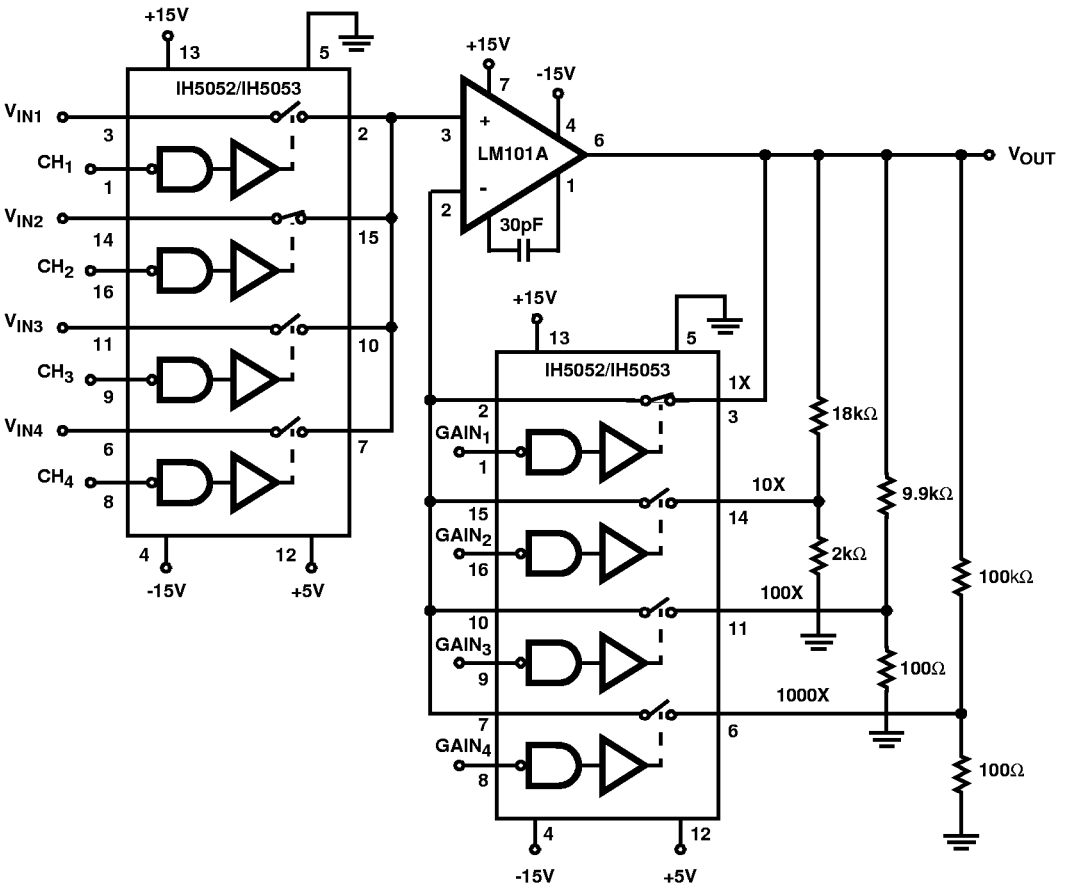


FIGURE 10. ACTIVE LOW PASS FILTER WITH DIGITALLY SELECTED BREAK FREQUENCY

Typical Applications

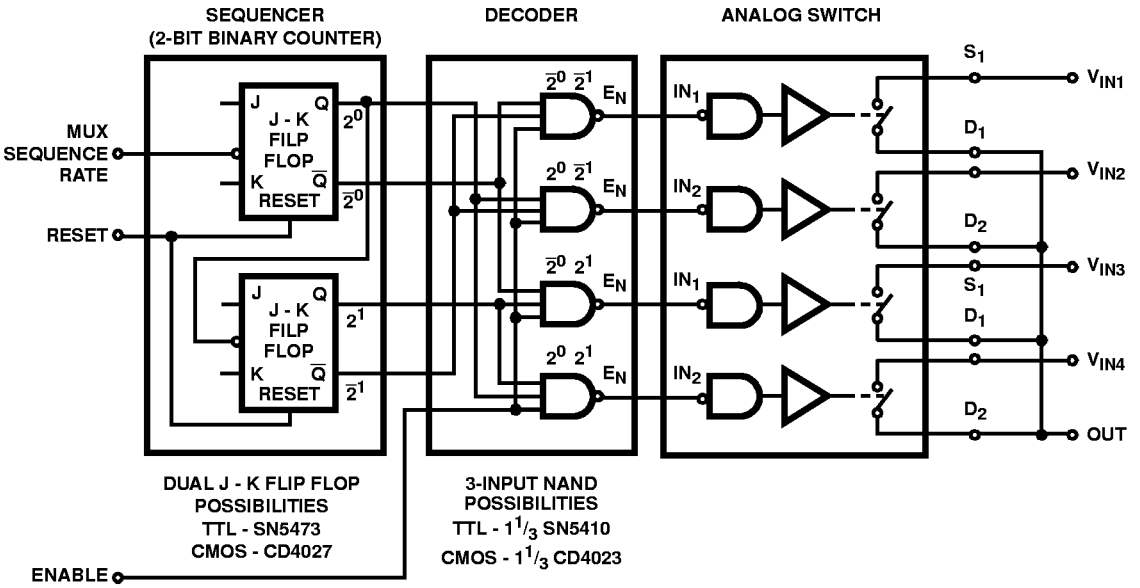


FIGURE 11. 4-CHANNEL SEQUENCING MUX

TRUTH TABLE (IH5052)

ENABLE	MUX SEQUENCE RATE	SEQUENCER OUTPUT		SWITCH STATES (- DENOTES OFF)			
		2^0	2^1	SW1	SW2	SW3	SW4
0	0	0	0	-	-	-	-
1	0	0	0	ON	-	-	-
1	1 Pulse	1	0	-	ON	-	-
1	2 Pulses	0	1	-	-	-	-
1	3 Pulses	1	1	-	-	-	ON
1	4 Pulses	0	0	ON	-	-	-

A Latching DPDT Switch

The latch feature insures positive switching action in response to non-repetitive or erratic commands. The A_1 and A_2 inputs are normally low. A HIGH input to A_2 turns S_1 and S_2 ON, a HIGH to A_1 turns S_3 and S_4 ON. Desirable for use with limit detectors, peak detectors, or mechanical contact closures.

TRUTH TABLE (IH5052)

COMMAND		STATE OF SWITCHES AFTER COMMAND	
A_2	A_1	S_3 and S_4	S_1 and S_2
0	0	Same	Same
0	1	On	Off
1	0	Off	On
1	1	Indeterminate	

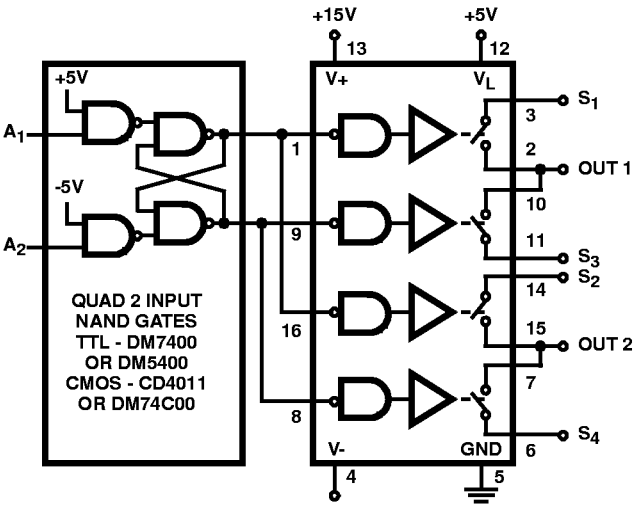


FIGURE 12. A LATCHING DPDT