DRV8436E/P Dual H-Bridge Motor Drivers With Integrated Current Sense and Smart Tune Technology

1 Features

- Dual H-bridge motor driver
  - One bipolar stepper motor
  - Dual bidirectional brushed-DC motors
  - Four unidirectional brushed-DC motors
- Integrated current sense functionality
  - No sense resistors required
  - ±7.5% Full-scale current accuracy
- 4.5- to 48-V Operating supply voltage range
- Multiple control interface options
  - PHASE/ENABLE
  - PWM
- Smart tune decay technology, fixed slow, fast and mixed decay options
- Low $R_{DS(ON)}$: 900 mΩ HS + LS at 24 V, 25°C
- High Current Capacity Per Bridge: 2.4-A peak, 1.5-A Full-Scale, 1.1-A rms
- Configurable Off-Time PWM Chopping
  - 7, 16, 24 or 32 µs
- Supports 1.8-V, 3.3-V, 5.0-V logic inputs
- Low-current sleep mode (2 µA)
- Spread spectrum clocking for low electromagnetic interference (EMI)
- Small package and footprint
- Protection features
  - VM undervoltage lockout (UVLO)
  - Charge pump undervoltage (CPUV)
  - Overcurrent protection (OCP)
  - Thermal shutdown (OTSD)
  - Fault condition output (nFAULT)

2 Applications

- Printers and scanners
- ATMs, currency counters, and EPOS
- Office and home automation
- Factory automation and robotics
- Major and small home appliances
- IP Network Camera and Video Conferencing
- Vacuum, humanoid, and toy robotics

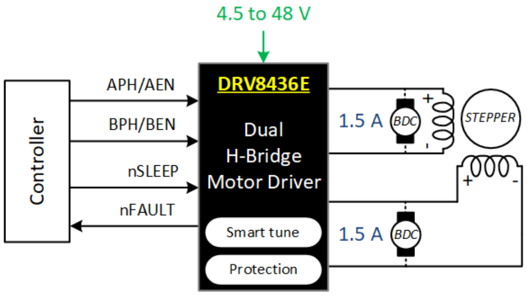
3 Description

The DRV8436E/P devices are dual H-bridge motor drivers for a wide variety of industrial applications. The devices can be used for driving two DC motors, or a bipolar stepper motor. The output stage of the driver consists of N-channel power MOSFETs configured as two full H-bridges, charge pump regulator, current sensing and regulation, and protection circuitry. The integrated current sensing uses an internal current mirror architecture, removing the need for a large power shunt resistor, saving board area and reducing system cost. A low-power sleep mode is provided to achieve ultra- low quiescent current draw by shutting down most of the internal circuitry. Internal protection features are provided for supply undervoltage lockout (UVLO), charge pump undervoltage (CPUV), output overcurrent (OCP), and device overtemperature (OTSD). The DRV8436E/P is capable of driving up to 1.5-A full scale or 1.1-A rms output current per H-bridge (dependent on PCB design).

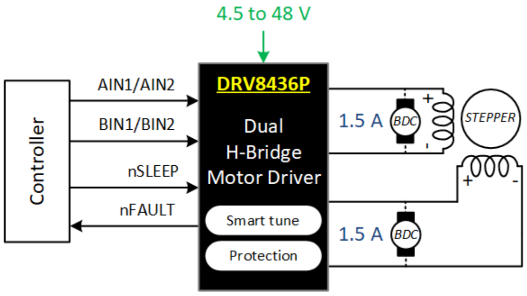
Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
DRV8436EPWPR	HTSSOP (28)	9.7 mm x 4.4 mm
DRV8436ERGER	VQFN (24)	4.0 mm x 4.0 mm
DRV8436PPWPR	HTSSOP (28)	9.7 mm x 4.4 mm
DRV8436PRGER	VQFN (24)	4.0 mm x 4.0 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



DRV8436E Simplified Schematic



DRV8436P Simplified Schematic

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (August 2020) to Revision B (July 2022)	Page
• Added Typical Characteristics curves	10
• Updated HTSSOP and QFN layout examples	33

Changes from Revision * (June 2020) to Revision A (August 2020)	Page
• Changed device status to "Production Data"	1

Device Options

PART NUMBER	CONTROL INTERFACE
DRV8436E	PHASE/ENABLE
DRV8436P	PWM

5 Pin Configuration and Functions

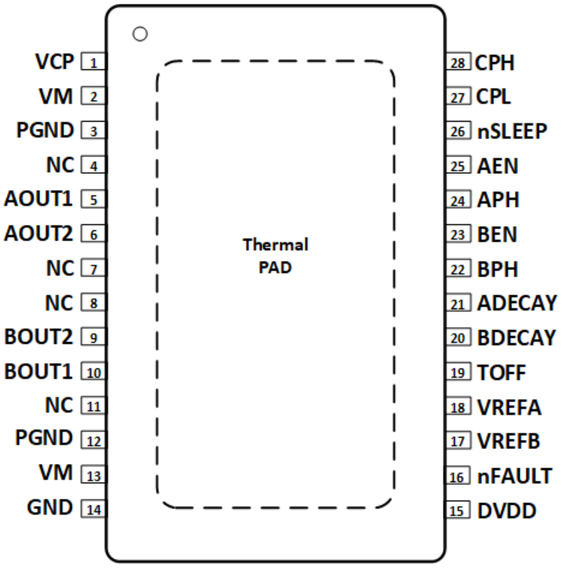


Figure 5-1. PWP PowerPAD™ Package 28-Pin HTSSOP Top View DRV8436E

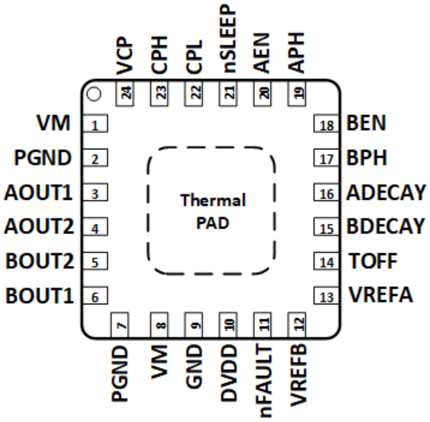


Figure 5-2. RGE Package 24-Pin VQFN with Exposed Thermal PAD Top View DRV8436E

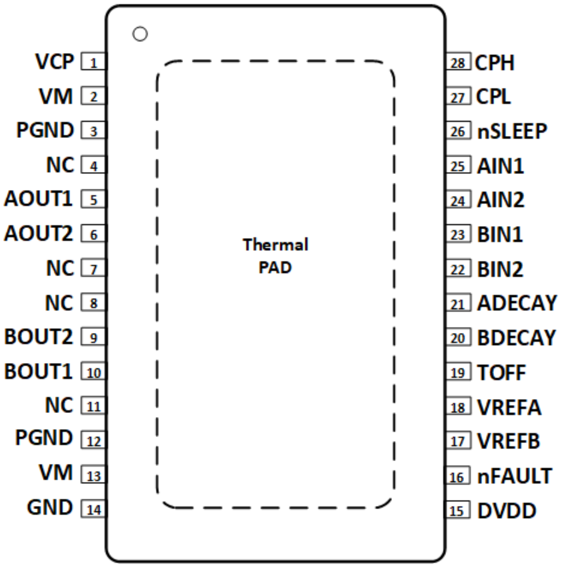


Figure 5-3. PWP PowerPAD™ Package 28-Pin HTSSOP Top View DRV8436P

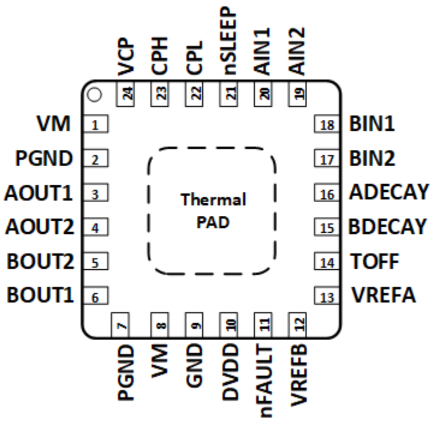


Figure 5-4. RGE Package 24-Pin VQFN with Exposed Thermal PAD Top View DRV8436P

Table 5-1. Pin Functions

PIN					TYPE	DESCRIPTION
NAME	PWP		RGE			
	DRV8436E	DRV8436P	DRV8436E	DRV8436P		
ADECAY	21	21	16	16	I	Decay mode setting pins. Set the decay mode for bridge A; quad-level pin.
AEN	25	—	20	—	I	Bridge A enable input. Logic high enables bridge A; logic low disables the bridge Hi-Z.
AIN1	—	25	—	20	I	Bridge A PWM input. Logic controls the state of H-bridge A; internal pulldown.
AIN2	—	24	—	19	I	Bridge A PWM input. Logic controls the state of H-bridge A; internal pulldown.
AOUT1	5	5	3	3	O	Winding A output. Connect to motor winding.
AOUT2	6	6	4	4	O	Winding A output. Connect to motor winding.
APH	24	—	19	—	I	Bridge A phase input. Logic high drives current from AOUT1 to AOUT2.

Table 5-1. Pin Functions (continued)

PIN					TYPE	DESCRIPTION
NAME	PWP		RGE			
	DRV8436E	DRV8436P	DRV8436E	DRV8436P		
VREFA	18	18	13	13	I	Reference voltage input. Voltage on this pin sets the full scale chopping current in H-bridge A. Maximum value 3.3 V. DVDD can be used to provide VREF through a resistor divider.
BDECAY	20	20	15	15	I	Decay mode setting pins. Set the decay mode for bridge B; quad-level pin.
BEN	23	—	18	—	I	Bridge B enable input. Logic high enables bridge B; logic low disables the bridge Hi-Z.
BIN1	—	23	—	18	I	Bridge B PWM input. Logic controls the state of H-bridge B; internal pulldown.
BIN2	—	22	—	17	I	Bridge B PWM input. Logic controls the state of H-bridge B; internal pulldown.
BOUT1	10	10	6	6	O	Winding B output. Connect to motor winding.
BOUT2	9	9	5	5	O	Winding B output. Connect to motor winding.
BPH	22	—	17	—	I	Bridge B phase input. Logic high drives current from BOUT1 to BOUT2.
VREFB	17	17	12	12	I	Reference voltage input. Voltage on this pin sets the full scale chopping current in H-bridge B. Maximum value 3.3 V. DVDD can be used to provide VREF through a resistor divider.
CPH	28	28	23	23	PWR	Charge pump switching node. Connect a X7R, 0.022-µF, VM-rated ceramic capacitor from CPH to CPL.
CPL	27	27	22	22		
GND	14	14	9	9	PWR	Device ground. Connect to system ground.
TOFF	19	19	14	14	I	Sets the decay mode off-time during current chopping; quad-level pin.
DVDD	15	15	10	10	PWR	Logic supply voltage. Connect a X7R, 0.47-µF, 6.3-V or 10-V rated ceramic capacitor to GND.
VCP	1	1	24	24	O	Charge pump output. Connect a X7R, 0.22-µF, 16-V ceramic capacitor to VM.
VM	2, 13	2, 13	1, 8	1, 8	PWR	Power supply. Connect to motor supply voltage and bypass to GND with two 0.01-µF ceramic capacitors (one for each pin) plus a bulk capacitor rated for VM.
PGND	3, 12	3, 12	2, 7	2, 7	PWR	Power ground. Both PGND pins are shorted internally. Connect to system ground on PCB.
nFAULT	16	16	11	11	O	Fault indication. Pulled logic low with fault condition; open-drain output requires an external pullup resistor.
nSLEEP	26	26	21	21	I	Sleep mode input. Logic high to enable device; logic low to enter low-power sleep mode; internal pulldown resistor.
NC	4, 7, 8, 11	4, 7, 8, 11	-	-	-	No Connect pins. Leave these pins unconnected.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range referenced with respect to GND (unless otherwise noted) (1)

	MIN	MAX	UNIT
Power supply voltage (VM)	–0.3	50	V
Charge pump voltage (VCP, CPH)	–0.3	V_{VM} + 7	V
Charge pump negative switching pin (CPL)	–0.3	V_{VM}	V
nSLEEP pin voltage (nSLEEP)	–0.3	V_{VM}	V
Internal regulator voltage (DVDD)	–0.3	5.75	V
Control pin voltage (APH, AEN, BPH, BEN, AIN1, AIN2, BIN1, BIN2, nFAULT, ADECAY, BDECAY, TOFF)	–0.3	5.75	V
Open drain output current (nFAULT)	0	10	mA
Reference input pin voltage (VREFA, VREFB)	–0.3	5.75	V
Continuous phase node pin voltage (AOUT1, AOUT2, BOUT1, BOUT2)	–1	V_{VM} + 1	V
Transient 100 ns phase node pin voltage (AOUT1, AOUT2, BOUT1, BOUT2)	–3	V_{VM} + 3	V
Peak drive current (AOUT1, AOUT2, BOUT1, BOUT2)	Internally Limited		A
Operating ambient temperature, T_J	–40	125	°C
Operating junction temperature, T_J	–40	150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001		±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101	Corner pins for PWP (1, 14, 15, and 28)	±750	
			Other pins	±500	

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{VM}	Supply voltage range for normal (DC) operation	4.5	48	V
V_I	Logic level input voltage	0	5.3	V
VREF	Reference rms voltage range (VREFA, VREFB)	0.05	3.3	V
f_{PWM}	Applied PWM signal (APH, AEN, BPH, BEN, AIN1, AIN2, BIN1, BIN2)	0	100	kHz
I_{FS}	Motor full-scale current (xOUTx)	0	1.5	A
I_{rms}	Motor RMS current (xOUTx)	0	1.1	A
T_A	Operating ambient temperature	–40	125	°C
T_J	Operating junction temperature	–40	150	°C

6.4 Thermal Information

THERMAL METRIC(1)		PWP (HTSSOP)	RGE (VQFN)	UNIT
		28 PINS	24 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	31.3	41.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	26.0	32.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	11.5	18.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.5	0.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	11.5	18.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.4	4.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

Typical values are at T_A = 25°C and V_{VM} = 24 V. All limits are over recommended operating conditions, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES (VM, DVDD)						
I_{VM}	VM operating supply current	nSLEEP = 1, No motor load, IC Enabled		5	7	mA
I_{VMQ}	VM sleep mode supply current	nSLEEP = 0		2	4	µA
t_{SLEEP}	Sleep time	nSLEEP = 0 to sleep-mode	75			µs
t_{WAKE}	Wake-up time	nSLEEP = 1 to output transition		0.6	0.9	ms
t_{ON}	Turn-on time	VM > UVLO to output transition		0.6	0.9	ms
V_{DVDD}	Internal regulator voltage	No external load, 6 V < V_{VM} < 45 V	4.5	5	5.5	V
CHARGE PUMP (VCP, CPH, CPL)						
V_{VCP}	VCP operating voltage			V_{VM} + 5		V
$f_{(VCP)}$	Charge pump switching frequency	V_{VM} > UVLO; nSLEEP = 1		400		kHz
LOGIC-LEVEL INPUTS (APH, AEN, BPH, BEN, AIN1, AIN2, BIN1, BIN2, nSLEEP)						
V_{IL}	Input logic-low voltage		0		0.6	V
V_{IH}	Input logic-high voltage		1.5		5.5	V
V_{HYS}	Input logic hysteresis			150		mV
I_{IL}	Input logic-low current	V_{IN} = 0 V	–1		1	µA
I_{IH}	Input logic-high current	V_{IN} = 5 V			50	µA
t_{PD}	Propagation delay	xPH, xEN, xINx input to current change		850		ns
QUAD-LEVEL INPUTS (ADECAY, BDECAY, TOFF)						
V_{I1}	Input logic-low voltage	Tied to GND	0		0.6	V
V_{I2}		330kΩ ± 5% to GND	1	1.25	1.4	V
V_{I3}	Input Hi-Z voltage	Hi-Z (>500kΩ to GND)	1.8	2	2.2	V
V_{I4}	Input logic-high voltage	Tied to DVDD	2.7		5.5	V
I_O	Output pull-up current			10		µA
CONTROL OUTPUTS (nFAULT)						
V_{OL}	Output logic-low voltage	I_O = 5 mA			0.4	V
I_{OH}	Output logic-high leakage	V_{VM} = 24 V	–1		1	µA
MOTOR DRIVER OUTPUTS (AOUT1, AOUT2, BOUT1, BOUT2)						
$R_{DS(ON)}$	High-side FET on resistance	V_{VM} = 24 V, T_J = 25°C, I_O = -1 A		450	550	mΩ
		V_{VM} = 24 V, T_J = 125°C, I_O = -1 A		700	850	mΩ
		V_{VM} = 24 V, T_J = 150°C, I_O = -1 A		780	950	mΩ
$R_{DS(ON)}$	Low-side FET on resistance	V_{VM} = 24 V, T_J = 25°C, I_O = 1 A		450	550	mΩ
		V_{VM} = 24 V, T_J = 125°C, I_O = 1 A		700	850	mΩ
		V_{VM} = 24 V, T_J = 150°C, I_O = 1 A		780	950	mΩ
t_{SR}	Output slew rate	VM = 24V, I_O = 0.5 A, Between 10% and 90%		150		V/µs
PWM CURRENT CONTROL (VREFA, VREFB)						
K_V	Transimpedance gain			2.2		V/A
t_{OFF}	PWM off-time	TOFF = 0		7		µs
		TOFF = 1		16		
		TOFF = Hi-Z		24		
		TOFF = 330 kΩ to GND		32		

Typical values are at T_A = 25°C and V_{VM} = 24 V. All limits are over recommended operating conditions, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ΔI_{TRIP}	Current trip accuracy	I_O = 1.5 A, 10% to 20% current setting	–13		10	%
		I_O = 1.5 A, 20% to 67% current setting	–8		8	
		I_O = 1.5 A, 67% to 100% current setting	–7.5		7.5	
$I_{O,CH}$	AOUT and BOUT current matching	I_O = 1.5 A	–2.5		2.5	%
PROTECTION CIRCUITS						
V_{UVLO}	VM UVLO lockout	VM falling, UVLO falling	4.15	4.25	4.35	V
		VM rising, UVLO rising	4.25	4.35	4.45	
$V_{UVLO,HYS}$	Undervoltage hysteresis	Rising to falling threshold		100		mV
V_{CPUV}	Charge pump undervoltage	VCP falling; CPUV report		V_{VM} + 2		V
I_{OCP}	Overcurrent protection	Current through any FET	2.4			A
t_{OCP}	Overcurrent deglitch time	VM < 37V		3		µs
		VM >= 37V		0.5		
t_{RETRY}	Overcurrent retry time			4		ms
T_{OTSD}	Thermal shutdown	Die temperature T_J	150	165	180	°C
T_{HYS_OTSD}	Thermal shutdown hysteresis	Die temperature T_J		20		°C

6.6 Typical Characteristics

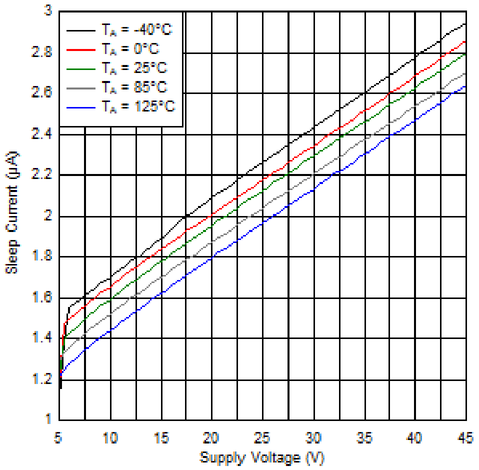


Figure 6-1. Sleep Current over VM

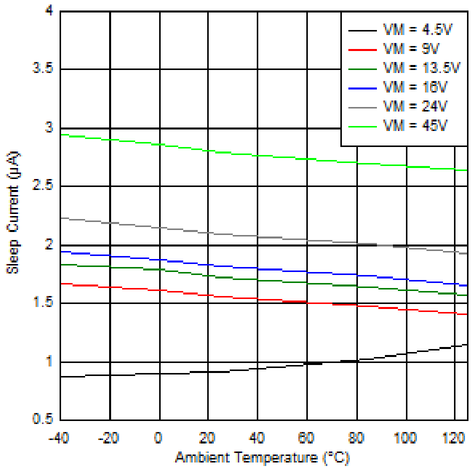


Figure 6-2. Sleep Current over Temperature

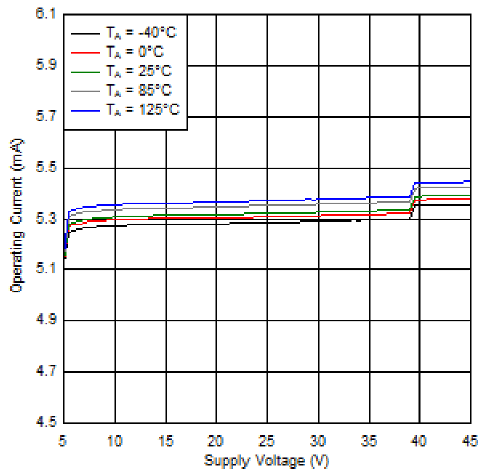


Figure 6-3. Operating Current over VM

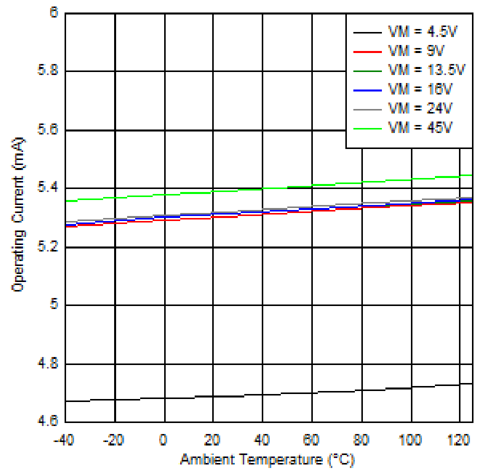


Figure 6-4. Operating Current over Temperature

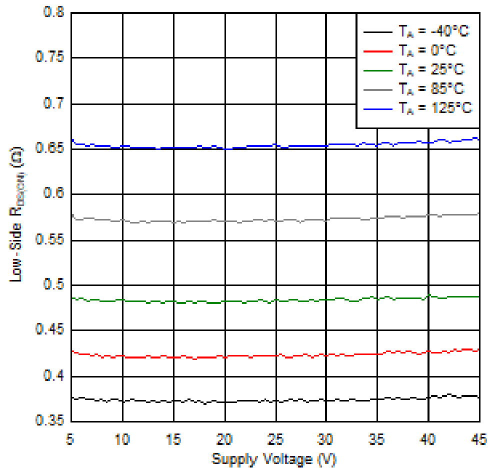


Figure 6-5. Low-Side $R_{DS(ON)}$ over VM

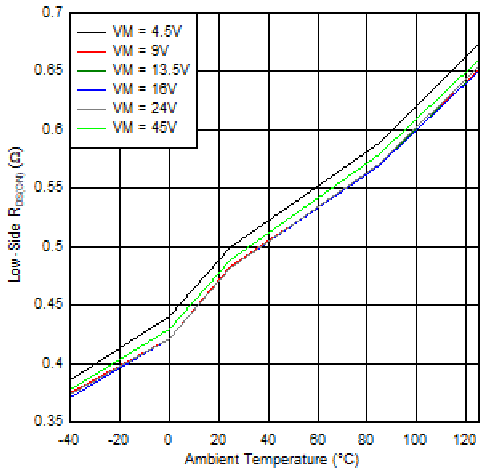


Figure 6-6. Low-Side $R_{DS(ON)}$ over Temperature

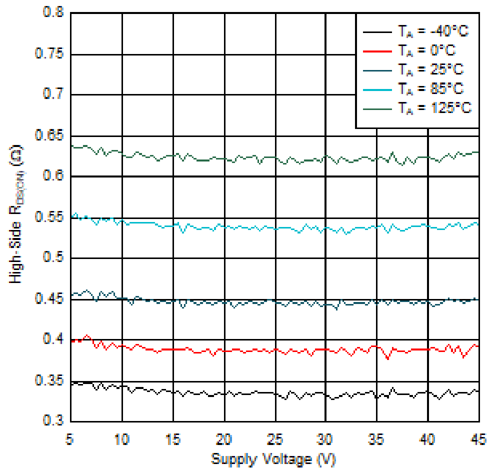


Figure 6-7. High-Side $R_{DS(ON)}$ over VM

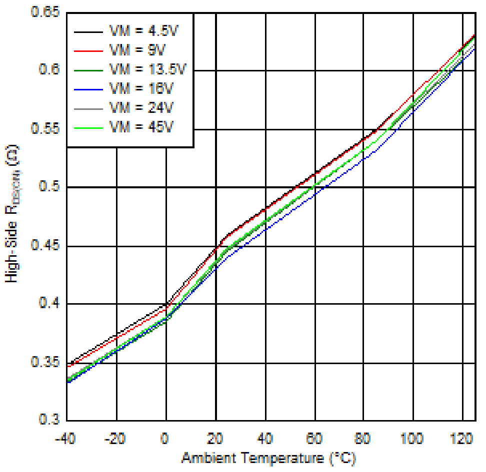


Figure 6-8. High-Side $R_{DS(ON)}$ over Temperature

7 Detailed Description

7.1 Overview

The DRV8436E/P are integrated motor driver solutions for bipolar stepper motors or dual brushed-DC motors. The devices integrate two N-channel power MOSFET H-bridges, integrated current sense and regulation circuitry. The DRV8436E/P can be powered with a supply voltage between 4.5 and 48 V. The devices are capable of providing an output current up to 2.4-A peak, 1.5-A full-scale, or 1.1-A root mean square (rms). The actual full-scale and rms current depends on the ambient temperature, supply voltage, and PCB thermal capability.

The DRV8436E/P devices use an integrated current-sense architecture which eliminates the need for two external power sense resistors. This architecture removes the power dissipated in the sense resistors by using a current mirror approach and using the internal power MOSFETs for current sensing. The current regulation set point is adjusted by the voltage at the VREFA and VREFB pins. These features reduce external component cost, board PCB size, and system power consumption.

A simple PH/**E**N (DRV8436**E**) or **P**WM (DRV8436**P**) interface allows easy interfacing to the controller circuit.

The current regulation is highly configurable, with several decay modes of operation. The decay mode can be selected as a smart tune Dynamic Decay, fixed slow, mixed, or fast decay. The smart tune decay mode automatically adjusts the decay setting to minimize current ripple while still reacting quickly to step changes. This feature greatly simplifies stepper driver integration into a motor drive system. The PWM off-time, t_{OFF}, can be adjusted to 7, 16, 24, or 32 μs.

A low-power sleep mode is included which allows the system to save power when not driving the motor.

7.2 Functional Block Diagrams

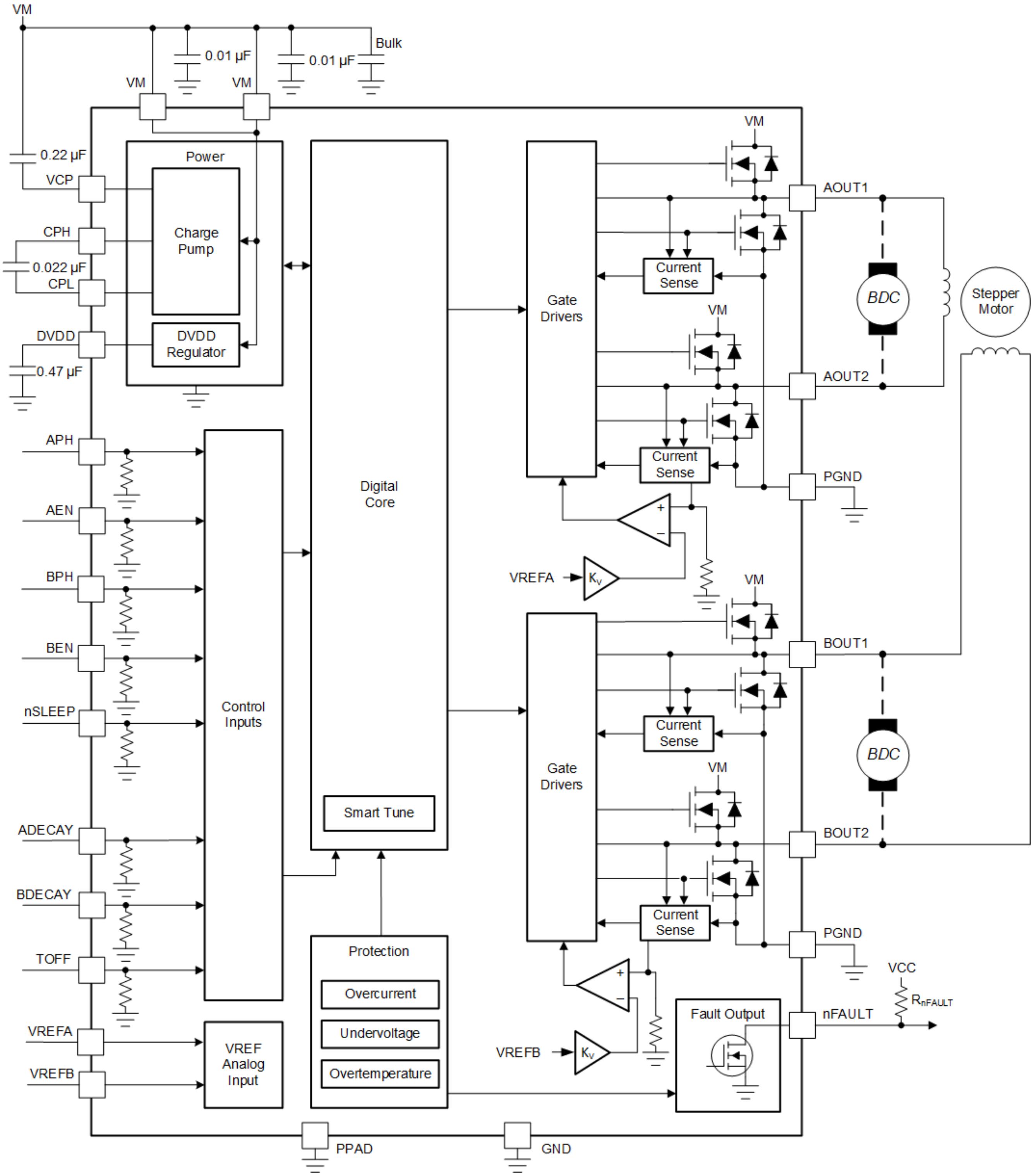


Figure 7-1. DRV8436E Block Diagram

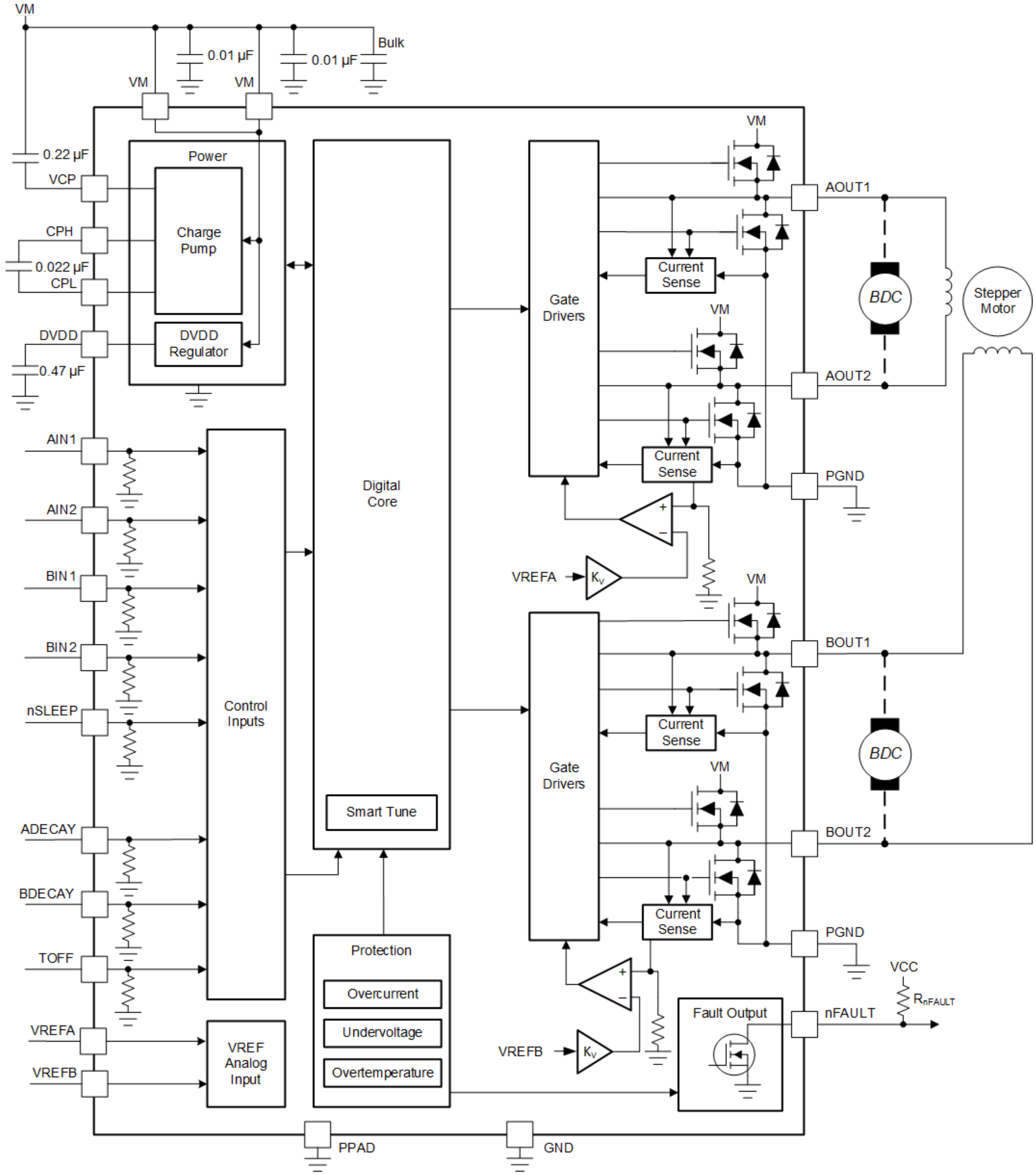


Figure 7-2. DRV8436P Block Diagram

7.3 Feature Description

Table 7-1 shows the recommended values of the external components for the gate driver.

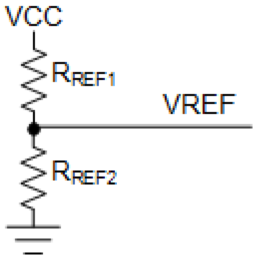


Figure 7-3. Resistor divider connected to the VREF pins

Table 7-1. External Components

COMPONENT	PIN 1	PIN 2	RECOMMENDED
C_{VM1}	VM	GND	Two X7R, 0.01-µF, VM-rated ceramic capacitors
C_{VM2}	VM	GND	Bulk, VM-rated capacitor
C_{VCP}	VCP	VM	X7R, 0.22-µF, 16-V ceramic capacitor
C_{SW}	CPH	CPL	X7R, 0.022-µF, VM-rated ceramic capacitor
C_{DVDD}	DVDD	GND	X7R, 0.47-µF to 1-µF, 6.3-V or 10-V rated ceramic capacitor
R_{nFAULT}	VCC	nFAULT	>4.7-kΩ resistor
R_{REF1}	VREFx	VCC	Resistor to limit chopping current. It is recommended that the value of parallel combination of R_{REF1} and R_{REF2} should be less than 50-kΩ.
R_{REF2} (Optional)	VREFx	GND	

7.3.1 PWM Motor Drivers

The DRV8436E/P contain drivers for two full H-bridges. Figure 7-4 shows a block diagram of the circuitry.

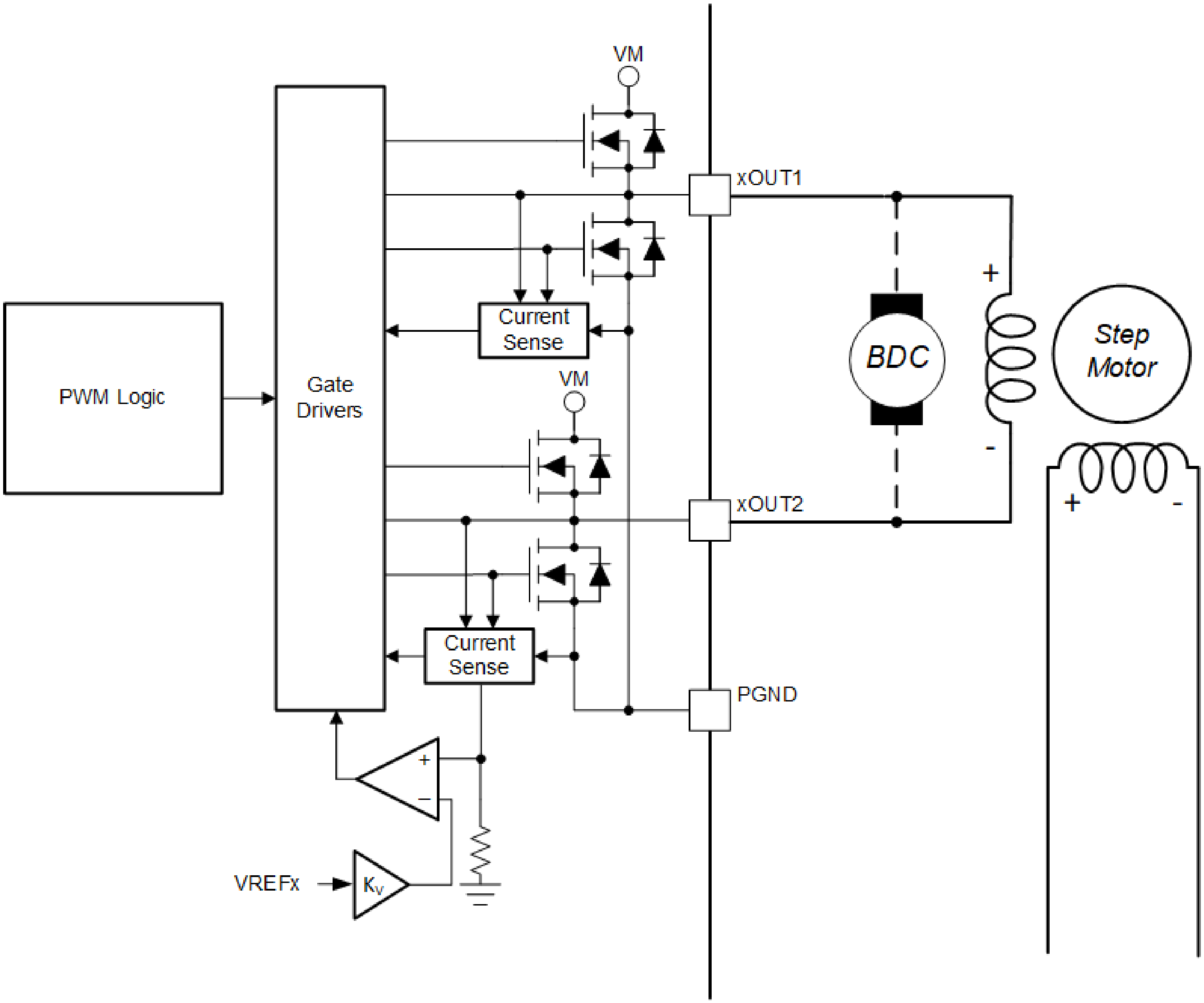


Figure 7-4. PWM Motor Driver Block Diagram

7.3.2 Bridge Control

The DRV8436E is controlled using a PH/EN interface. Table 7-2 gives the full H-bridge state. Note that this table does not take into account the current control built into the DRV8436E. Positive current is defined in the direction of xOUT1 to xOUT2.

Table 7-2. DRV8436E (PH/EN) Control Interface

nSLEEP	ENx	PHx	xOUT1	xOUT2	DESCRIPTION
0	X	X	Hi-Z	Hi-Z	Sleep mode; H-bridge disabled Hi-Z
1	0	X	Hi-Z	Hi-Z	H-bridge disabled Hi-Z
1	1	0	L	H	Reverse (current xOUT2 to xOUT1)
1	1	1	H	L	Forward (current xOUT1 to xOUT2)

The DRV8436P is controlled using a PWM interface. Table 7-3 gives the full H-bridge state. Note that this table does not take into account the current control built into the DRV8436P. Positive current is defined in the direction of xOUT1 to xOUT2.

Table 7-3. DRV8436P (PWM) Control Interface

nSLEEP	xIN1	xIN2	xOUT1	xOUT2	DESCRIPTION
0	X	X	Hi-Z	Hi-Z	Sleep mode; H-bridge disabled Hi-Z
1	0	0	Hi-Z	Hi-Z	Coast; H-bridge disabled Hi-Z
1	0	1	L	H	Reverse (current xOUT2 to xOUT1)
1	1	0	H	L	Forward (current xOUT1 to xOUT2)
1	1	1	L	L	Brake; low-side slow decay

7.3.3 Current Regulation

The current through the motor windings is regulated by an adjustable, off-time PWM current-regulation circuit. When an H-bridge is enabled, current rises through the winding at a rate dependent on the DC voltage, inductance of the winding, and the magnitude of the back EMF present. When the current hits the current regulation threshold, the bridge enters a decay mode for a period of time determined by the TOFF pin setting to decrease the current. After the off-time expires, the bridge is re-enabled, starting another PWM cycle.

Table 7-4. Off-Time Settings

TOFF	OFF-TIME t_{OFF}
0	7 µs
1	16 µs
Hi-Z	24 µs
330kΩ to GND	32 µs

The PWM chopping current is set by a comparator which monitors the voltage across the current sense MOSFETs in parallel with the low-side power MOSFETs. To generate the reference voltage for the current chopping comparator, the VREFx input is attenuated by a factor of Kv.

The chopping current (I_{FS}) can be calculated as I_{FS} (A) = V_{REFx} (V) / K_V (V/A) = V_{REFx} (V) / 2.2 (V/A).

7.3.4 Decay Modes

During PWM current chopping, the H-bridge is enabled to drive through the motor winding until the PWM current chopping threshold is reached. This is shown in Figure 7-5, Item 1.

Once the chopping current threshold is reached, the H-bridge can operate in two different states, fast decay or slow decay. In fast decay mode, once the PWM chopping current level has been reached, the H-bridge reverses state to allow winding current to flow in a reverse direction. Fast decay mode is shown in Figure 7-5, item 2. In slow decay mode, winding current is re-circulated by enabling both of the low-side FETs in the bridge. This is shown in Figure 7-5, Item 3.

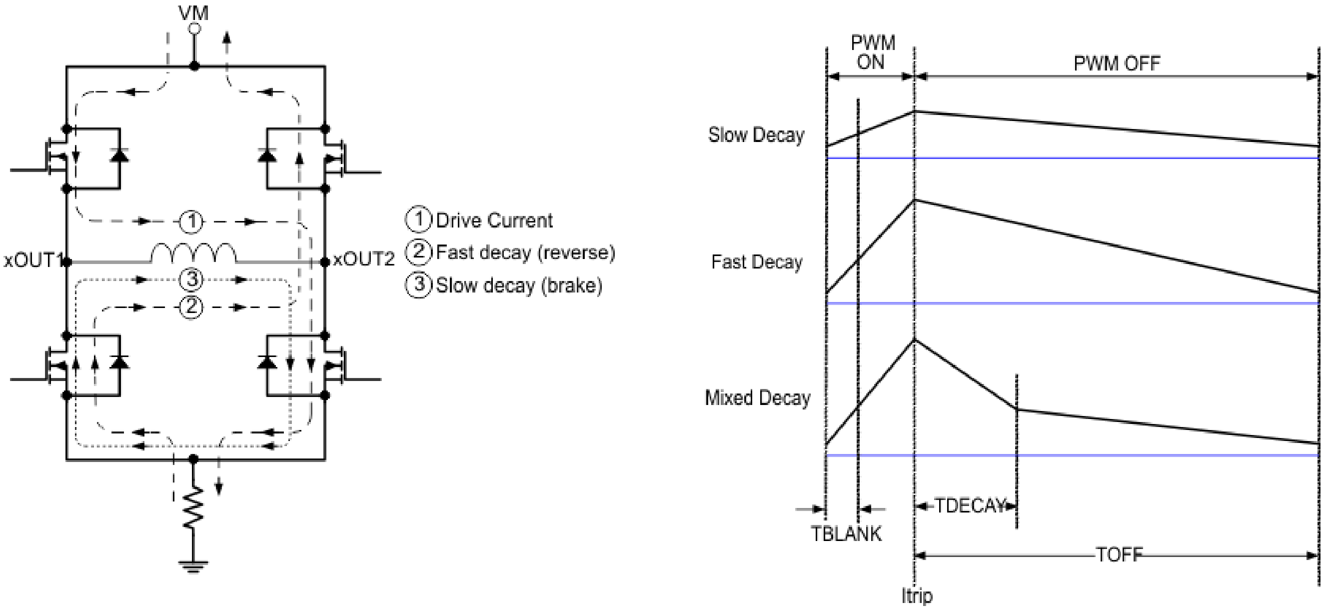


Figure 7-5. Decay Modes

The decay mode is selected by setting the quad-level ADECAY and BDECAY pins as shown in Table 7-5.

Table 7-5. Decay Mode Settings

xDECAY	DECAY MODE
0	Smart tune Dynamic Decay
330k to GND	Slow decay
Hi-Z	Mixed decay: 30% fast
1	Fast decay

The ADECAY pin sets the decay mode for H-bridge A (AOUT1, AOUT2), and the BDECAY pin sets the decay mode for H-bridge B (BOUT1, BOUT2).

7.3.4.1 Slow Decay

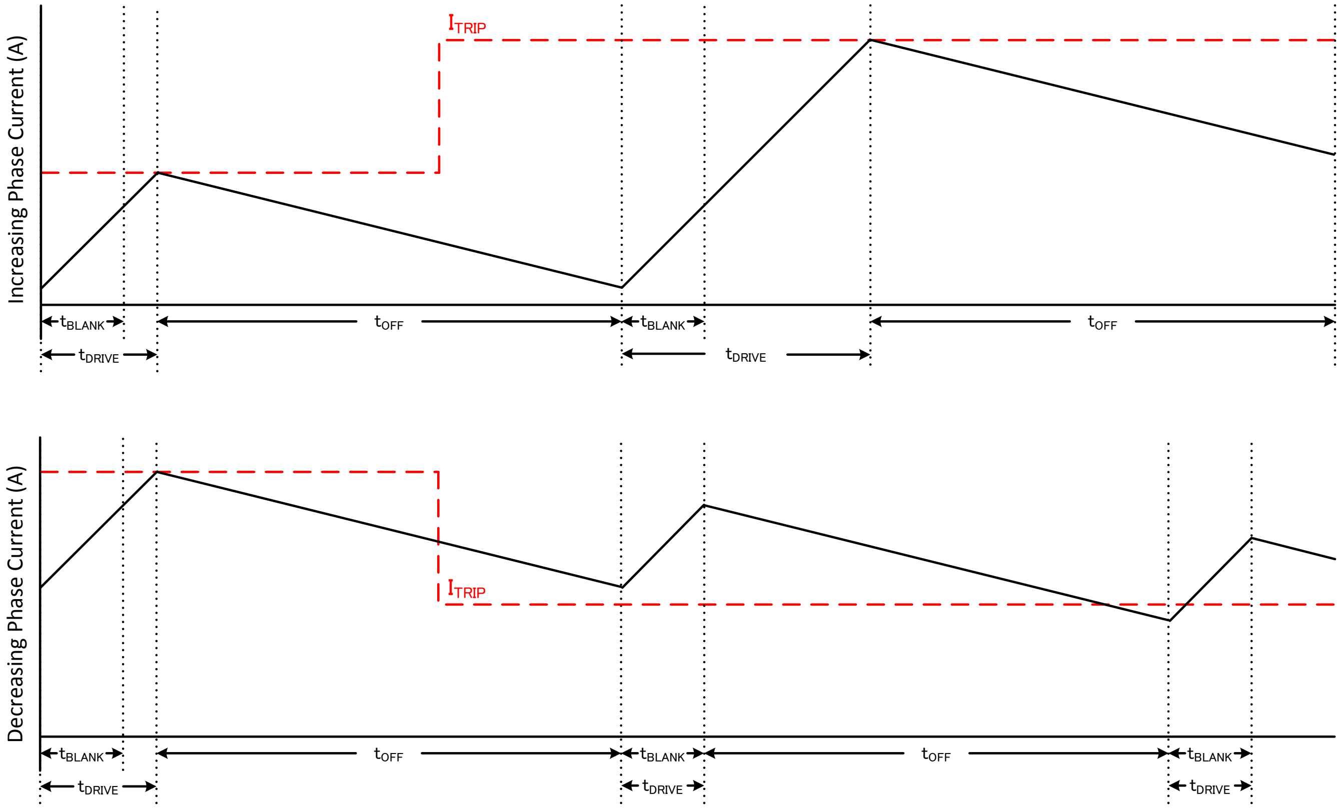


Figure 7-6. Slow Decay Mode

During slow decay, both of the low-side FETs of the H-bridge are turned on, allowing the current to be recirculated.

Slow decay exhibits the least current ripple of the decay modes for a given t_{OFF}. However on decreasing current steps, slow decay will take a long time to settle to the new ITRIP level because the current decreases very slowly. If the current at the end of the off time is above the ITRIP level, slow decay will be extended for another off time duration and so on, till the current at the end of the off time is below ITRIP level.

In cases where current is held for a long time, slow decay may not properly regulate current because no back-EMF is present across the motor windings. In this state, motor current can rise very quickly, and may require a large off-time. In some cases this may cause a loss of current regulation, and a more aggressive decay mode is recommended.

7.3.4.2 Mixed Decay

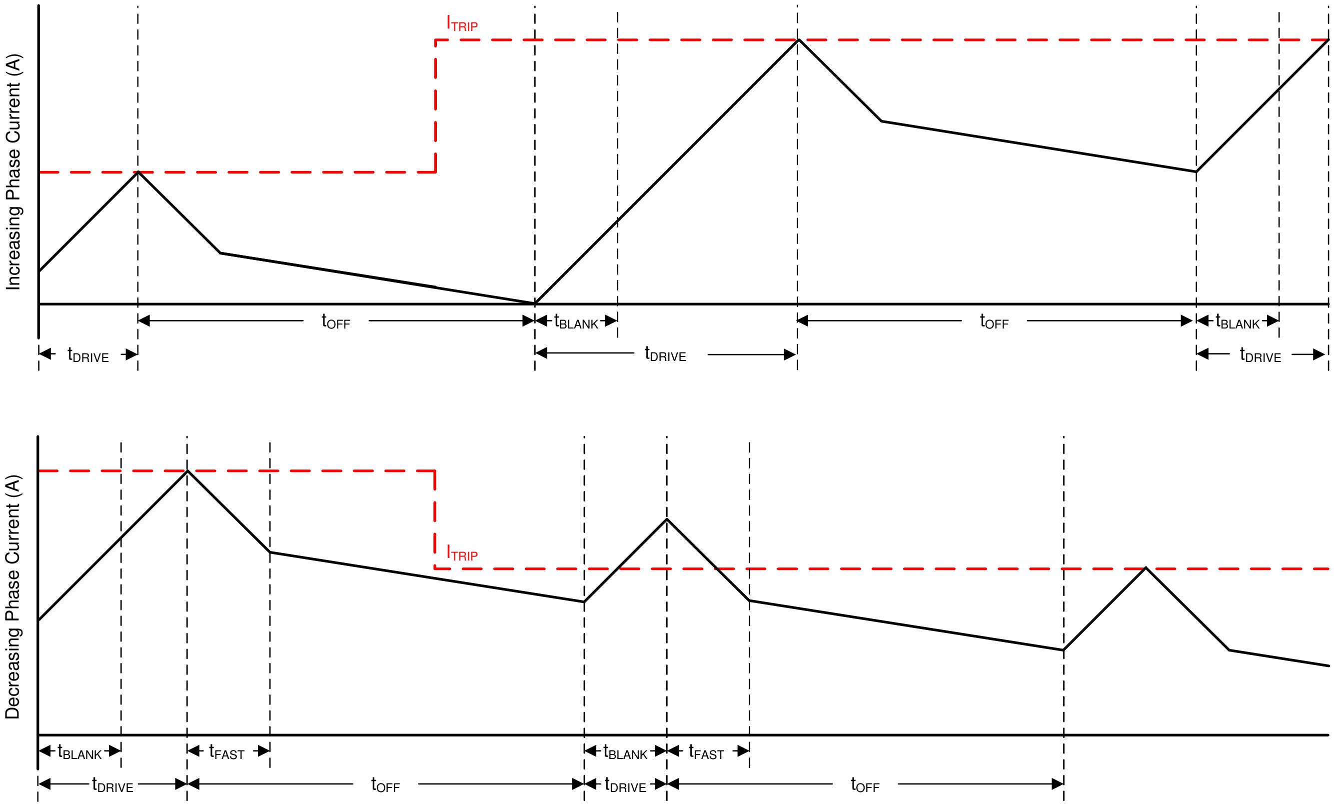


Figure 7-7. Mixed Decay Mode

Mixed decay begins as fast decay for 30% of t_{OFF}, followed by slow decay for the remainder of t_{OFF}.

This mode exhibits ripple larger than slow decay, but smaller than fast decay. On decreasing current steps, mixed decay settles to the new I_{TRIP} level faster than slow decay.

7.3.4.3 Fast Decay

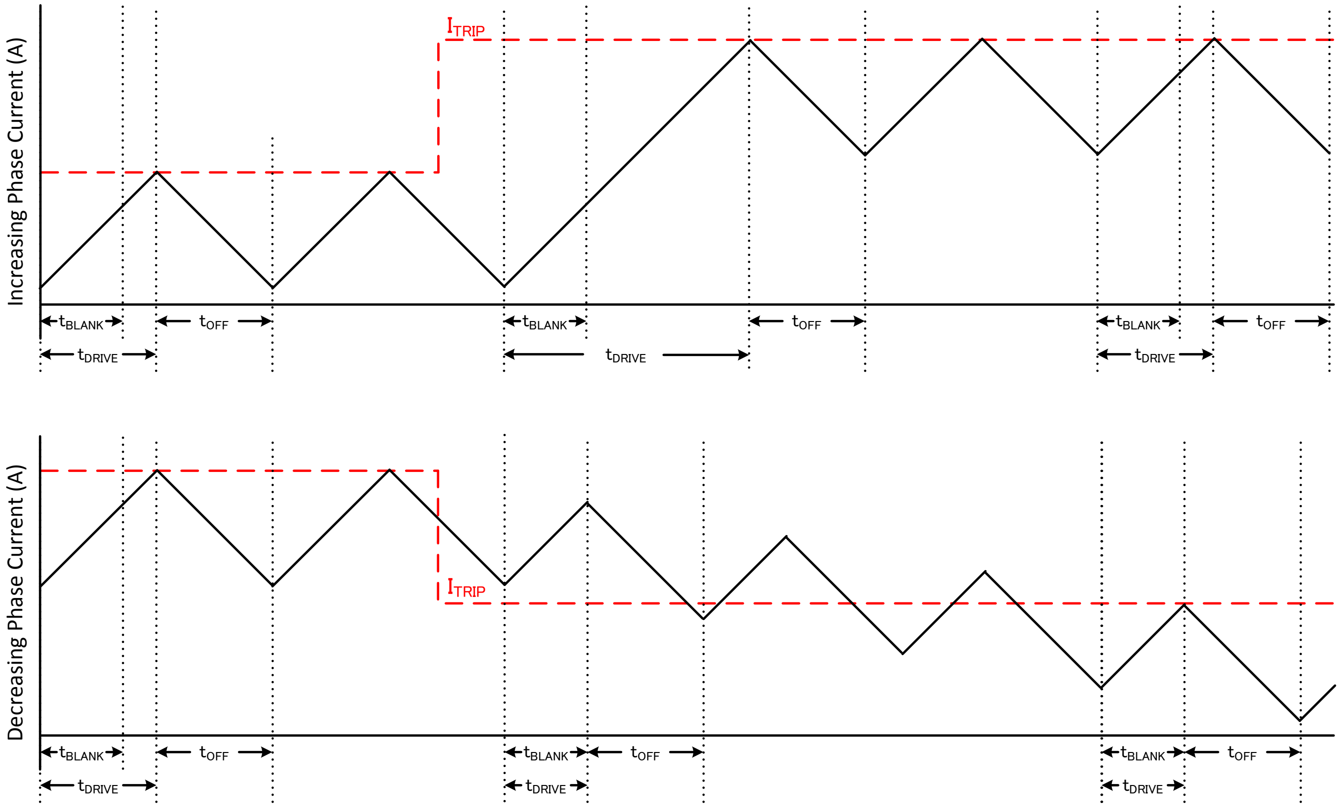


Figure 7-8. Fast/Fast Decay Mode

During fast decay, the polarity of the H-bridge is reversed. The H-bridge will be turned off as current approaches zero in order to prevent current flow in the reverse direction.

Fast decay exhibits the highest current ripple of the decay modes for a given t_{OFF}. Transition time on decreasing current steps is much faster than slow decay since the current is allowed to decrease much faster.

7.3.4.4 Smart tune Dynamic Decay

The smart tune current regulation scheme is an advanced current-regulation control method compared to traditional fixed off-time current regulation schemes. Smart tune current regulation scheme helps the stepper motor driver adjust the decay scheme based on operating factors such as the ones listed as follows:

- Motor winding resistance and inductance
- Motor aging effects
- Motor dynamic speed and load
- Motor supply voltage variation
- Low-current versus high-current dI/dt

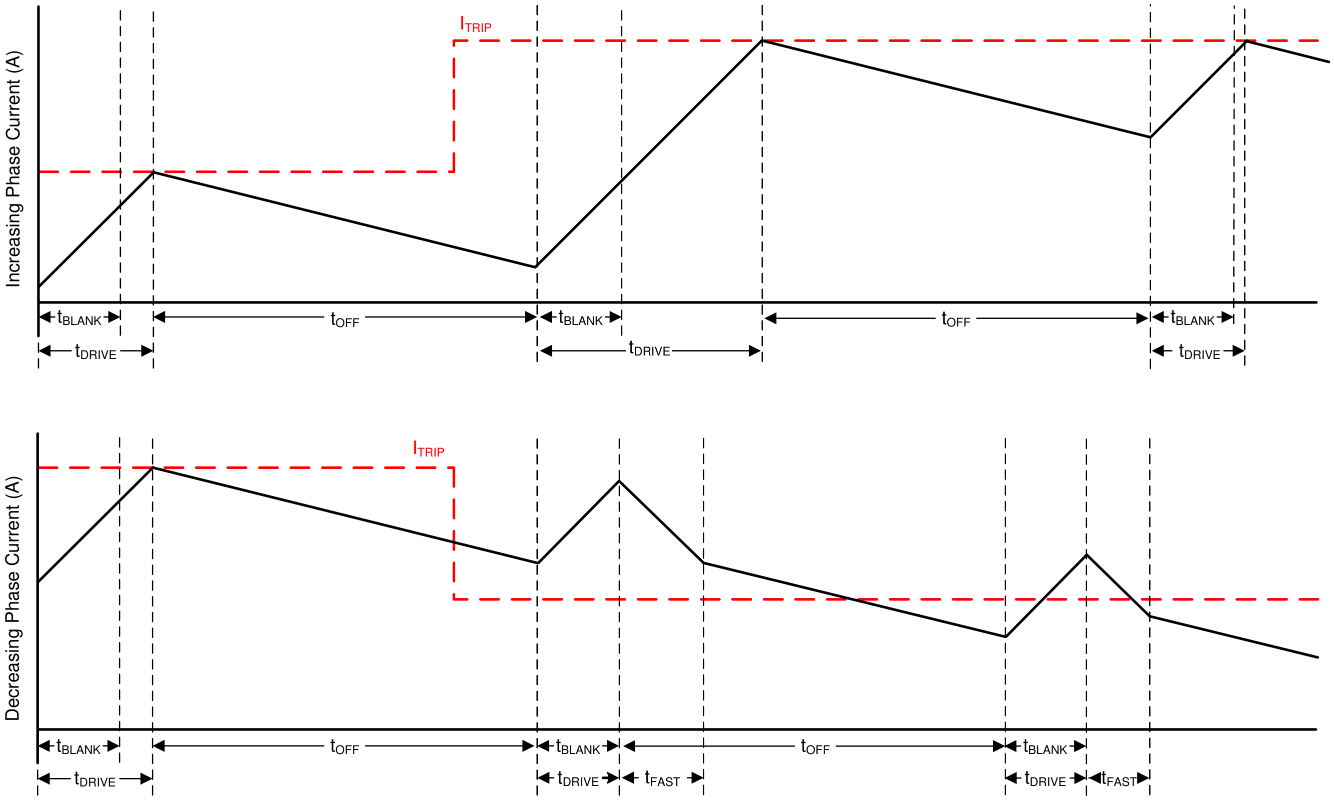


Figure 7-9. Smart tune Dynamic Decay Mode

Smart tune Dynamic Decay greatly simplifies the decay mode selection by automatically configuring the decay mode between slow, mixed, and fast decay. In mixed decay, smart tune dynamically adjusts the fast decay percentage of the total mixed decay time. This feature eliminates motor tuning by automatically determining the best decay setting that results in the lowest ripple for the motor.

The decay mode setting is optimized iteratively each PWM cycle. If the motor current overshoots the target trip level, then the decay mode becomes more aggressive (add fast decay percentage) on the next cycle to prevent regulation loss. If a long drive time must occur to reach the target trip level, the decay mode becomes less aggressive (remove fast decay percentage) on the next cycle to operate with less ripple and more efficiently. On falling steps, smart tune Dynamic Decay automatically switches to fast decay to reach the next step quickly.

Smart tune Dynamic Decay is optimal for applications that require minimal current ripple but want to maintain a fixed frequency in the current regulation scheme.

7.3.4.5 Blanking time

After the current is enabled (start of drive phase) in an H-bridge, the current sense comparator is ignored for a period of time (t_{BLANK}) before enabling the current-sense circuitry. The blanking time also sets the minimum drive time of the PWM. The blanking time is approximately 860ns.

7.3.5 Charge Pump

A charge pump is integrated to supply a high-side N-channel MOSFET gate-drive voltage. The charge pump requires a capacitor between the VM and VCP pins to act as the storage capacitor. Additionally a ceramic capacitor is required between the CPH and CPL pins to act as the flying capacitor.

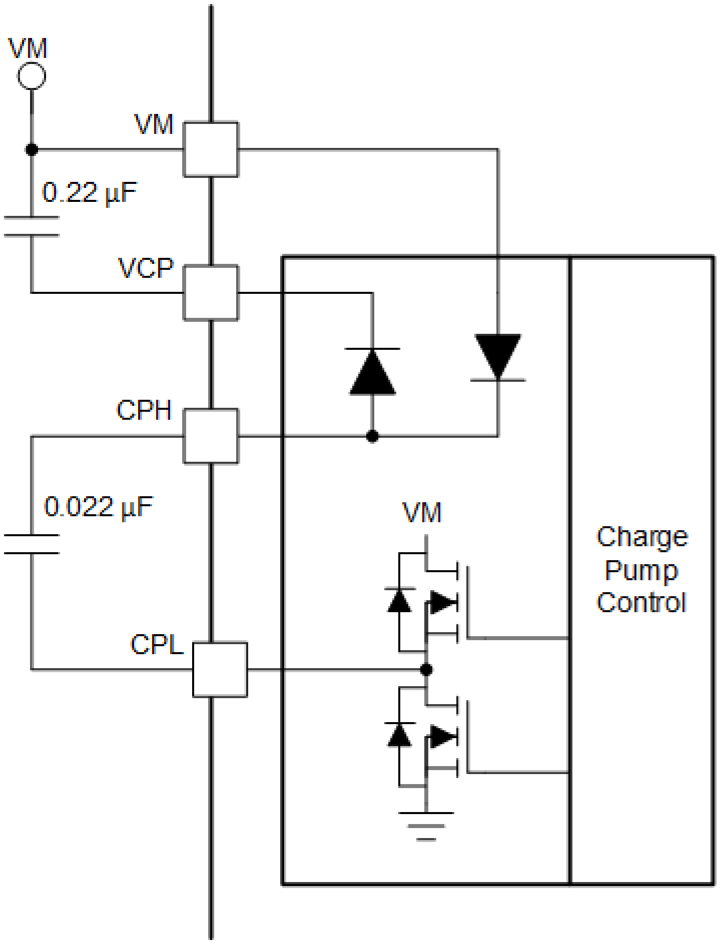


Figure 7-10. Charge Pump Block Diagram

7.3.6 Linear Voltage Regulators

A linear voltage regulator is integrated in the device. The DVDD regulator can be used to provide a reference voltage. DVDD can supply a maximum of 2 mA load. For proper operation, bypass the DVDD pin to GND using a ceramic capacitor.

The DVDD output is nominally 5-V. When the DVDD LDO current load exceeds 2 mA, the output voltage drops significantly.

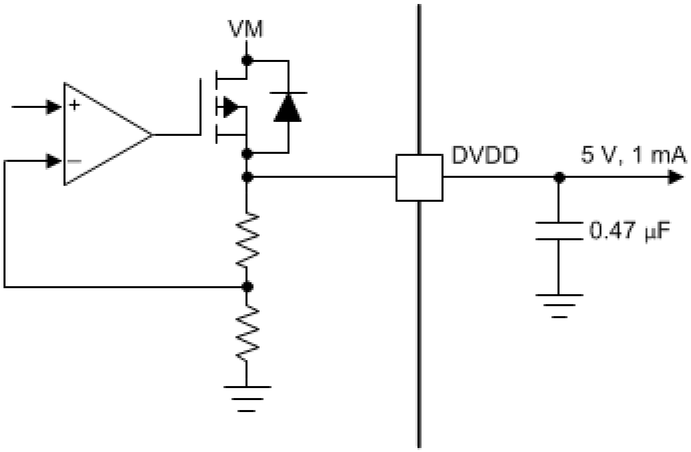


Figure 7-11. Linear Voltage Regulator Block Diagram

If a digital input must be tied permanently high (that is, ADECAY, BDECAY or TOFF), tying the input to the DVDD pin instead of an external regulator is preferred. This method saves power when the VM pin is not applied or in sleep mode: the DVDD regulator is disabled and current does not flow through the input pulldown resistors. For reference, logic level inputs have a typical pulldown of 200 kΩ.

The nSLEEP pin cannot be tied to DVDD, else the device will never exit sleep mode.

7.3.7 Logic and Quad-Level Pin Diagrams

Figure 7-12 gives the input structure for logic-level pins APH, AEN, BPH, BEN, AIN1, AIN2, BIN1, BIN2 and nSLEEP:

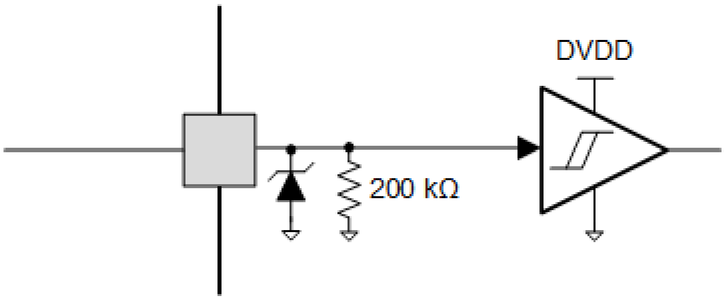


Figure 7-12. Logic-level Input Pin Diagram

Quad-level logic pins TOFF, ADECAY, and BDECAY have the following structure as shown in Figure 7-13.

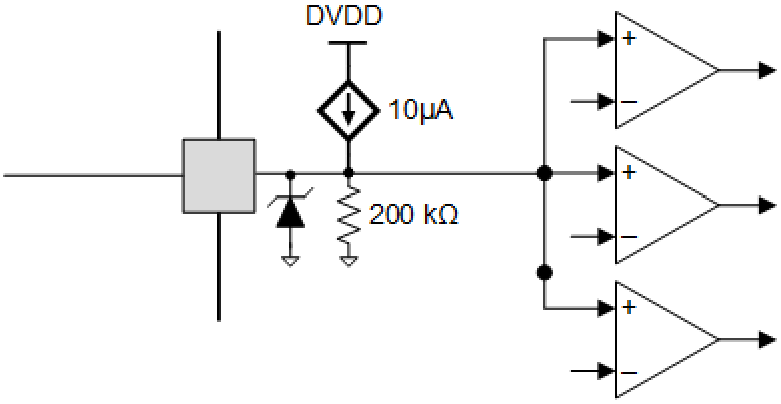


Figure 7-13. Quad-Level Input Pin Diagram

7.3.7.1 nFAULT Pin

The nFAULT pin has an open-drain output and should be pulled up to a 5-V or 3.3-V supply. When a fault is detected, the nFAULT pin will be logic low. nFAULT pin will be high after power-up. For a 5-V pullup, the nFAULT pin can be tied to the DVDD pin with a resistor. For a 3.3-V pullup, an external 3.3-V supply must be used.

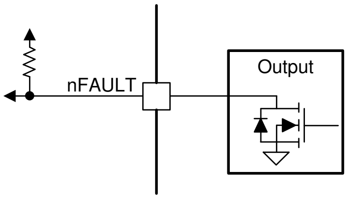


Figure 7-14. nFAULT Pin

7.3.8 Protection Circuits

The devices are fully protected against supply undervoltage, charge pump undervoltage, output overcurrent, and device overtemperature events.

7.3.8.1 VM Undervoltage Lockout (UVLO)

If at any time the voltage on the VM pin falls below the UVLO-threshold voltage for the voltage supply, all the outputs are disabled, and the nFAULT pin is driven low. The charge pump is disabled in this condition.

Normal operation resumes (motor-driver operation and nFAULT released) when the VM undervoltage condition is removed.

7.3.8.2 VCP Undervoltage Lockout (CPUV)

If at any time the voltage on the VCP pin falls below the CPUV voltage, all the outputs are disabled, and the nFAULT pin is driven low. The charge pump remains active during this condition. Normal operation resumes (motor-driver operation and nFAULT released) when the VCP undervoltage condition is removed.

7.3.8.3 Overcurrent Protection (OCP)

An analog current-limit circuit on each FET limits the current through the FET by removing the gate drive. If this current limit persists for longer than the t_{OCP} time, the FETs in that particular H-bridge are disabled and the nFAULT pin is driven low. The charge pump remains active during this condition. Normal operation resumes automatically (motor-driver operation starts and nFAULT released) after the t_{RETRY} time has elapsed and the fault condition is removed.

7.3.8.4 Thermal Shutdown (OTSD)

If the die temperature exceeds the thermal shutdown limit (T_{OTSD}) all MOSFETs in the H-bridge are disabled, and the nFAULT pin is driven low. The charge pump remains active during this condition. Normal operation resumes (motor-driver operation and the nFAULT line released) when the junction temperature falls below the overtemperature threshold limit minus the hysteresis ($T_{OTSD} – T_{HYS\_OTSD}$).

7.3.8.5

Table 7-6. Fault Condition Summary

FAULT	CONDITION	ERROR REPORT	H-BRIDGE	CHARGE PUMP	INDEXER	LOGIC	RECOVERY
VM undervoltage (UVLO)	VM < V_{UVLO}	nFAULT	Disabled	Disabled	Disabled	Reset (V_{DVDD} < 3.9 V)	Automatic: VM > V_{UVLO}
VCP undervoltage (CPUV)	VCP < V_{CPUV}	nFAULT	Disabled	Operating	Operating	Operating	VCP > V_{CPUV}
Overcurrent (OCP)	I_{OUT} > I_{OCP}	nFAULT	Disabled	Operating	Operating	Operating	Automatic retry: t_{RETRY}
Thermal Shutdown (OTSD)	T_J > T_{TSD}	nFAULT	Disabled	Disabled	Operating	Operating	Automatic: T_J < T_{OTSD} - T_{HYS_OTSD}

7.4 Device Functional Modes

7.4.1 Sleep Mode (nSLEEP = 0)

The state of the device is managed by the nSLEEP pin. When the nSLEEP pin is low, the device enters a low-power sleep mode. In sleep mode, all the internal MOSFETs are disabled and the charge pump is disabled. The t_{SLEEP} time must elapse after a falling edge on the nSLEEP pin before the device enters sleep mode. The device is brought out of sleep automatically if the nSLEEP pin is brought high. The t_{WAKE} time must elapse before the device is ready for inputs.

7.4.2 Operating Mode (nSLEEP = 1)

When the nSLEEP pin is high, and VM > UVLO, the device enters the active mode. The t_{WAKE} time must elapse before the device is ready for inputs.

7.4.3 Functional Modes Summary

Table 7-7 lists a summary of the functional modes.

Table 7-7. Functional Modes Summary

CONDITION		CONFIGURATION	H-BRIDGE	DVDD Regulator	CHARGE PUMP	Logic
Sleep mode	4.5 V < VM < 48 V	nSLEEP pin = 0	Disabled	Disbaled	Disabled	Disabled

Table 7-7. Functional Modes Summary (continued)

CONDITION		CONFIGURATION	H-BRIDGE	DVDD Regulator	CHARGE PUMP	Logic
Operating	4.5 V < VM < 48 V	nSLEEP pin = 1	Operating	Operating	Operating	Operating

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DRV8436E/P is used in stepper or brushed motor control.

8.2 Primary Application

In this application, the device is configured to drive bidirectional currents through two external loads (such as two brushed DC motors) using H-bridge configuration. The H-bridge polarity and duty cycle are controlled from the external controller to the xEN/xIN1 and xPH/xIN2 pins.

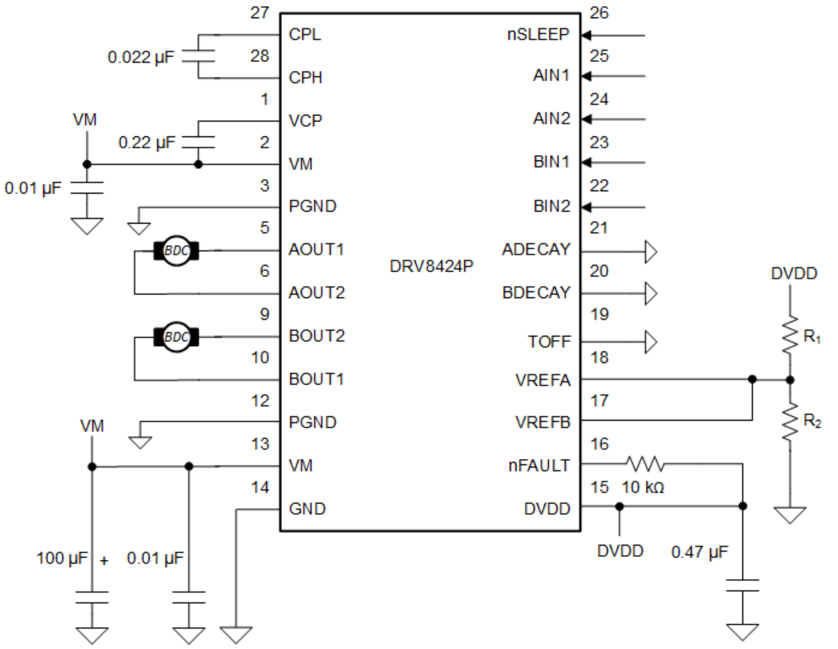


Figure 8-1. Primary Application Schematic

8.2.1 Design Requirements

Table 8-1 gives design input parameters for system design.

Table 8-1. Design Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Supply voltage	VM	24 V
Motor winding resistance	R_L	6 Ω
Motor winding inductance	L_L	4.1 mH
f_{PWM}	Switching frequency	20 kHz
Target maximum motor current	I_{TRIP}	1 A

8.2.2 Detailed Design Procedure

8.2.2.1 Current Regulation

The maximum current (I_{TRIP}) is set by the VREFx analog voltage. When starting a brushed-DC motor, a large inrush current may occur because there is no back-EMF. Current regulation will act to limit this inrush current and prevent high current on startup.

8.3 Typical Application

The following design procedure can be used to configure the DRV8436E/P. In this application, the device will be used to drive a stepper motor.

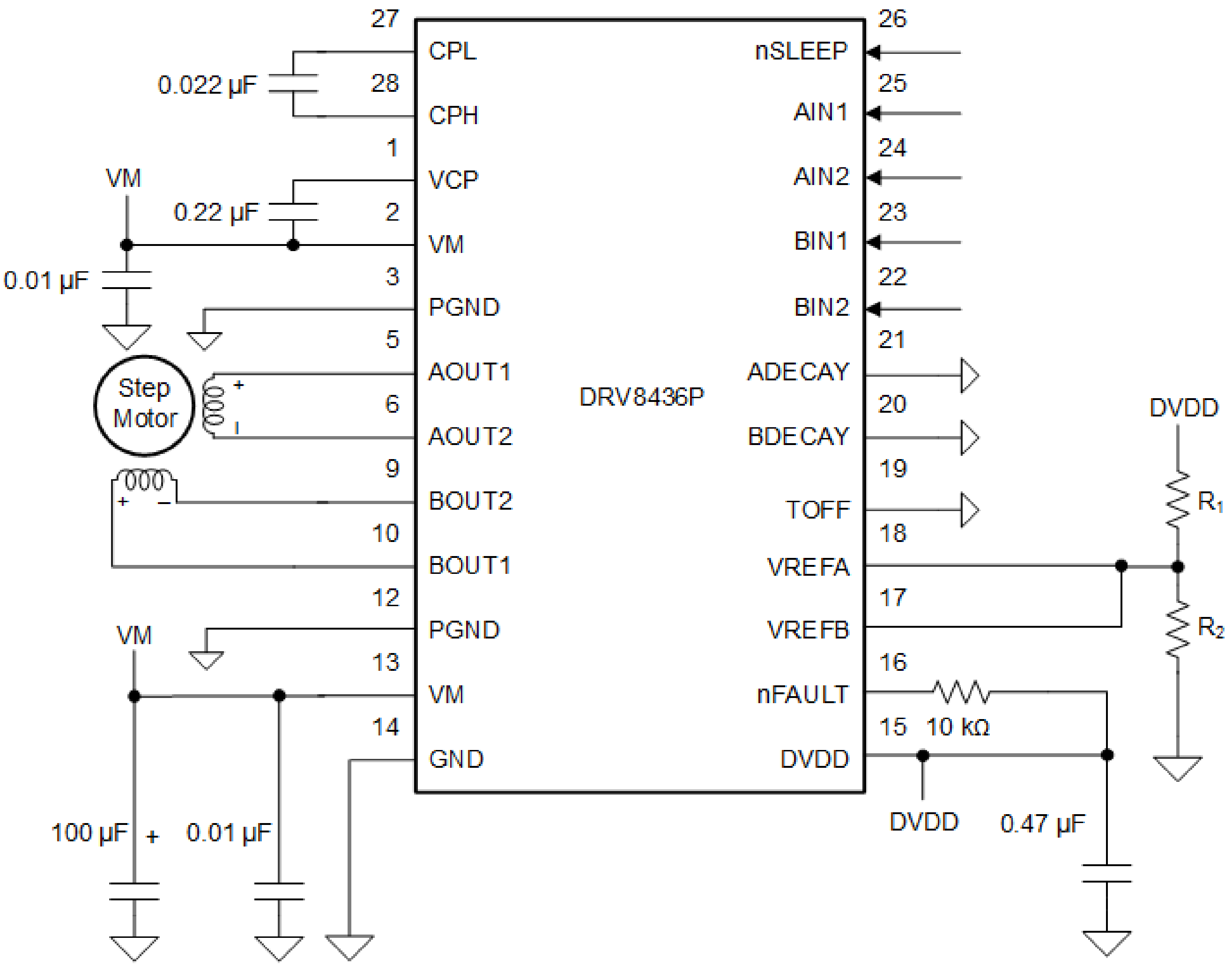


Figure 8-2. Typical Application Schematic

8.3.1 Design Requirements

Table 8-2 lists the design input parameters for system design.

Table 8-2. Design Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Supply voltage	VM	24 V
Motor winding resistance	R_L	0.93 Ω/phase
Motor winding inductance	L_L	1.9 mH/phase
Motor full step angle	$θ_{step}$	1.8°/step
Target microstepping level	n_m	Non-circular 1/2 step
Target motor speed	v	120 rpm
Target full-scale current	I_{FS}	2 A

8.3.2 Detailed Design Procedure

8.3.2.1 Current Regulation

In a stepper motor, the full-scale current (I_{FS}) is the maximum current driven through either winding. This quantity depends on the VREFx voltage. The maximum allowable voltage on the VREFx pins is 3.3 V. DVDD can be used to provide VREFx through a resistor divider.

I_{FS} (A) = V_{REF} (V) / 2.2 (V/A)

Note

The I_{FS} current must also follow the equation shown below to avoid saturating the motor. VM is the motor supply voltage, and R_L is the motor winding resistance.

$$I_{FS}\ (A) < \frac{VM\ (V)}{R_L\ (\Omega) + 2 \times R_{DS(ON)}\ (\Omega)} \quad (1)$$

8.3.2.2 Stepper Motor Speed

Next, the driving waveform needs to be planned. In order to command the correct speed, determine the frequency of the input waveform.

If the target motor speed is too high, the motor will not spin. Make sure that the motor can support the target speed.

For a desired motor speed (v), microstepping level (n_m), and motor full step angle (θ_{step}),

$$f_{step}\ (steps / s) = \frac{v\ (rpm) \times 360\ (^\circ / rot)}{\theta_{step}\ (^\circ / step) \times n_m\ (steps / microstep) \times 60\ (s / min)} \quad (2)$$

θ_{step} can be found in the stepper motor data sheet or written on the motor itself.

The frequency f_{step} gives the frequency of input change on the device. For the design parameters mentioned above, f_{step} can be calculated as 800 Hz.

$$f_{step}\ (steps / s) = \frac{120\ rpm \times 360^\circ / rot}{1.8^\circ / step \times 1/2\ steps / microstep \times 60\ s / min} = 800\,Hz \quad (3)$$

8.3.2.3 Decay Modes

The device supports several different decay modes: slow decay, fast decay, mixed decay, and smart tune. The current through the motor windings is regulated using an adjustable fixed-time-off scheme. This means that after any drive phase, when a motor winding current has hit the current chopping threshold (I_{TRIP}), the device will place the winding in one of the decay modes for TOFF. After TOFF, a new drive phase starts.

9 Power Supply Recommendations

The device is designed to operate from an input voltage supply (VM) range from 4.5 V to 48 V. A 0.01-µF ceramic capacitor rated for VM must be placed at each VM pin as close to the device as possible. In addition, a bulk capacitor must be included on VM.

9.1 Bulk Capacitance

Having appropriate local bulk capacitance is an important factor in motor drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the motor system
- The power supply's capacitance and ability to source current
- The amount of parasitic inductance between the power supply and motor system
- The acceptable voltage ripple
- The type of motor used (brushed DC, brushless DC, stepper)
- The motor braking method

The inductance between the power supply and motor drive system will limit the rate current can change from the power supply. If the local bulk capacitance is too small, the system will respond to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate sized bulk capacitor.

The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.

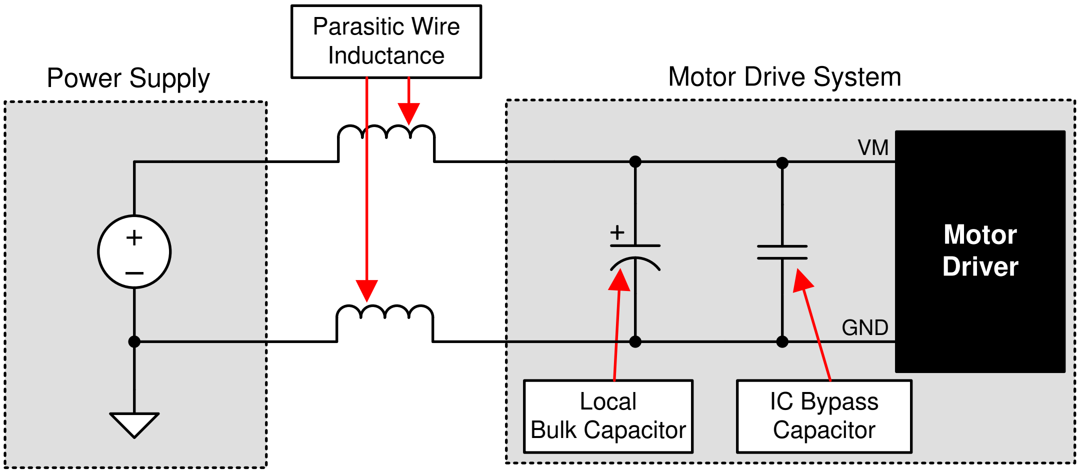


Figure 9-1. Example Setup of Motor Drive System With External Power Supply

10 Layout

10.1 Layout Guidelines

The VM pin should be bypassed to GND using a low-ESR ceramic bypass capacitor with a recommended value of 0.01 µF rated for VM. This capacitor should be placed as close to the VM pin as possible with a thick trace or ground plane connection to the device GND pin.

The VM pin must be bypassed to ground using a bulk capacitor rated for VM. This component can be an electrolytic capacitor.

A low-ESR ceramic capacitor must be placed in between the CPL and CPH pins. A value of 0.022 µF rated for VM is recommended. Place this component as close to the pins as possible.

A low-ESR ceramic capacitor must be placed in between the VM and VCP pins. A value of 0.22 µF rated for 16 V is recommended. Place this component as close to the pins as possible.

Bypass the DVDD pin to ground with a low-ESR ceramic capacitor. A value of 0.47 µF rated for 6.3 V is recommended. Place this bypassing capacitor as close to the pin as possible.

The thermal PAD must be connected to system ground.

10.2 Layout Example

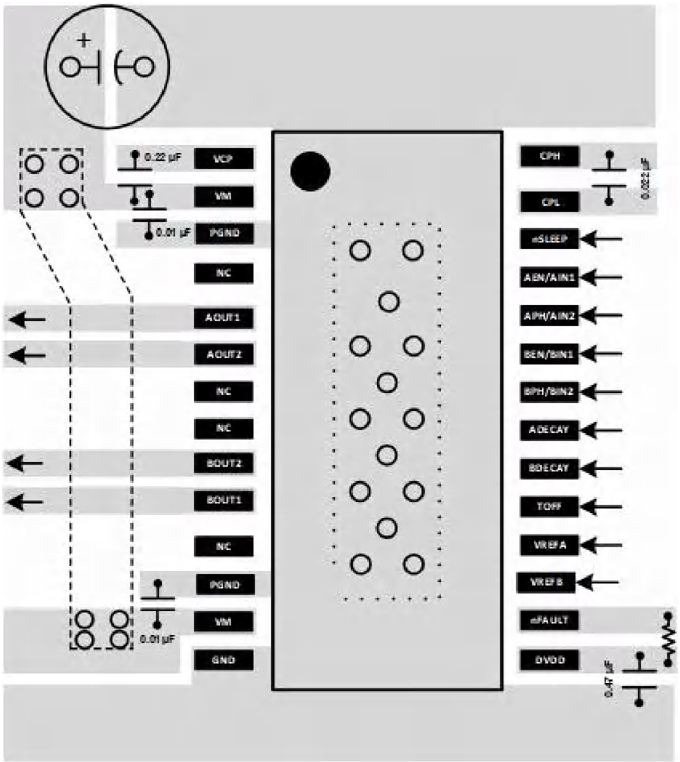


Figure 10-1. HTSSOP Layout Recommmendation

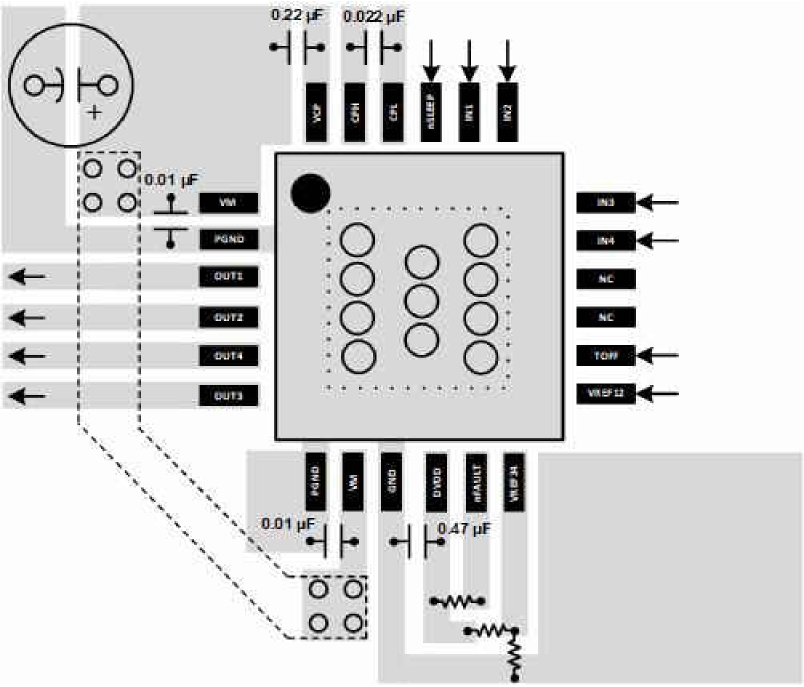


Figure 10-2. QFN Layout Recommendation

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *PowerPAD™ Thermally Enhanced Package* application report
- Texas Instruments, *PowerPAD™ Made Easy* application report
- Texas Instruments, *Current Recirculation and Decay Modes* application report
- Texas Instruments, *Calculating Motor Driver Power Dissipation* application report
- Texas Instruments, *Understanding Motor Driver Current Ratings* application report
- Texas Instruments, *High Resolution Microstepping Driver With the DRV88xx Series* application report

11.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Community Resources

11.5 Trademarks

All trademarks are the property of their respective owners.

12 Mechanical, Packaging, and Orderable Information

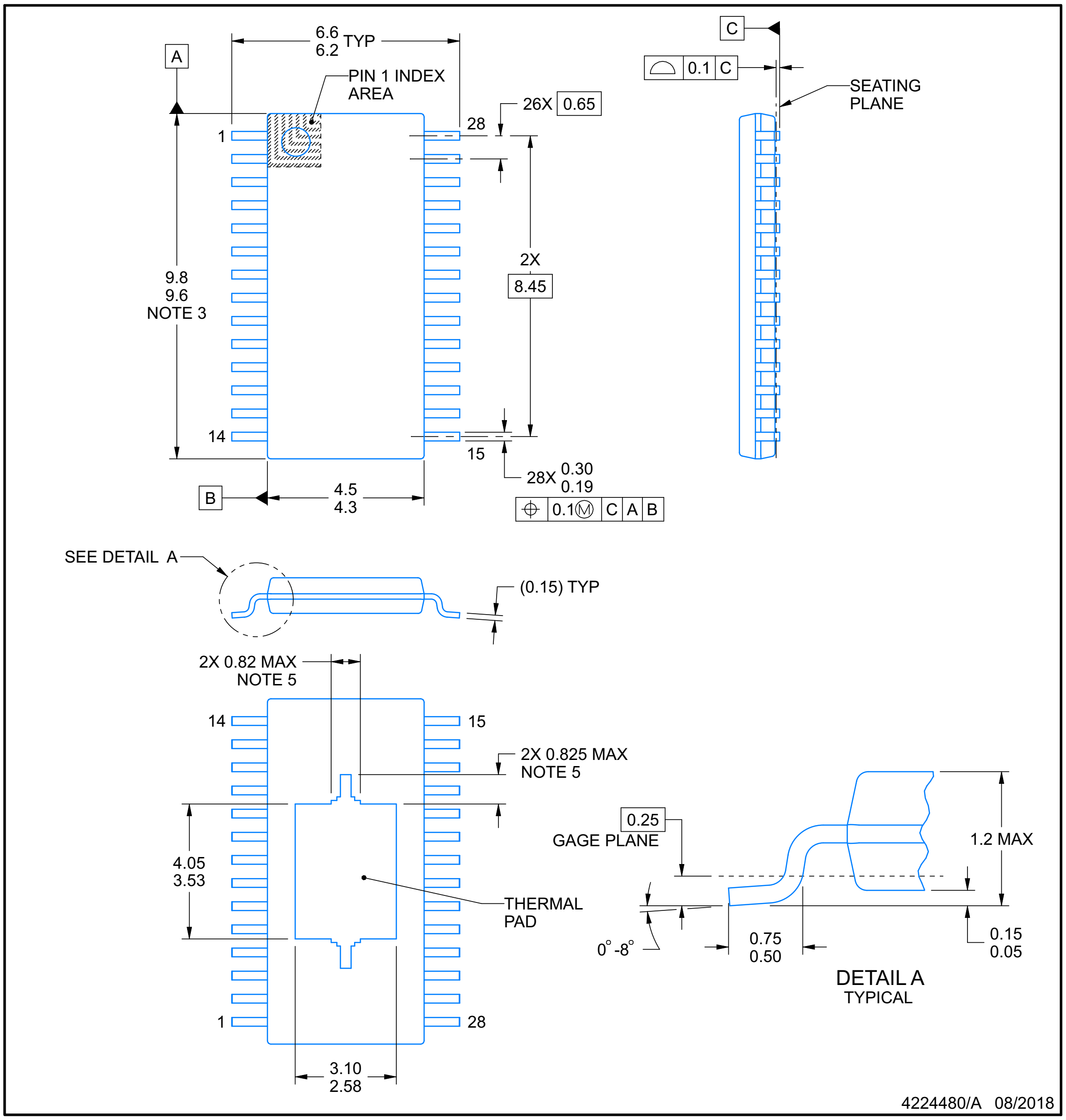
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

PWP0028M

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



PowerPAD is a trademark of Texas Instruments.

NOTES:

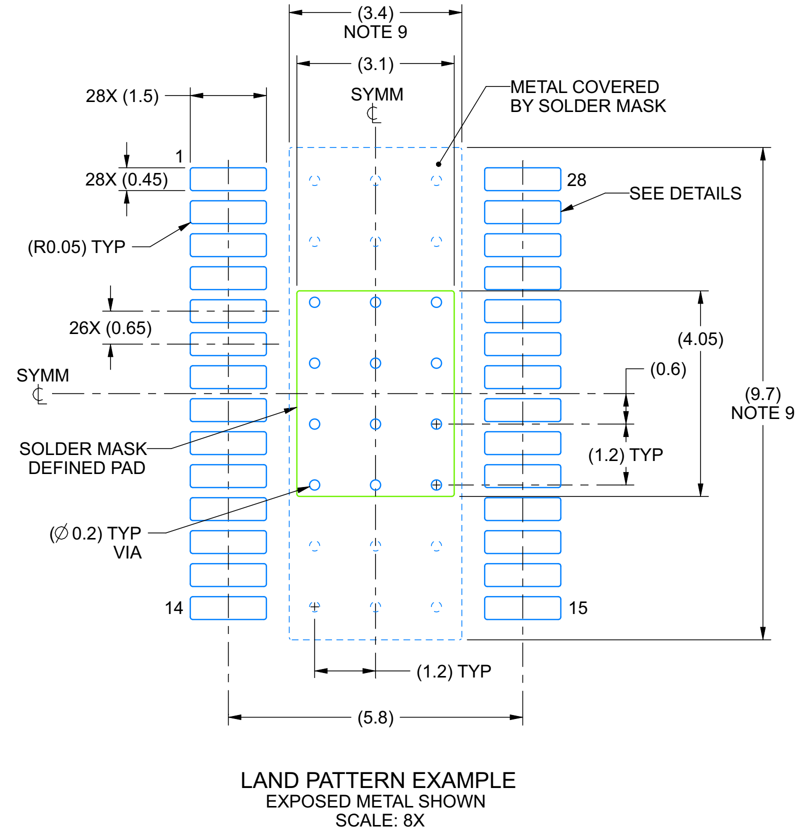
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.

TEXAS INSTRUMENTS
www.ti.com

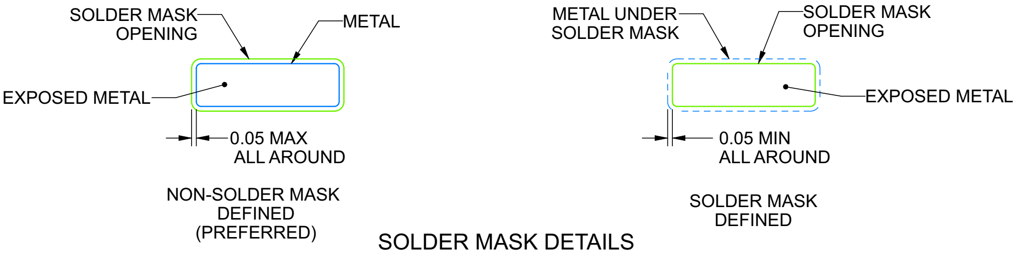
EXAMPLE BOARD LAYOUT

PWP0028M **PowerPAD™ TSSOP - 1.2 mm max height**

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X



SOLDER MASK DETAILS

4224480/A 08/2018

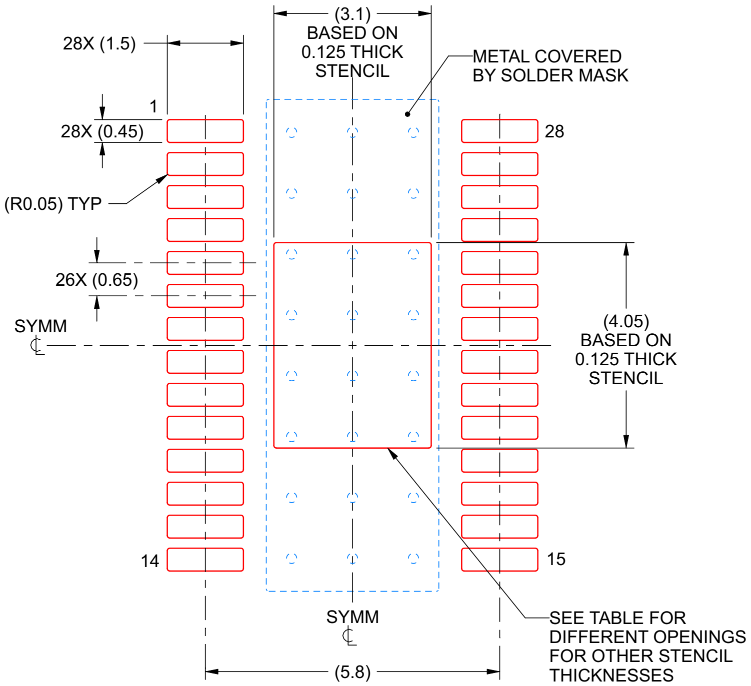
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

PWP0028M **PowerPAD™ TSSOP - 1.2 mm max height**

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.47 X 4.53
0.125	3.10 X 4.05 (SHOWN)
0.15	2.83 X 3.70
0.175	2.62 X 3.42

4224480/A 08/2018

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV8436EPWPR	ACTIVE	HTSSOP	PWP	28	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8436E	Samples
DRV8436ERGER	ACTIVE	VQFN	RGE	24	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DRV 8436E	Samples
DRV8436PPWPR	ACTIVE	HTSSOP	PWP	28	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8436P	Samples
DRV8436PRGER	ACTIVE	VQFN	RGE	24	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DRV 8436P	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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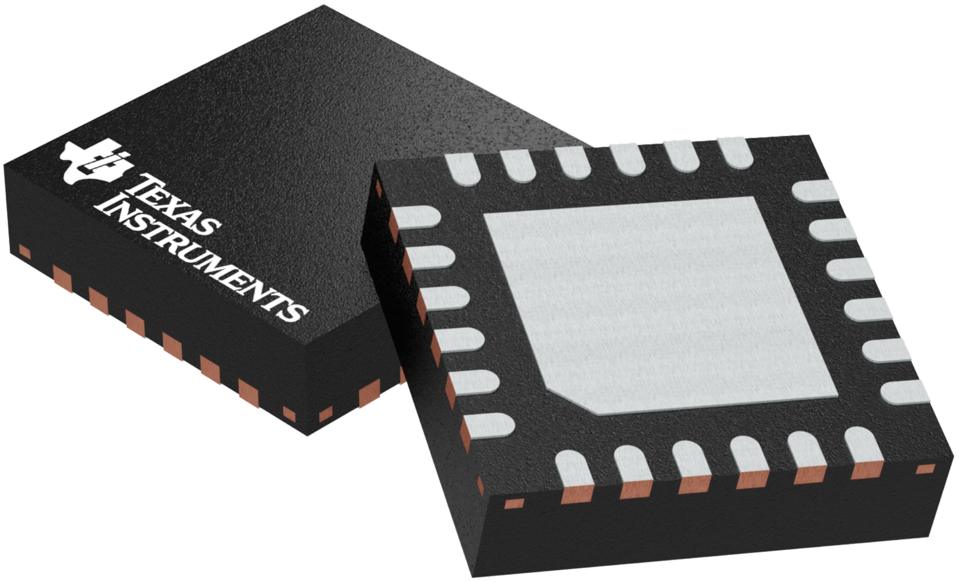
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

GENERIC PACKAGE VIEW

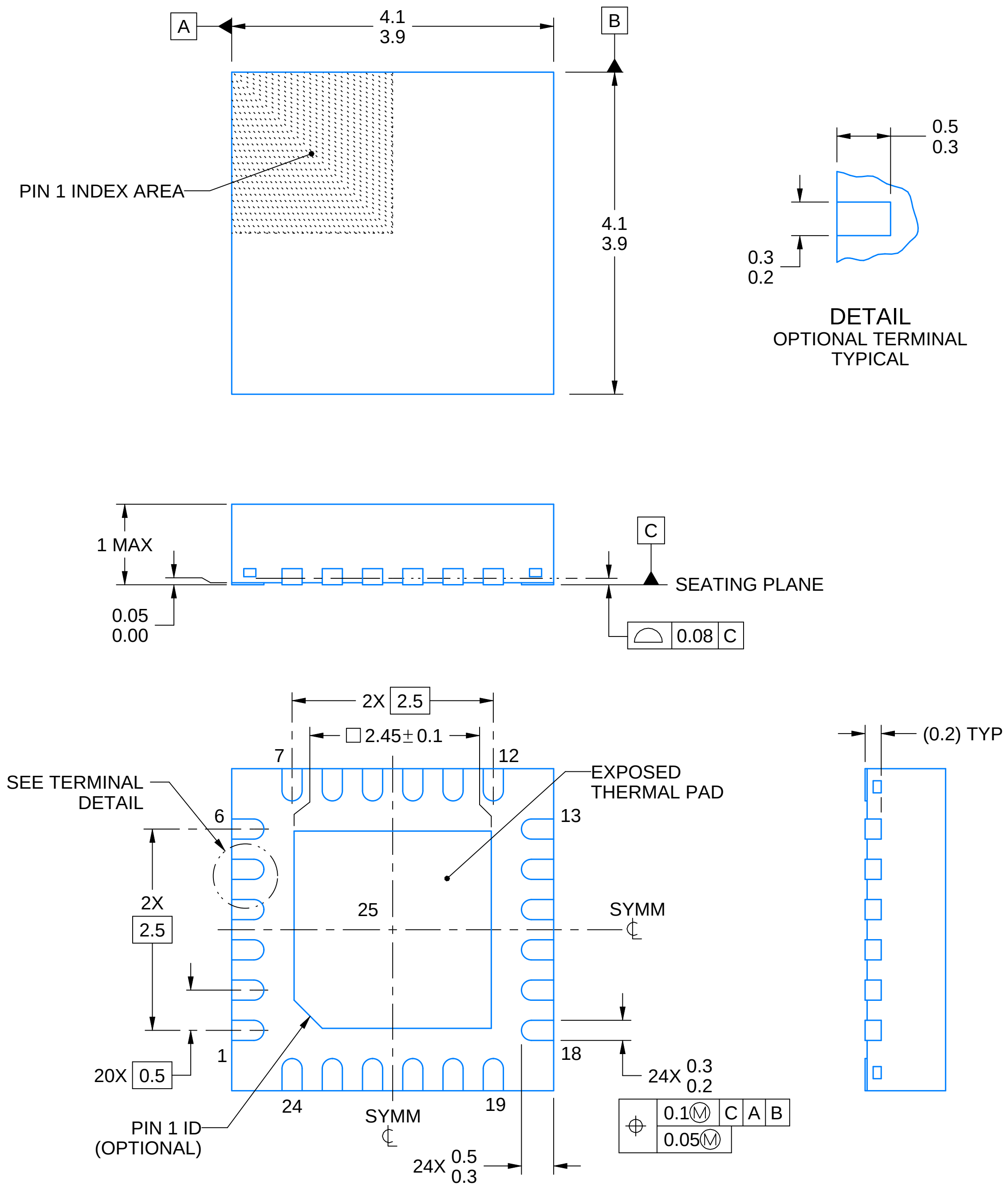
RGE 24 **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4204104/H



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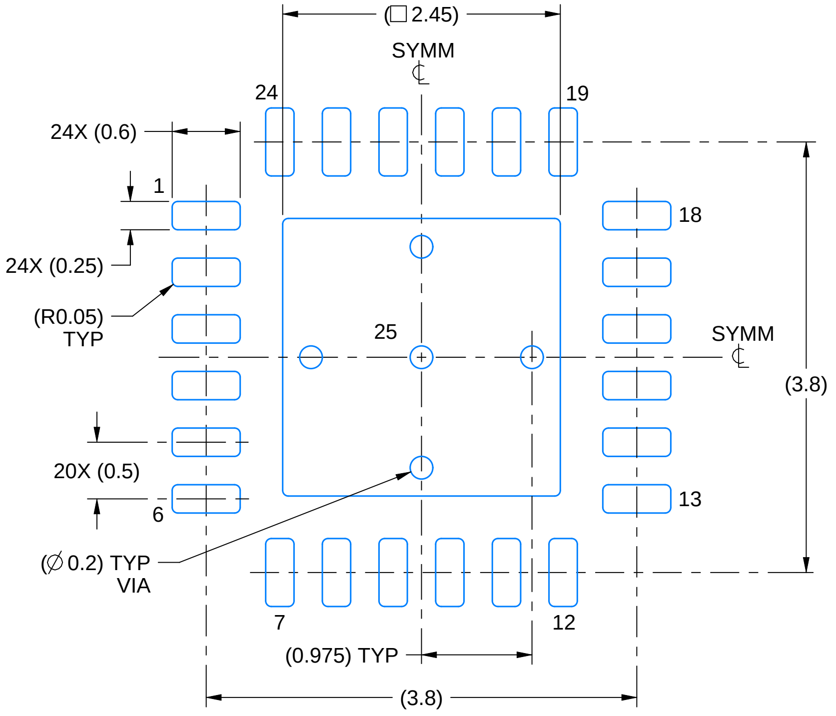
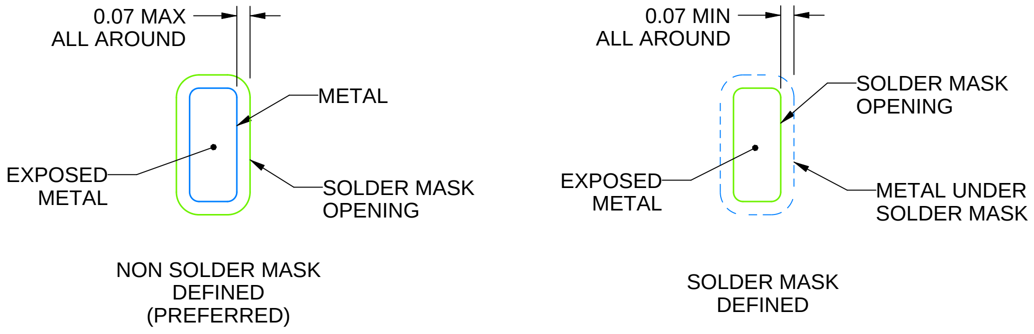
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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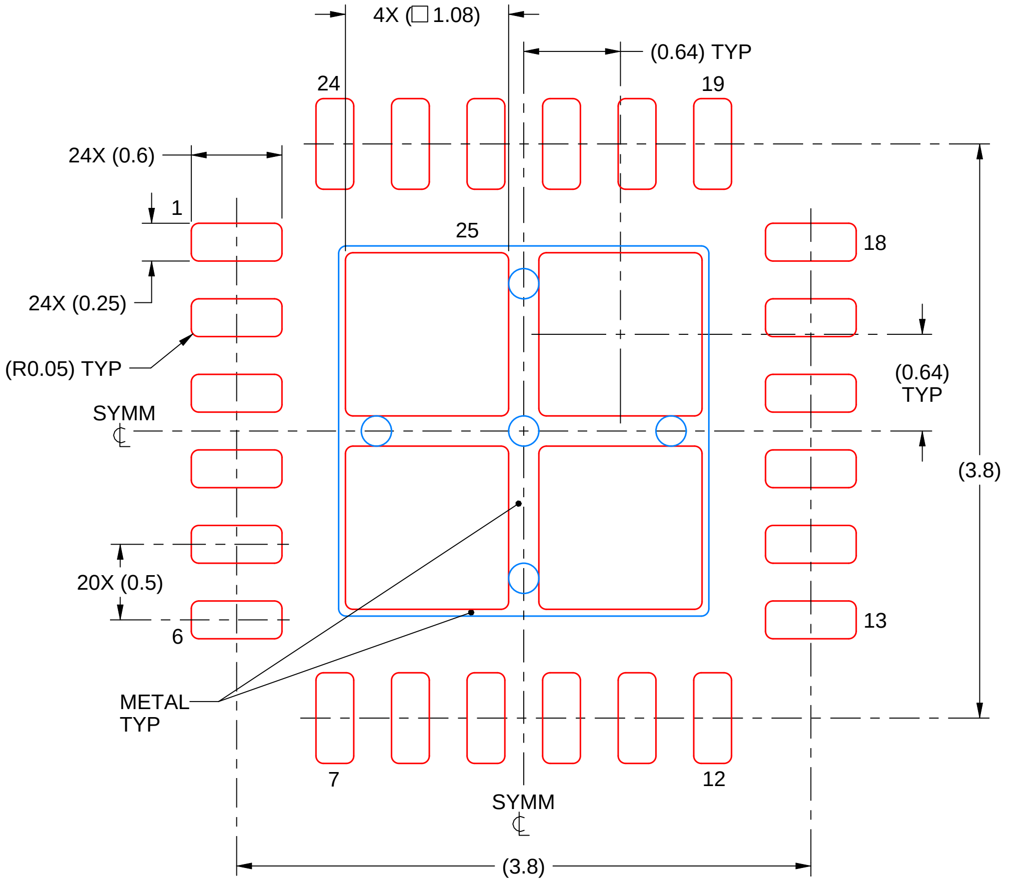
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

GENERIC PACKAGE VIEW

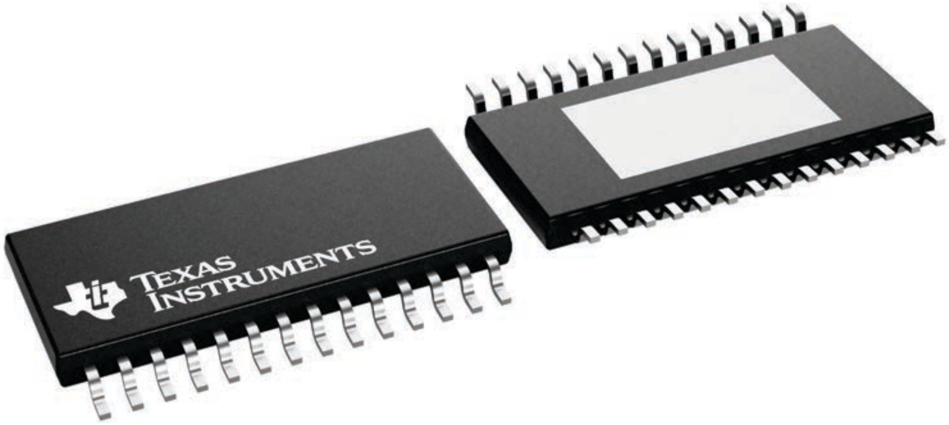
PWP 28

PowerPAD™ TSSOP - 1.2 mm max height

4.4 x 9.7, 0.65 mm pitch

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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