

## N-channel 600 V, 0.135 $\Omega$ typ., 20 A MDmesh™ II Power MOSFET in a TO-220FP package

Datasheet - production data

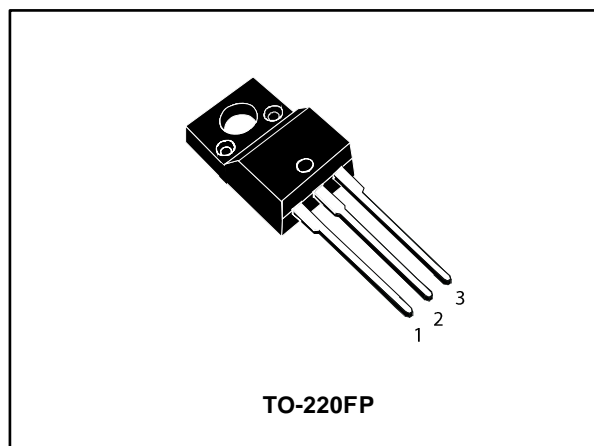
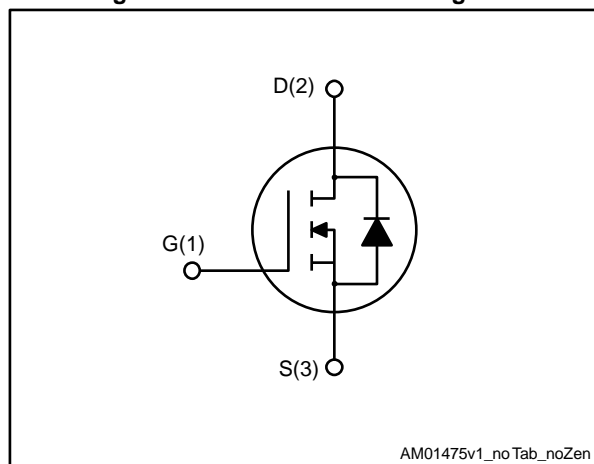


Figure 1: Internal schematic diagram



### Features

Order code	V <sub>DS</sub>	R <sub>DS(on)</sub> max	I <sub>D</sub>
STF26NM60N	600 V	0.165 $\Omega$	20 A

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

### Applications

- Switching applications

### Description

This device is an N-channel Power MOSFET developed using the second generation of MDmesh™ technology. This revolutionary Power MOSFET associates a vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters.

Table 1: Device summary

Order code	Marking	Package	Packaging
STF26NM60N	26NM60N	TO-220FP	Tube

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# 1 Electrical ratings

**Table 2: Absolute maximum ratings**

Symbol	Parameter	Value	Unit
V <sub>DS</sub>	Drain-source voltage	600	V
V <sub>GS</sub>	Gate-source voltage	±30	V
I <sub>D</sub> <sup>(1)</sup>	Drain current (continuous) at T <sub>C</sub> = 25 °C	20	A
I <sub>D</sub> <sup>(1)</sup>	Drain current (continuous) at T <sub>C</sub> = 100 °C	12.6	A
I <sub>DM</sub> <sup>(1)(2)</sup>	Drain current (pulsed)	80	A
P <sub>TOT</sub>	Total dissipation at T <sub>C</sub> = 25 °C	35	W
dv/dt <sup>(3)</sup>	Peak diode recovery voltage slope	15	V/ns
V <sub>ISO</sub>	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s; T <sub>C</sub> = 25 °C)	2500	V
T <sub>stg</sub>	Storage temperature range	-55 to 150	°C
T <sub>j</sub>	Operating junction temperature range		

**Notes:**

<sup>(1)</sup>Limited by package.

<sup>(2)</sup>Pulse width limited by safe operating area.

<sup>(3)</sup>I<sub>SD</sub> ≤ 20 A, di/dt ≤ 400 A/μs, V<sub>DS(peak)</sub> ≤ V<sub>(BR)DSS</sub>, V<sub>DD</sub> ≤ 80% V<sub>(BR)DSS</sub>

**Table 3: Thermal data**

Symbol	Parameter	Value	Unit
R <sub>thj-case</sub>	Thermal resistance junction-case	3.6	°C/W
R <sub>thj-amb</sub>	Thermal resistance junction-ambient	62.5	°C/W

**Table 4: Avalanche characteristics**

Symbol	Parameter	Value	Unit
I <sub>AS</sub>	Single pulse avalanche current (pulse width limited by T <sub>jmax</sub> )	6	A
E <sub>AS</sub>	Single pulse avalanche energy (starting T <sub>J</sub> =25 °C, I <sub>D</sub> =I <sub>AR</sub> , V <sub>DD</sub> =50 V)	610	mJ

## 2 Electrical characteristics

(T<sub>CASE</sub> = 25 °C unless otherwise specified)

**Table 5: On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source breakdown voltage	I <sub>D</sub> = 1 mA, V <sub>GS</sub> = 0 V	600			V
I <sub>DSS</sub>	Zero gate voltage drain current	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 600 V			1	μA
		V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 600 V, T <sub>C</sub> = 125 °C <sup>(1)</sup>			100	
I <sub>GSS</sub>	Gate-body leakage current	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±25 V			±0.1	μA
V <sub>GS(th)</sub>	Gate threshold voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	2	3	4	V
R <sub>DS(on)</sub>	Static drain-source on-resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 10 A		0.135	0.165	Ω

**Notes:**

<sup>(1)</sup>Defined by design, not subject to production test.

**Table 6: Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C <sub>iss</sub>	Input capacitance	V <sub>DS</sub> = 50 V, f = 1 MHz, V <sub>GS</sub> = 0 V	-	1800	-	pF
C <sub>oss</sub>	Output capacitance		-	115	-	pF
C <sub>rss</sub>	Reverse transfer capacitance		-	6	-	pF
C <sub>oss eq.</sub> <sup>(1)</sup>	Equivalent output capacitance	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 0 to 480 V	-	310	-	pF
Q <sub>g</sub>	Total gate charge	V <sub>DD</sub> = 480 V, I <sub>D</sub> = 20 A, V <sub>GS</sub> = 10 V (see <a href="#">Figure 14: "Test circuit for gate charge behavior"</a> )	-	60	-	nC
Q <sub>gs</sub>	Gate-source charge		-	8.5	-	nC
Q <sub>gd</sub>	Gate-drain charge		-	30	-	nC
R <sub>G</sub>	Gate input resistance	f = 1 MHz, I <sub>D</sub> = 0 A	-	2.8	-	Ω

**Notes:**

<sup>(1)</sup>C<sub>oss eq.</sub> is defined as a constant equivalent capacitance giving the same charging time as C<sub>oss</sub> when V<sub>DS</sub> increases from 0 to 80% V<sub>DS</sub>

**Table 7: Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t <sub>d(on)</sub>	Turn-on delay time	V <sub>DD</sub> = 300 V, I <sub>D</sub> = 10 A, R <sub>G</sub> = 4.7 Ω, V <sub>GS</sub> = 10 V (see <a href="#">Figure 13: "Test circuit for resistive load switching times"</a> and <a href="#">Figure 18: "Switching time waveform"</a> )	-	13	-	ns
t <sub>r</sub>	Rise time		-	25	-	ns
t <sub>d(off)</sub>	Turn-off delay time		-	85	-	ns
t <sub>f</sub>	Fall time		-	50	-	ns

Table 8: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}^{(1)}$	Source-drain current		-		20	A
$I_{SDM}^{(2)}$	Source-drain current (pulsed)		-		80	A
$V_{SD}^{(3)}$	Forward on voltage	$I_{SD} = 20 \text{ A}$ , $V_{GS} = 0 \text{ V}$	-		1.5	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 20 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 60 \text{ V}$ (see <a href="#">Figure 15: "Test circuit for inductive load switching and diode recovery times"</a> )	-	370		ns
$Q_{rr}$	Reverse recovery charge		-	5.8		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	31.6		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 20 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 60 \text{ V}$ , $T_j = 150 \text{ }^\circ\text{C}$ (see <a href="#">Figure 15: "Test circuit for inductive load switching and diode recovery times"</a> )	-	450		ns
$Q_{rr}$	Reverse recovery charge		-	7.5		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	32.5		A

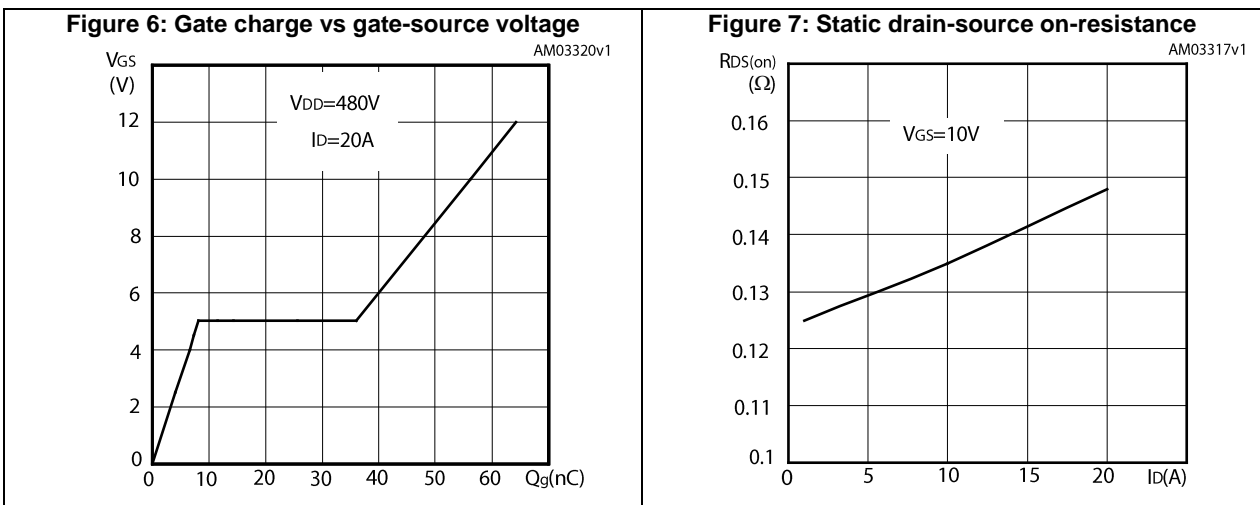
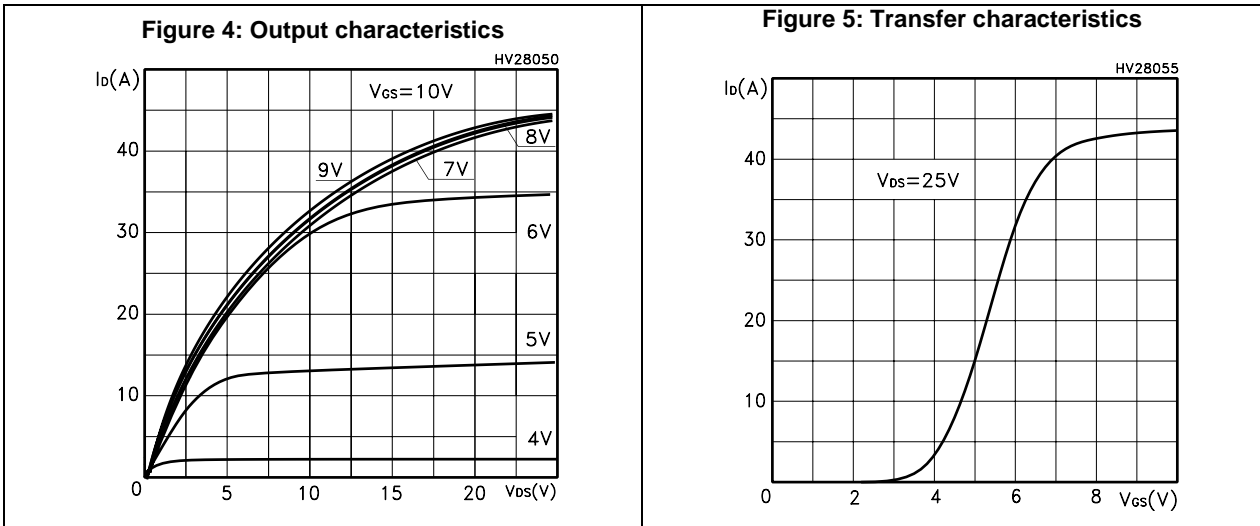
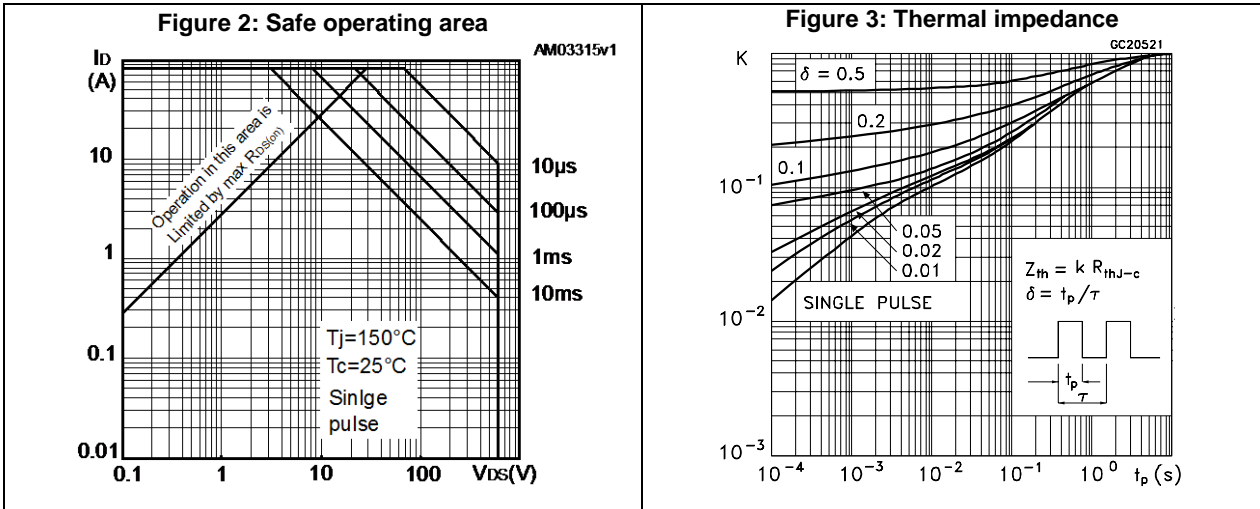
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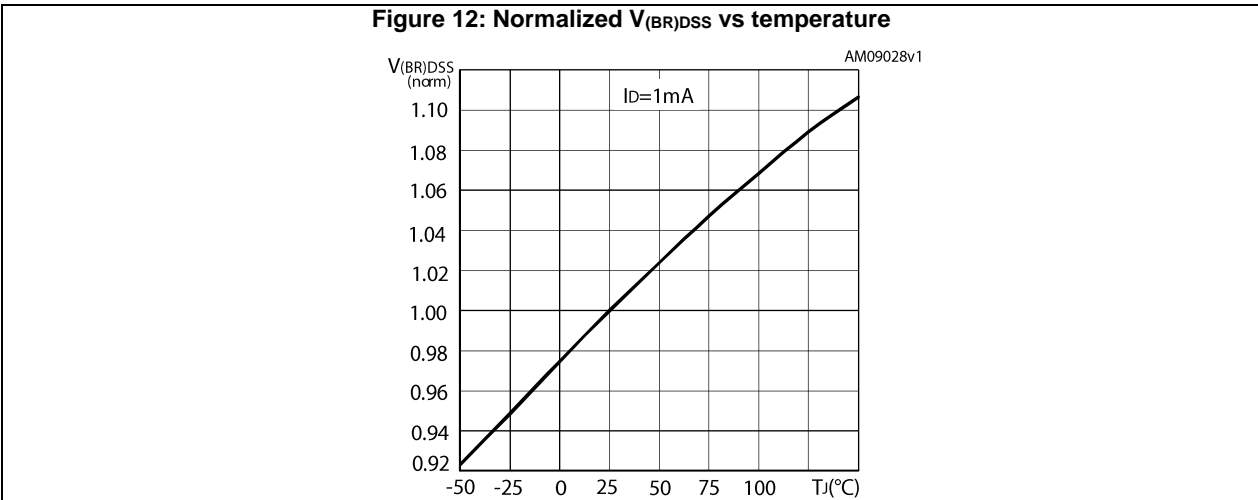
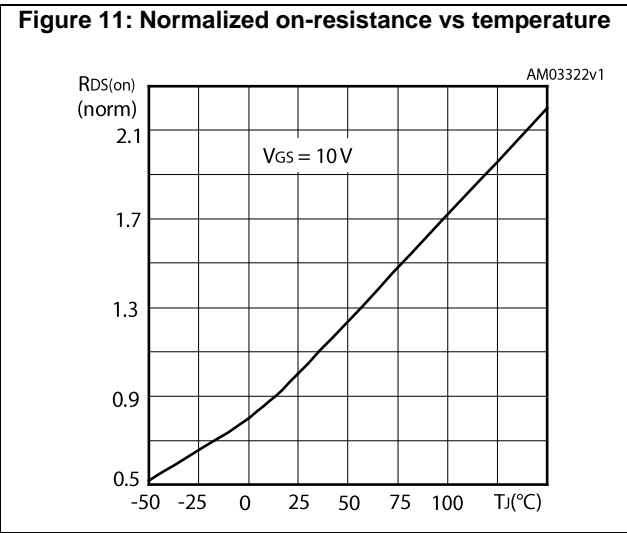
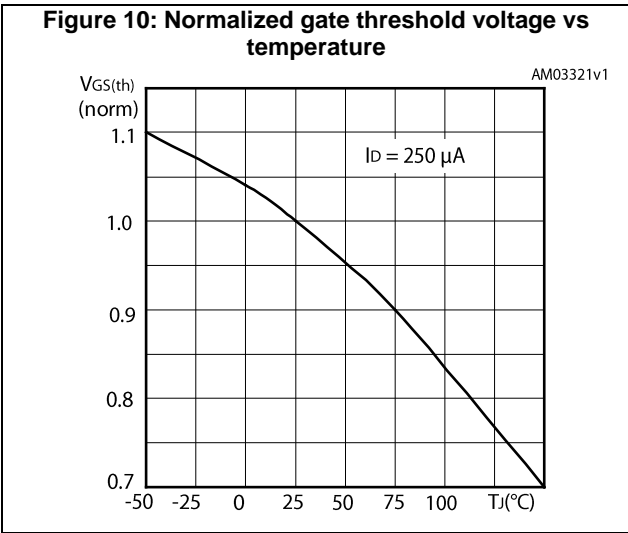
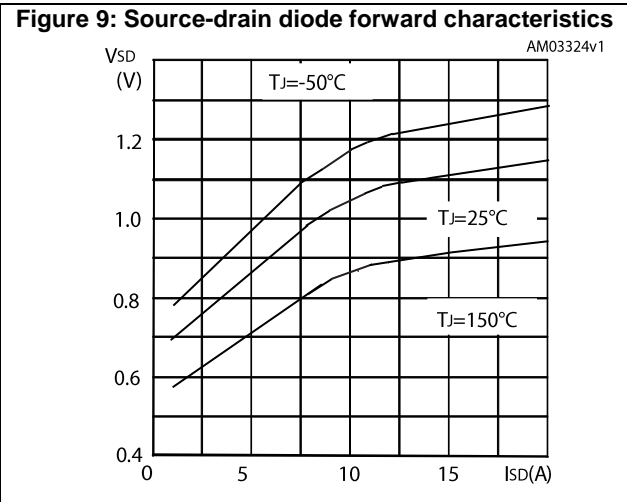
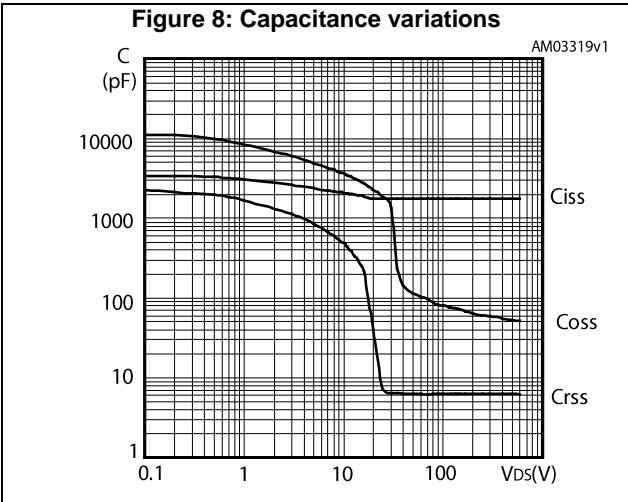
(1) Pulse width limited by package.

(2) Pulse width limited by safe operating area.

(3) Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)





### 3 Test circuits

**Figure 13: Test circuit for resistive load switching times**



AM01468v1

**Figure 14: Test circuit for gate charge behavior**



AM01469v1

**Figure 15: Test circuit for inductive load switching and diode recovery times**



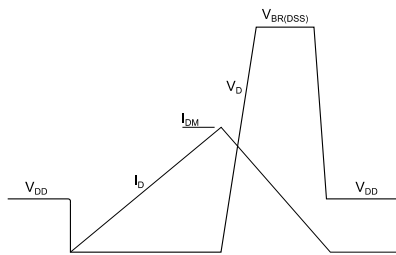
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**Figure 16: Unclamped inductive load test circuit**



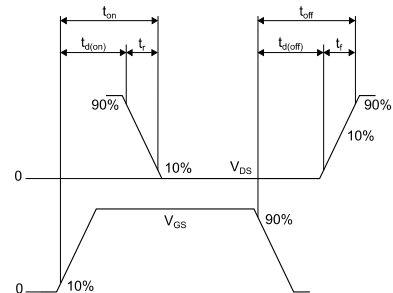
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**Figure 17: Unclamped inductive waveform**



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**Figure 18: Switching time waveform**



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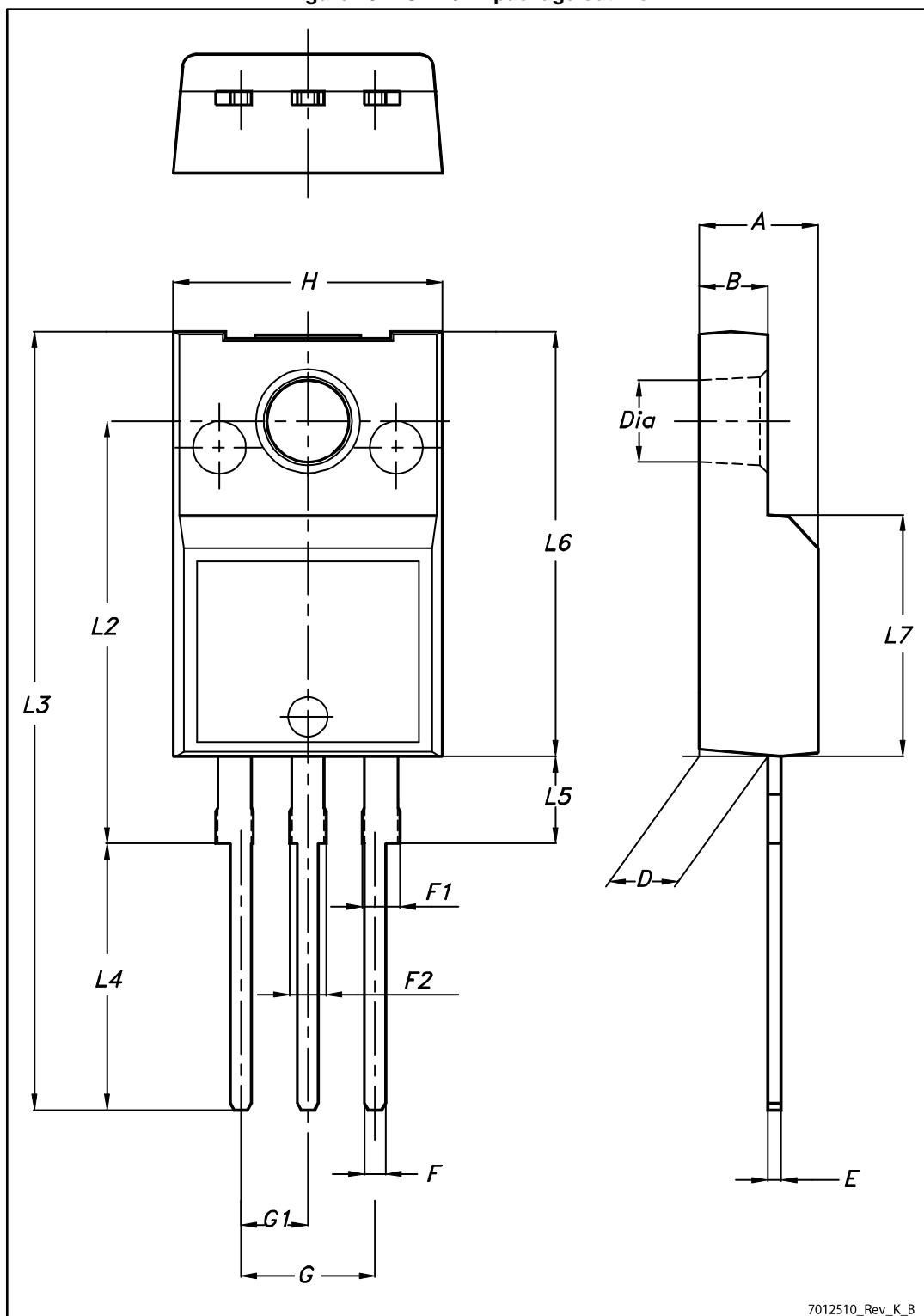


## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

### 4.1 TO-220FP package information

Figure 19: TO-220FP package outline



7012510\_Rev\_K\_B

Table 9: TO-220FP package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

## 5 Revision history

Table 10: Document revision history

Date	Revision	Changes
13-Dec-2016	1	First release. Part number previously included in datasheet DocID15642

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