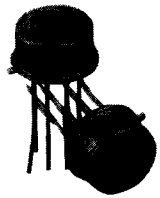
BURR-BROWN®

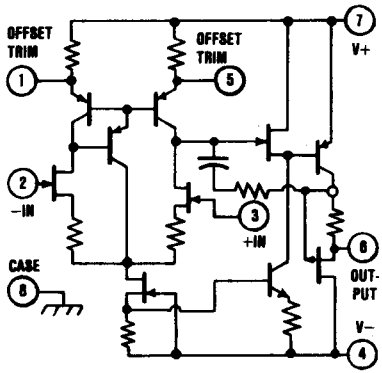


3550 SERIES

Fast-Settling FET OPERATIONAL AMPLIFIERS

FEATURES

- SETTLING TIME (0.01%), 600nsec, max
- TRUE DIFFERENTIAL INPUT
- SLEW RATE, 100V/μsec, min
- FULL POWER, 1.5MHz, min
- INPUT IMPEDANCE, $10^{11}\Omega$
- INTERNALLY COMPENSATED
- STABLE OPERATION, 1000pF, typ



DESCRIPTION

The 3550 is specifically designed for fast transient applications such as D/A and A/D conversion, sample/hold, multiplexer buffering and pulse amplification where the primary amplifier requirements are fast settling, good accuracy, and high input impedance.

Because the 3550 is internally compensated, elaborate compensation schemes requiring external components are not necessary. The smooth 6dB/octave rolloff of open-loop gain and the low output impedance provides the excellent step response and smooth settling without sacrificing frequency stability (no oscillations even with 1000pF of capacitive load)! A 10 to 1 improvement in settling time with large capacitive loads can be obtained with the addition of a single capacitor.

Unlike many wideband and fast settling amplifiers the 3550 has a true differential input. This means it can provide its excellent transient performance in the inverting, non-inverting, current to voltage, and difference configurations.

The 3550J and S have identical specifications except for temperature range: The 3550J is specified for 0°C to +70°C and the 3550S is specified for -55°C to +125°C. The 3550K has improved dynamic specifications and is specified over the 0°C to +70°C temperature range.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-302B

SPECIFICATIONS

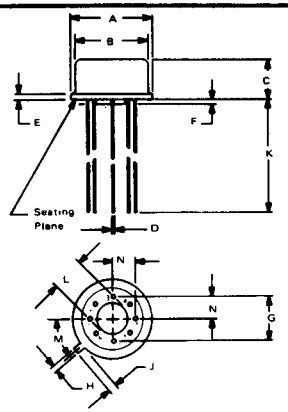
ELECTRICAL

Specifications typical at +25°C and ±15VDC Power Supply unless otherwise noted.

MODELS	3550J	3550K	3550S
OPEN LOOP GAIN, DC			
No load		100dB	
1kΩ, load min		88dB	
RATED OUTPUT			
Voltage, min		±10V	
Current, min		±10mA	
Open-loop Output Resistance		100Ω at 1MHz	
DYNAMIC RESPONSE			
Bandwidth (0dB, small signal)	10MHz	20MHz	10MHz
Full Power Response, min	1.0MHz	1.5MHz	1.0MHz
Slew Rate, min	65V/μsec	100V/μsec	65V/μsec
Settling Time (0.01%), max	1μsec	0.6μsec	1μsec
INPUT OFFSET VOLTAGE			
Initial Offset, +25°C, max		±1mV	
vs Temperature		±50μV/°C	
vs Supply Voltage		±500μV/V	
vs Time		±100μV/mo	
INPUT BIAS CURRENT			
Initial Bias, +25°C, max		−100pA (after full warm-up)	
vs Temperature		doubles every 10°C	
vs Supply Voltage		±1pA/V	
INPUT DIFFERENCE CURRENT			
Initial Difference, +25°C		±40pA	
INPUT IMPEDANCE			
Differential		$10^{11}\Omega$ || 3pF	
Common Mode		$10^{11}\Omega$ || 3pF	
INPUT NOISE			
Voltage, 0.01Hz - 10Hz, p-p		20μV	
10Hz - 10kHz, rms		4μV	
Current, 0.01Hz - 10Hz, p-p		0.2pA	
10Hz - 10kHz, rms		1.5pA	
INPUT VOLTAGE RANGE			
Common-Mode Voltage		±(|V_{cc}| −5)V	
Common-Mode Rejection		70dB at +5V, −10V	
Safe Input Voltage, max		±Supply	
POWER SUPPLY			
Rated Voltage		±15VDC	
Voltage Range, derated		±5VDC to ±20VDC	
Current, quiescent[1]		11mA	
TEMPERATURE RANGE			
Specification	0°C to +70°C		−55°C to +125°C
Operating	−55°C to +125°C		−55°C to +125°C
Storage		−65°C to +150°C	

NOTES:
1. The use of a finned heat sink is recommended.

MECHANICAL



NOTE:
Leads in true position within .010" (.25mm) R @ MMC at seating plane.
Pin numbers shown for reference only.
Numbers may not be marked on package.

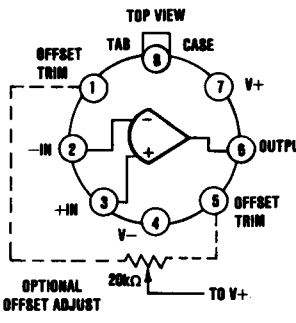
BOTTOM VIEW

Dimensions in inches are in parentheses.

Pin material and plating composition conform to method 2003 (solderability) of Mil-Std-883 (except paragraph 3.2)

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500		12.7	
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

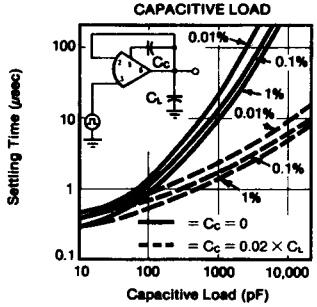
CONNECTION DIAGRAM



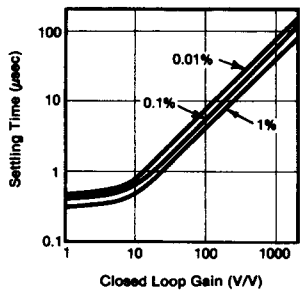
TYPICAL PERFORMANCE CURVES

T_A = +25°C ±V_{CC} = 15VDC unless otherwise indicated.

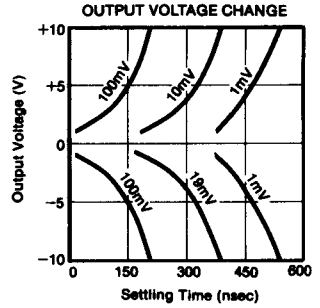
SETTLING TIME VS CAPACITIVE LOAD



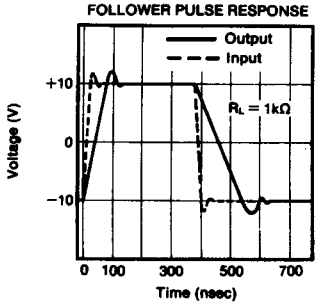
SETTLING TIME VS CLOSED LOOP GAIN



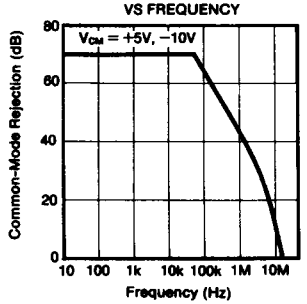
SETTLING TIME VS OUTPUT VOLTAGE CHANGE



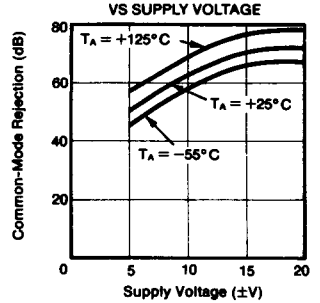
LARGE SIGNAL VOLTAGE FOLLOWER PULSE RESPONSE



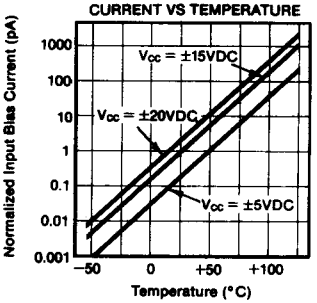
COMMON MODE REJECTION VS FREQUENCY



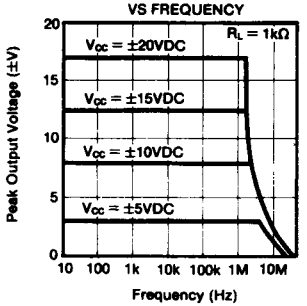
COMMON MODE REJECTION VS SUPPLY VOLTAGE



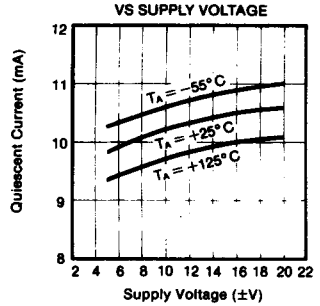
NORMALIZED INPUT BIAS CURRENT VS TEMPERATURE



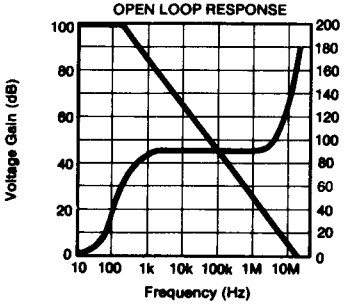
OUTPUT VOLTAGE VS FREQUENCY



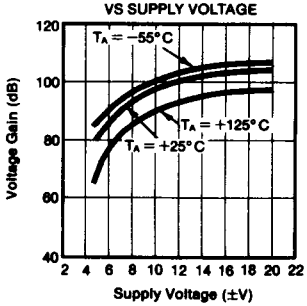
QUIESCENT CURRENT VS SUPPLY VOLTAGE



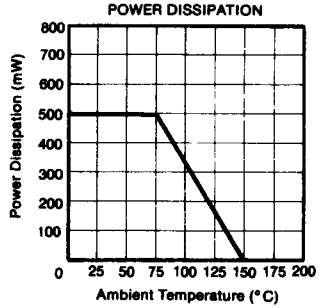
OPEN LOOP RESPONSE



OPEN LOOP GAIN VS SUPPLY VOLTAGE



MAXIMUM POWER DISSIPATION



APPLICATIONS

SETTLING TIME

Settling time of an amplifier is defined (see Figure 1) as the total time required, after an input step signal, for the output to "settle" within a specified error band around the final value. This error band is expressed as a percentage of the magnitude of the step transition. A recommended test circuit for settling time is shown in Figure 2. The output error signal appears, attenuated by a factor of two, at point A and may be observed at this point with the aid of an oscilloscope. The diodes act as limiters to prevent overloading the oscilloscope during the fast leading edge of the input signal. All resistors should be 2kΩ or less to eliminate degradation of performance due to stray capacitance. A typical measurement desired is the settling time to 0.01% for a 10-volt step input. This is the time required for the signal at point A to decrease to 0.5mV or less and remain below this level.

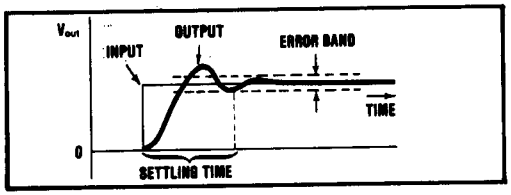


FIGURE 1. Concept of Settling Time.

Settling time for noninverting circuits can also be measured but requires the use of ultra-fast differential amplifier test fixtures. For the 3550 settling time is equal for inverting or noninverting circuits of equal gain.

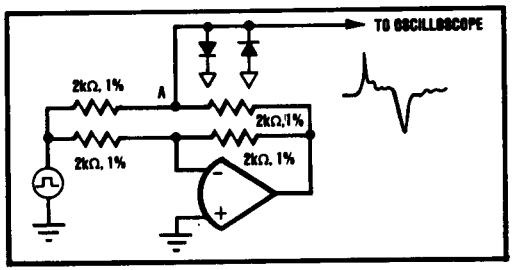


FIGURE 2. Settling Time Test Circuit.

Because settling time is affected by bandwidth which in turn is dependent upon closed-loop gain, the settling time of any operational amplifier will be a function of closed loop gain. Settling Time versus Gain curves illustrate this effect for the 3550 at several levels of settling accuracy.

The 3550 is remarkably tolerant of load capacitance because of its stable, 6dB/octave gain rolloff and low output impedance. Settling Time versus Load Capacitance curves show this characteristic for the unity-gain configuration. For larger values of load capacitance the compensation technique of Figure 3 may be used to optimize the response. The slight negative feedback provided by C_C tends to reduce any ringing at the top of the output voltage waveform without significantly affecting the slew rate. See the Settling Time versus Load Capacitance curves for typcial improvements in settling time.

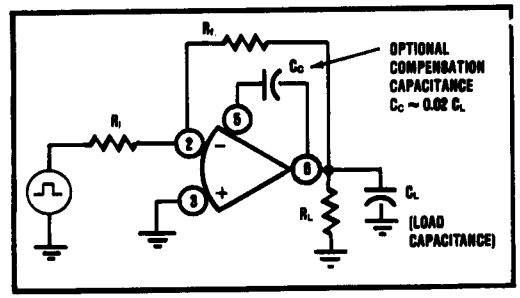


FIGURE 3. Compensation for Load Capacitance.

WIRING RECOMMENDATIONS

In order to fully realize the high frequency performance capabilities of the 3550, proper attention must be given to layout, component selection and grounding. All leads associated with the input and feedback elements should be as short as possible and all connections should be made as close to the amplifier terminals as possible. Input and feedback resistors should be made as small as possible consistent with other circuit constraints. Capacitance from the ouput to noninverting input can cause high frequency oscillations, particularly in high gain circuits operating from large source impedance. Careful layout of wiring or PC board patterns is the only satisfactory way of preventing such problems.

In order to prevent high frequency oscillations due to lead inductance the power supply leads should be bypassed. This should be done by connecting a 10μF tantalum capacitor in parallel with a 0.001μF ceramic capacitor from pins 7 and 4 to the power supply common.

INPUT AND OUTPUT VOLTAGE RANGE

Although the 3550 is specified for best operation on power supply voltage of ±15VDC, it will operate with minor performance changes over a power supply voltage range of ±5VDC to ±20VDC. Many of the curves show performance of the 3550 when operated from supplies other than ±15VDC.