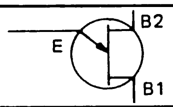
2N4870
2N4871

SOLID STATE INC.
46 FARRAND STREET
BLOOMFIELD, NEW JERSEY 07003
www.solidstateinc.com

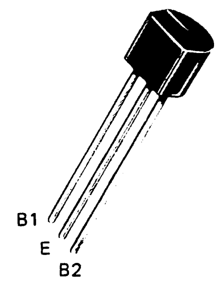


PN UNIJUNCTION TRANSISTORS

SILICON UNIJUNCTION TRANSISTORS

. . .designed for pulse and timing circuits, sensing circuits, and thyristor trigger circuits. These devices feature:

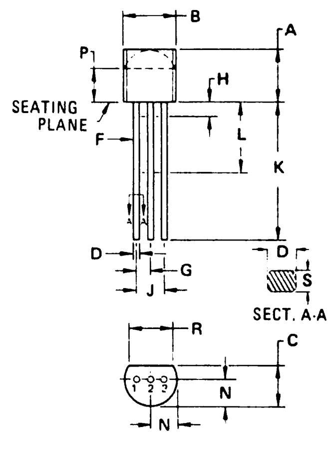
- Low Peak Point Current — 1.0 μA Typical
- Low Emitter Reverse Current — 5.0 nA Typical
- Passivated Surface for Reliability and Uniformity
- One-Piece Injection-Molded Unibloc‡ Plastic Package for Economy and Reliability
- High η for greater bandwith.



MAXIMUM RATINGS (T_A = 25° unless otherwise noted)

Rating	Symbol	Value	Unit
RMS Power Dissipation*	P_D*	300	mW
RMS Emitter Current	I_e	50	mA
Peak-Pulse Emitter Current**	i_e**	1.5	Amp
Emitter Reverse Voltage	V_{B2E}	30	Volts
Interbase Voltage†	V_{B2B1}†	35	Volts
Operating Junction Temperature Range	T_J	-55 to +125	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C

*Derate 3.0 mW/°C increase in ambient temperature.
**Duty cycle ≤ 1%, PRR = 10 PPS (see Figure 5).
†Based upon power dissipation at T_A = 25°C.



STYLE 9:
PIN 1. BASE 1
2. EMITTER
3. BASE 2

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.32	5.33	0.170	0.210
B	4.44	5.21	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.41	0.56	0.016	0.022
F	0.41	0.48	0.016	0.019
G	1.14	1.40	0.045	0.055
H	–	2.54	–	0.100
J	2.41	2.67	0.095	0.105
K	12.70	–	0.500	–
L	6.35	–	0.250	–
N	2.03	2.92	0.080	0.115
P	2.92	–	0.115	–
R	3.43	–	0.135	–
S	0.36	0.41	0.014	0.016

All JEDEC dimensions and notes apply.

FIGURE 1 — UNIJUNCTION TRANSISTOR SYMBOL AND NOMENCLATURE

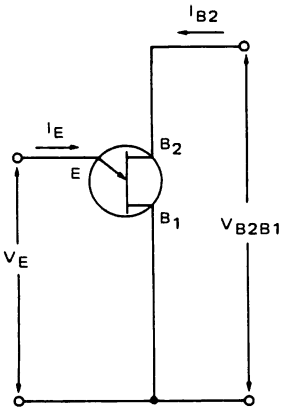
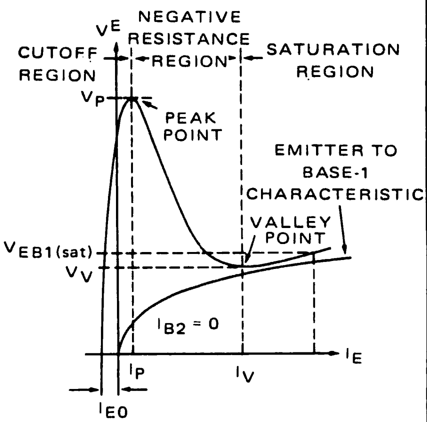


FIGURE 2 — STATIC EMITTER CHARACTERISTICS CURVES



ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Fig. No.	Symbol	Min	Typ	Max	Unit
Intrinsic Standoff Ratio* (V_{B2B1} = 10 V)	2N4870	4, 7	η*	0.56	–	0.75	–
	2N4871			0.70	–	0.85	
Interbase Resistance (V_{B2B1} = 3.0 V, I_E = 0)		10,11	R_{BB}	4.0	6.0	9.1	k ohms
Interbase Resistance Temperature Coefficient (V_{B2B1} = 3.0 V, I_E = 0, T_A = -65 to +125°C)		11	αR_{BB}	0.10	–	0.90	%/°C
Emitter Saturation Voltage** (V_{B2B1} = 10 V, I_E = 50 mA)			$V_{EB1(sat)}$**	–	2.5	–	Volts
Modulated Interbase Current (V_{B2B1} = 10 V, I_E = 50 mA)			$I_{B2(mod)}$	–	15	–	mA
Emitter Reverse Current (V_{B2E} = 30 V, I_{B1} = 0)		6	I_{EB2O}	–	0.005	1.0	μA
Peak-Point Emitter Current (V_{B2B1} = 25 V)		8, 9	I_P	–	1.0	5.0	μA
Valley-Point Current** (V_{B2B1} = 20 V, R_{B2} = 100 ohms)	2N4870	12, 13	I_V**	2.0	5.0	–	mA
	2N4871			4.0	7.0	–	
Base-One Peak Pulse Voltage	2N4870	3, 16	V_{OB1}	3.0	6.0	–	Volts
	2N4871			5.0	8.0	–	

* η, Intrinsic standoff ratio, is defined in terms of the peak-point voltage, V_P, by means of the equation: $V_P = \eta V_{B2B1} + V_F$, where V_F is about 0.49 volt at 25°C @ I_F = 10 μA and decreases with temperature at about 2.5 mV/°C. The test circuit is shown in Figure 4. Components R_1, C_1, and the UJT form a relaxation oscillator; the remaining circuitry serves as a peak-voltage detector. The forward drop of Diode D_1 compensates for V_R. To use, the "cal" button is pushed, and R_3 is adjusted to make the current meter, M_1, read full scale. When the "cal" button is released, the value of η is read directly from the meter, if full scale on the meter reads 1.0.

** Use pulse techniques: PW ≈ 300 μs, duty cycle ≤ 2.0% to avoid internal heating, which may result in erroneous readings.

FIGURE 3 — V_{OB1} TEST CIRCUIT

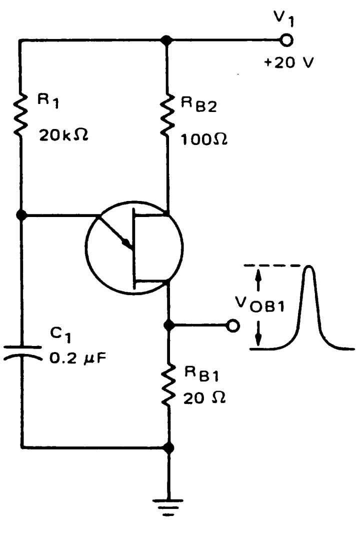


FIGURE 4 — η TEST CIRCUIT

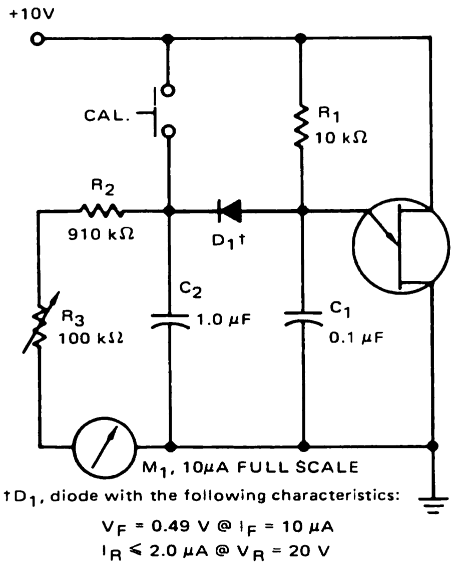
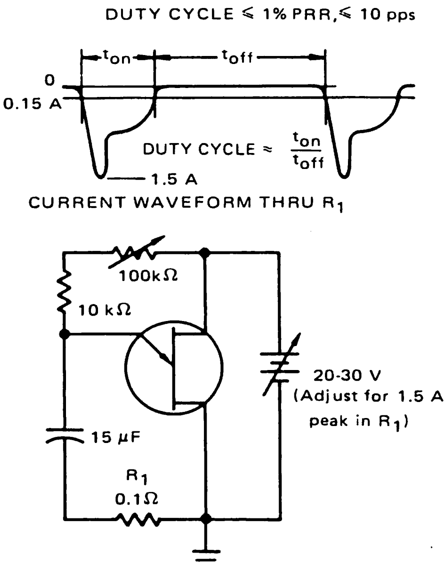


FIGURE 5 — PRR TEST CIRCUIT AND WAVEFORM



TYPICAL CHARACTERISTICS

FIGURE 6 – EMITTER REVERSE CURRENT

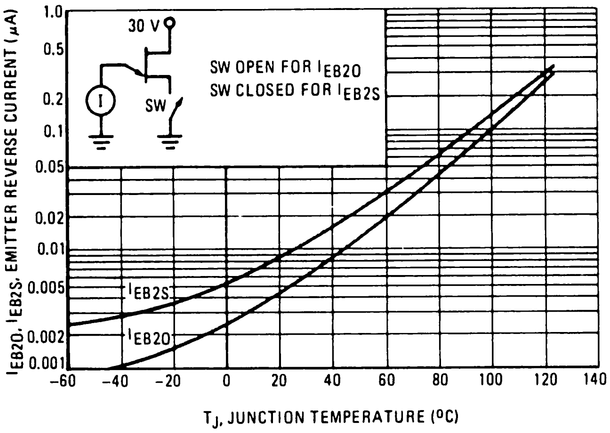
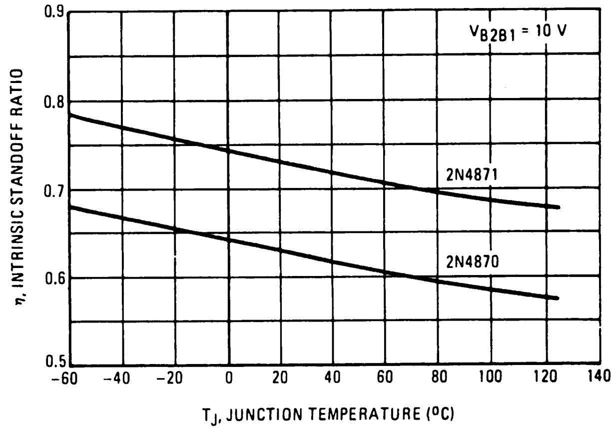


FIGURE 7 – INTRINSIC STANDOFF RATIO



PEAK POINT CURRENT

FIGURE 8 – EFFECT OF VOLTAGE

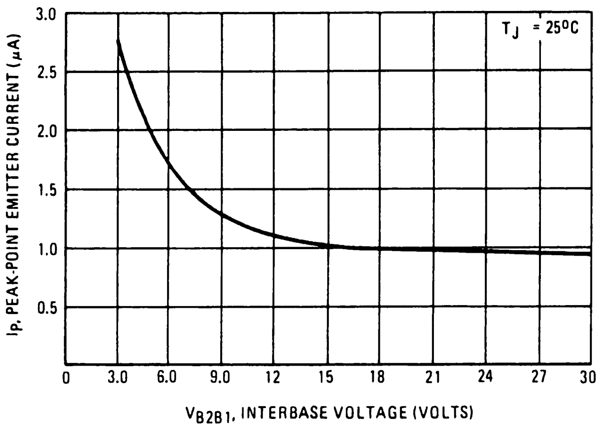
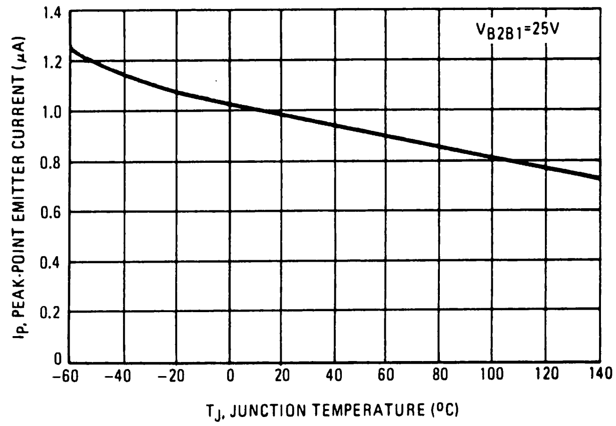


FIGURE 9 – EFFECT OF TEMPERATURE



INTERBASE RESISTANCE

FIGURE 10 – EFFECT OF VOLTAGE

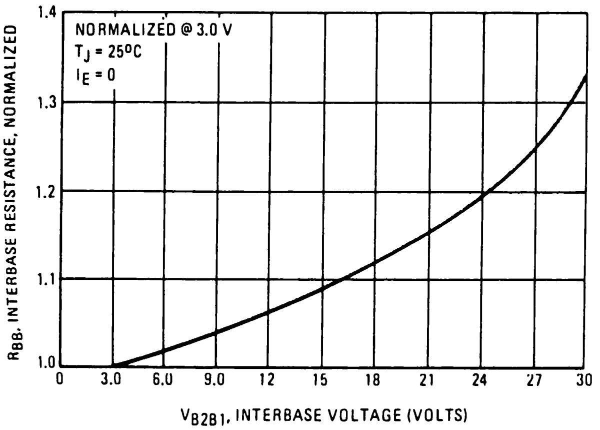
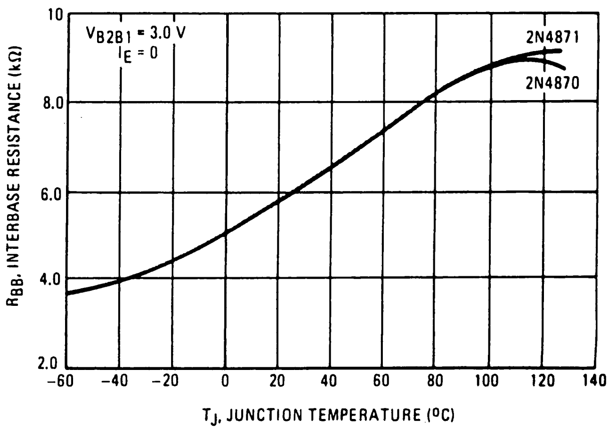


FIGURE 11 – EFFECT OF TEMPERATURE



TYPICAL CHARACTERISTICS

VALLEY CURRENT

FIGURE 12 – EFFECT OF VOLTAGE

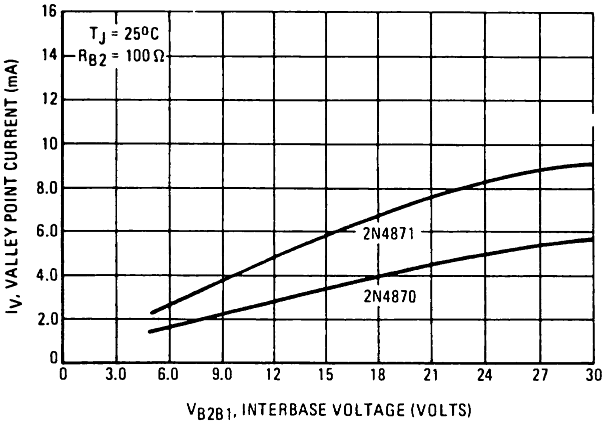
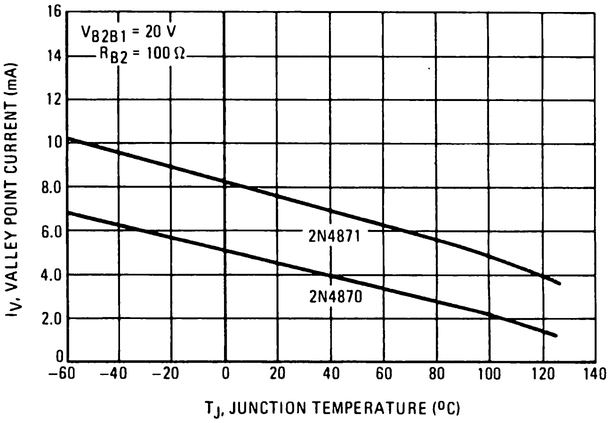


FIGURE 13 – EFFECT OF TEMPERATURE



VALLEY VOLTAGE

FIGURE 14 – EFFECT OF VOLTAGE

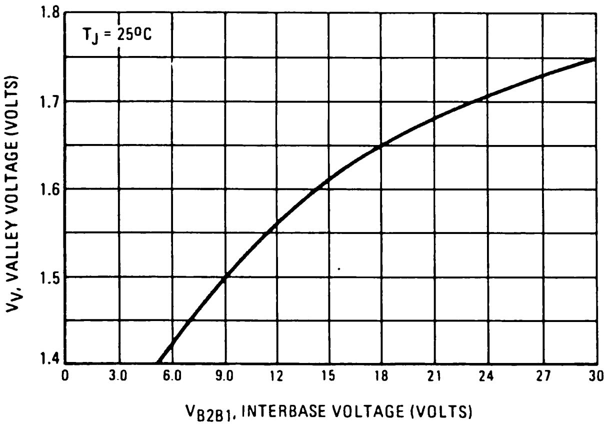


FIGURE 15 – EFFECT OF TEMPERATURE

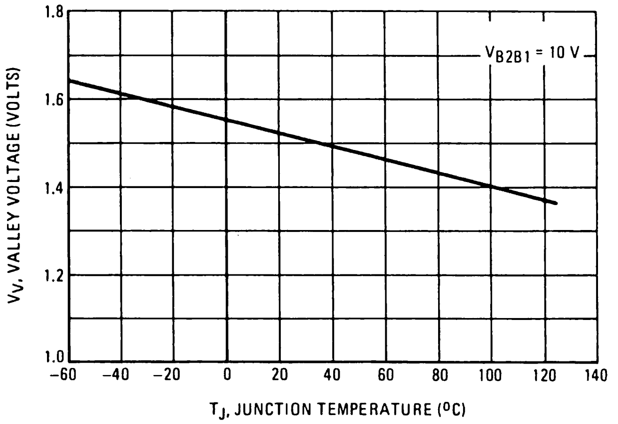


FIGURE 16 – OUTPUT VOLTAGE