



MM54HC563/MM74HC563 TRI-STATE® Octal D-Type Latch with Inverted Outputs

General Description

These high speed octal D-type latches utilize advanced silicon-gate CMOS technology. They possess the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 15 LS-TTL loads. Due to the large output drive capability and the TRI-STATE feature, these devices are ideally suited for interfacing with bus lines in a bus organized system.

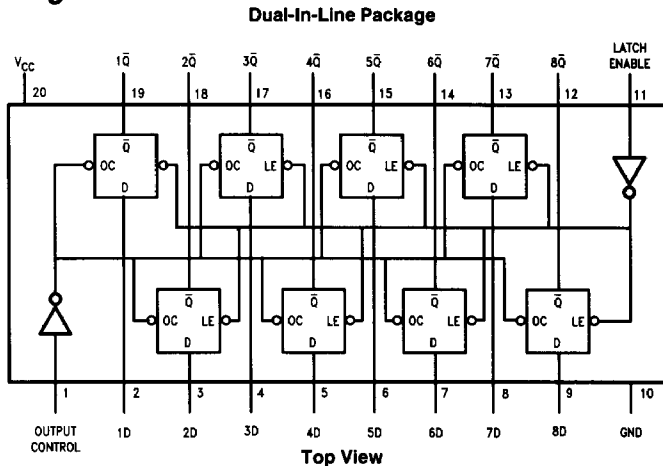
When the LATCH ENABLE (LE) input is high, the data present on the D inputs will appear inverted at the \bar{Q} outputs. When the LATCH ENABLE goes low, the inverted data will be retained at the \bar{Q} outputs until LATCH ENABLE returns high again. When a high logic level is applied to the OUTPUT CONTROL (OC) input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

The 54HC/74HC logic family is speed, function and pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 13 ns
- Wide operating voltage range: 2 to 6 volts
- Low input current: 1 μ A maximum
- Low quiescent current: 80 μ A maximum (74 Series)
- Compatible with bus-oriented systems
- Output drive capability: 15 LS-TTL loads
- Functionally compatible with '580

Connection Diagram



TL/F/5210-1

Order Number MM54HC563* or MM74HC563*

*Please look into Section 8, Appendix D for availability of various package types.

Truth Table

Output Control	Latch Enable	Data	Output
L	H	H	L
L	H	L	H
L	L	X	\bar{Q}_0
H	X	X	Z

H = high level, L = low level

\bar{Q}_0 = level of output before steady-state input conditions were established

Z = high impedance

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	-0.5 to +7.0V
DC Input Voltage (V_{IN})	-1.5 to $V_{CC} + 1.5V$
DC Output Voltage (V_{OUT})	-0.5 to $V_{CC} + 0.5V$
Clamp Diode Current (I_{CC})	± 20 mA
DC Output Current, per pin (I_{OUT})	± 35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	± 70 mA
Storage Temperature Range (T_{STG})	-65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	-40	+85	°C
MM54HC	-55	+125	°C
Input Rise or Fall Times (t_r, t_f)			
$V_{CC} = 2.0V$		1000	ns
$V_{CC} = 4.5V$		500	ns
$V_{CC} = 6.0V$		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	$T_A = 25^\circ C$			Units	
				Typ	74HC $T_A = -40$ to $85^\circ C$	54HC $T_A = -55$ to $125^\circ C$		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	V	
			4.5V		3.15	3.15	V	
			6.0V		4.2	4.2	V	
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	V	
			4.5V		1.35	1.35	V	
			6.0V		1.8	1.8	V	
V_{OH}	Minimum High Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL} $ I_{OUT} \leq 20 \mu A$	2.0V	2.0	1.9	1.9	V	
			4.5V	4.5	4.4	4.4	V	
			6.0V	6.0	5.9	5.9	V	
		$V_{IN} = V_{IH}$ or V_{IL} $ I_{OUT} \leq 6.0$ mA $ I_{OUT} \leq 7.8$ mA	4.5V	4.2	3.98	3.84	3.7	V
			6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL} $ I_{OUT} \leq 20 \mu A$	2.0V	0	0.1	0.1	V	
			4.5V	0	0.1	0.1	V	
			6.0V	0	0.1	0.1	V	
		$V_{IN} = V_{IH}$ or V_{IL} $ I_{OUT} \leq 6.0$ mA $ I_{OUT} \leq 7.8$ mA	4.5V	0.2	0.26	0.33	0.4	V
			6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN} = V_{CC}$ or GND	6.0V		± 0.1	± 1.0	μA	
I_{OZ}	Maximum TRI-STATE Output Leakage Current	$V_{OUT} = V_{CC}$ or GND $OC = V_{IH}$	6.0V		± 0.5	± 5.0	μA	
I_{CC}	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND $I_{OUT} = 0 \mu A$			8.0	80	160	μA

Note 1: Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: -12 mW/°C from 65°C to 85°C; ceramic "J" package: -12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V $\pm 10\%$ the worst case output voltages (V_{OH} and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at $V_{CC} = 5.5V$ and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN} , I_{CC} , and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

** V_{IL} limits are currently tested at 20% of V_{CC} . The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics $V_{CC} = 5V$, $T_A = 25^\circ C$, $t_r = t_f = 6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL} , t_{PLH}	Maximum Propagation Delay, Data to \bar{Q}	$C_L = 45$ pF	12	19	ns
t_{PHL} , t_{PLH}	Maximum Propagation Delay, LE to \bar{Q}	$C_L = 45$ pF	12	20	ns
t_{PZH} , t_{PZL}	Maximum Output Enable Time	$R_L = 1$ k Ω $C_L = 45$ pF	13	25	ns
t_{PHZ} , t_{PLZ}	Maximum Output Disable Time	$R_L = 1$ k Ω $C_L = 5$ pF	11	20	ns
t_S	Minimum Set Up Time, Data to LE		10	15	ns
t_H	Minimum Hold Time, LE to Data		2	5	ns
t_W	Minimum Pulse Width, LE or Data		10	16	ns

AC Electrical Characteristics $V_{CC} = 2.0-6.0V$, $t_r = t_f = 6$ ns

Symbol	Parameter	Conditions	V_{CC}	$T_A = 25^\circ C$		74HC $T_A = -40$ to $85^\circ C$		54HC $T_A = -55$ to $125^\circ C$		Units
				Typ		Guaranteed Limits				
t_{PHL} , t_{PLH}	Maximum Propagation Delay, Data to \bar{Q}	$C_L = 50$ pF $C_L = 150$ pF	2.0V	45	110	138		165		ns
			2.0V	58	150	188		225		ns
		4.5V	14	22	28		33		ns	
			21	30	38		40		ns	
t_{PHL} , t_{PLH}	Maximum Propagation Delay, LE to \bar{Q}	$C_L = 50$ pF $C_L = 150$ pF	2.0V	46	115	143		173		ns
			2.0V	60	155	194		233		ns
		4.5V	14	23	29		35		ns	
			21	31	47		47		ns	
t_{PZH} , t_{PZL}	Maximum Output Enable Time	$R_L = 1$ k Ω	2.0V	55	140	175		210		ns
			2.0V	67	180	225		270		ns
		4.5V	15	28	35		42		ns	
			24	36	45		54		ns	
t_{PHZ} , t_{PLZ}	Maximum Output Disable Time	$R_L = 1$ k Ω $C_L = 50$ pF	2.0V	40	125	156		188		ns
			4.5V	13	25	31		38		ns
		6.0V	12	21	27		32		ns	
			6.0V	14	24	30		36		ns
t_S	Minimum Set Up Time Data to LE		2.0V	30	75	95		110		ns
			4.5V	10	15	19		22		ns
			6.0V	9	13	16		19		ns
				2.0V	25	31	38		ns	
t_H	Minimum Hold Time LE to Data		4.5V	5	6	7		ns		
			6.0V	4	5	6		ns		
				2.0V	30	80	100		120	
			4.5V	9	16	20		24		ns
6.0V	8	14		18		20		ns		
	$C_L = 50$ pF	2.0V		25	60	75		90		ns
4.5V		7	12	15		18		ns		
6.0V		6	10	13		15		ns		
C_{PD}	Power Dissipation Capacitance (Note 5) (per latch)	$OC = V_{CC}$ $OC = GND$		30					pF	
				50					pF	
C_{IN}	Maximum Input Capacitance			5	10	10		10		pF
C_{OUT}	Maximum Output Capacitance			15	20	20		20		pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.