CORELIS
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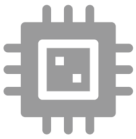
MTM-Bus


PXIe


Slave


Monitor


API


Master

PXIe-1149.5

IEEE-1149.5 MTM-Bus Tester

Features

- Message Based Device with Shared RAM
- Full IEEE-1149.5 Electrical and Protocol Compatibility
- Three modes of operation: MTM-Bus Master, Slave, or Bus Monitor
- Dual MTM-Bus Physical Interfaces
- Two MTM-Bus Interface Options: TTL or BTL
- Error Injection and Detection on a Word-by-Word basis
- 64 MB Shared Memory for Transmit and Receive Data Storage
- Received Data Time Stamping
- Programmable MTM-Bus Clock Speeds up to 12.5MHz
- Internally or Externally Generated Clock Source
- Drivers and API for Microsoft Windows

Benefits

- Test and monitor IEEE-1149.5-compliant MTM-Bus interfaces
- Single instrument can be configured as master, slave, or monitor
- PXIe interface for integration with modern ATE systems

IEEE-1149.5 standardizes a serial backplane test and maintenance bus (MTM-Bus) to integrate testable modules, which may consist of one or more logic boards, into a testable and maintainable subsystem using a multidrop serial backplane.

The Corelis PXIe-1149.5 is a versatile, multi-mode instrument for interfacing with MTM-Bus modules. The PXIe-1149.5 adds MTM-Bus master, slave, and monitoring with full IEEE-1149.5 electrical and protocol compatibility with a standard PXIe interface for convenient integration into any Test Program Set (TPS).

Featuring programmable clock rate, dual MTM-Bus interface circuits, configurable TTL or BTL physical interfaces, and on-board directive execution, PXIe-1149.5 can accommodate a variety of system configurations.

Applications

Hardware Development
Test and debug IEEE-1149.5 interfaces with a versatile master, slave, and monitor test instrument.

ATE Integration
Integrate MTM-bus control with popular ATE environments such as NI LabWindows, Teststand, and more using a C-style API.

Service & Repair
Add IEEE-1149.5 capability to based avionics repair depot ATE systems with a modern, PXIe-based interface.

PXIe-1149.5™

The PXIe-1149.5 is a single-slot, 3U PXIe module designed for control, test, and simulation of systems that utilize the IEEE-1149.5 Standard Backplane Module Test and Maintenance (MTM) bus protocol. The PXIe-1149.5 provides intelligent interfacing between the serial MTM-Bus and a PXIe bus host. Software controls the PXIe-1149.5 operation as either an MTM-Bus master, slave, or bus monitor. Extensive error injection and detection capabilities are also provided. Its full compliance with the IEEE-1149.5 MTM-Bus protocol and the PXIe bus makes it an excellent choice for testing, dynamic simulation, and development applications.

MTM-Bus Communication

The MTM-Bus interface is configured differently for the three modes of operation. In the **Master** mode of operation, the PXIe-1149.5 module drives the MCLK, MCTL, and MMD signals and receives the MSD and the MPR signals. The user can configure the card to receive MCLK externally and to ignore the slave MPR signal.

In the **Slave** mode of operation, the card receives the MCLK, MCTL and MMD signals and drives the MSD and the MPR signals. The user can also configure the card to drive MCLK.

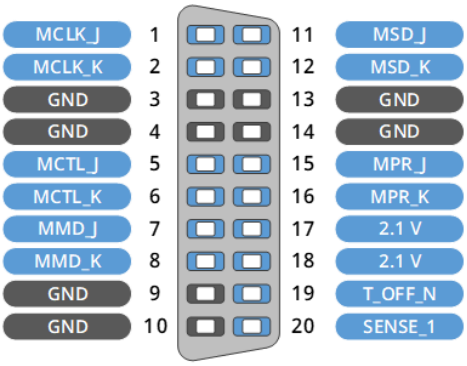
In the **Monitor** mode, the card only receives the MTM-Bus signals and the data sent by both the master and slaves. This data is recorded in the shared memory along with the timestamp of each transfer. The user can program the card to receive all messages or to filter the data and only record messages sent to or from a particular MTM-Bus slave. A pattern matching mechanism is also provided.

Transfer Rates

The MCLK clock rate is programmable from 156 kHz to 12.5 MHz in steps. The user has the option of configuring the card to generate the clock on-board or to receive it from an external source. The clock source selections include the on-board clock generator, the front panel EXT CLK connector, or the MTM-Bus (external) MCLK signal.

Directives

Operation of the MTM-Bus interface is controlled by special commands called directives. Unlike word serial commands, directives are memory-based commands. The directives reside in a pre-assigned area of memory and are typically written by the host and read by the onboard microprocessor. In a typical MTM-Bus application, the host configures the card via the word serial protocol and then instructs the embedded microprocessor to begin interpreting the directives.



MTM-Bus Connector Pinout Diagram

Embedded Microprocessor

An embedded microprocessor provides the on-board intelligence of the PXIe-1149.5 module. The microprocessor may be used to run user-created embedded code for on-board directive execution.

Software API

The PXIe-1149.5 module is controlled through a C DLL application programming interface (API). The API can be integrated into a variety of programming languages or used with systems such as NI LabVIEW, LabWindows/CVI, and more.

IEEE-1149.5 Selected Hardware Specifications[1]

General	
Dimensions	6.3 in. (160 mm) x 3.9 in. (100 mm) x 0.8 in. (18.4 mm)
Interface	PXIe 3U Module
Certifications	RoHS Compliant
Interface	
MTM-Bus	20-Pos D-Sub connector (TE Connectivity 5787190-1 or equivalent)
External Clock	SMA connector for external clock input
MTM-Bus Output	
BTL Transceivers	BTL open collector, 100 mA sink current
TTL Transceivers	BTL open collector, 64 mA sink current

[1]For detailed specifications, please see the PXIe-1149.5 User's Manual.

Ordering Information

Part Number - 10421

For more information, or to order this product online, please visit our website at www.corelis.com

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