

## N-channel 30 V, 0.021 $\Omega$ typ., 6 A STripFET™ H6 Power MOSFET in a PowerFLAT™ 2x2 package

Datasheet - production data

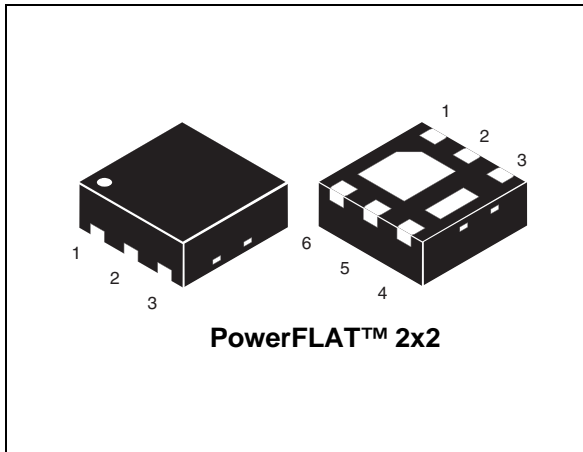
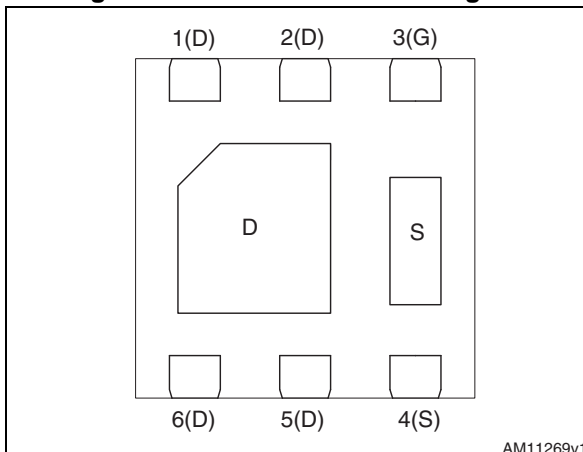


Figure 1. Internal schematic diagram



### Features

| Order code | V <sub>DS</sub> | R <sub>DS(on)</sub> max   | I <sub>D</sub> | P <sub>TOT</sub> |
|------------|-----------------|---|----------------|------------------|
| STL6N3LLH6 | 30 V            | 0.025 $\Omega$ (V <sub>GS</sub> =10 V)<br>0.04 $\Omega$ (V <sub>GS</sub> = 4.5 V) | 6 A            | 2.4 W            |

- Very low on-resistance
- Very low gate charge
- High avalanche ruggedness
- Low gate drive power loss

### Applications

- Switching applications

### Description

This device is an N-channel Power MOSFET developed using the STripFET™ H6 technology, with a new trench gate structure. The resulting Power MOSFET exhibits very low R<sub>DS(on)</sub> in all packages.

Table 1. Device summary

| Order code | Marking | Package        | Packaging     |
|------------|---------|----------------|---------------|
| STL6N3LLH6 | STG1    | PowerFLAT™ 2x2 | Tape and reel |

# Contents

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

| Symbol            | Parameter   | Value      | Unit             |
|-------------------|---|------------|------------------|
| $V_{DS}$          | Drain-source voltage  | 30         | V                |
| $V_{GS}$          | Gate-source voltage   | $\pm 20$   | V                |
| $I_D^{(1)}$       | Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$      | 13         | A                |
| $I_D^{(1)}$       | Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$     | 8.2        | A                |
| $I_{DM}^{(1)(2)}$ | Drain current (pulsed)  | 52         | A                |
| $I_D^{(3)}$       | Drain current (continuous) at $T_{pcb} = 25\text{ }^\circ\text{C}$  | 6          | A                |
| $I_D^{(3)}$       | Drain current (continuous) at $T_{pcb} = 100\text{ }^\circ\text{C}$ | 3.75       | A                |
| $I_{DM}^{(2)(3)}$ | Drain current (pulsed)  | 24         | A                |
| $P_{TOT}^{(1)}$   | Total dissipation at $T_C = 25\text{ }^\circ\text{C}$               | 7.8        | W                |
| $P_{TOT}^{(3)}$   | Total dissipation at $T_{pcb} = 25\text{ }^\circ\text{C}$           | 2.4        |                  |
| $T_J$             | Operating junction temperature                                      | -55 to 150 | $^\circ\text{C}$ |
| $T_{stg}$         | Storage temperature   |            |                  |

1. This value is rated according to  $R_{thj-case}$
2. Pulse width limited by safe operating area
3. This value is rated according to  $R_{thj-pcb}$

**Table 3. Thermal resistance**

| Symbol              | Parameter                            | Value | Unit                      |
|---------------------|--------------------------------------|-------|---------------------------|
| $R_{thj-pcb}^{(1)}$ | Thermal resistance junction-pcb      | 52    | $^\circ\text{C}/\text{W}$ |
| $R_{thj-case}$      | Thermal resistance junction-case max | 16    | $^\circ\text{C}/\text{W}$ |

1. When mounted on FR-4 board of 1inch<sup>2</sup>, 2oz Cu,  $t < 10\text{ sec}$

## 2 Electrical characteristics

( $T_{CASE} = 25\text{ °C}$  unless otherwise specified).

**Table 4. On/off states**

| Symbol        | Parameter                         | Test conditions  | Min. | Typ.  | Max.      | Unit          |
|---------------|-----------------------------------|--|------|-------|-----------|---------------|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage    | $I_D = 250\ \mu\text{A}$ , $V_{GS} = 0\ \text{V}$                  | 30   |       |           | V             |
| $I_{DSS}$     | Zero gate voltage drain current   | $V_{DS} = 30\ \text{V}$ , $V_{GS} = 0$                             |      |       | 1         | $\mu\text{A}$ |
|               |                                   | $V_{DS} = 30\ \text{V}$ , $T_C = 125\text{°C}$<br>( $V_{GS} = 0$ ) |      |       | 10        | $\mu\text{A}$ |
| $I_{GSS}$     | Gate body leakage current         | $V_{GS} = \pm 20\ \text{V}$ , ( $V_{DS} = 0$ )                     |      |       | $\pm 100$ | nA            |
| $V_{GS(th)}$  | Gate threshold voltage            | $V_{DS} = V_{GS}$ , $I_D = 250\ \mu\text{A}$                       | 1    |       |           | V             |
| $R_{DS(on)}$  | Static drain-source on-resistance | $V_{GS} = 10\ \text{V}$ , $I_D = 3\ \text{A}$                      |      | 0.021 | 0.025     | $\Omega$      |
|               |                                   | $V_{GS} = 4.5\ \text{V}$ , $I_D = 3\ \text{A}$                     |      | 0.032 | 0.04      | $\Omega$      |

**Table 5. Dynamic**

| Symbol    | Parameter                    | Test conditions  | Min. | Typ. | Max. | Unit |
|-----------|------------------------------|--|------|------|------|------|
| $C_{iss}$ | Input capacitance            | $V_{DS} = 24\ \text{V}$ , $f = 1\ \text{MHz}$ ,<br>( $V_{GS} = 0$ )  | -    | 283  | -    | pF   |
| $C_{oss}$ | Output capacitance           |  | -    | 61   | -    |      |
| $C_{rss}$ | Reverse transfer capacitance |  | -    | 31   | -    |      |
| $Q_g$     | Total gate charge            | $V_{DD} = 15\ \text{V}$ , $I_D = 6\ \text{A}$<br>$V_{GS} = 4.5\ \text{V}$<br>(see <a href="#">Figure 14.: Gate charge test circuit</a> ) | -    | 3.6  | -    | nC   |
| $Q_{gs}$  | Gate-source charge           |  | -    | 1.5  | -    |      |
| $Q_{gd}$  | Gate-drain charge            |  | -    | 1.1  | -    |      |

**Table 6. Switching times**

| Symbol       | Parameter           | Test conditions   | Min. | Typ. | Max. | Unit |
|--------------|---------------------|---|------|------|------|------|
| $t_{d(on)}$  | Turn-on delay time  | $V_{DD} = 10\ \text{V}$ , $I_D = 6\ \text{A}$ ,<br>$R_G = 4.7\ \Omega$ , $V_{GS} = 4.5\ \text{V}$<br>(see <a href="#">Figure 13.: Switching times test circuit for resistive load</a> ) | -    | 4.8  | -    | ns   |
| $t_r$        | Rise time           |   | -    | 11.2 | -    |      |
| $t_{d(off)}$ | Turn-off delay time |   | -    | 9.4  | -    |      |
| $t_f$        | Fall time           |   | -    | 5.4  | -    |      |

Table 7. Source drain diode

| Symbol         | Parameter                | Test conditions   | Min. | Typ. | Max. | Unit |
|----------------|--------------------------|---|------|------|------|------|
| $V_{SD}^{(1)}$ | Forward on voltage       | $I_{SD} = 6 \text{ A}$ , $V_{GS} = 0 \text{ V}$   | -    |      | 1.1  | V    |
| $t_{rr}$       | Reverse recovery time    | $I_{SD} = 6 \text{ A}$ ,<br>$di/dt = 100 \text{ A}/\mu\text{s}$ ,<br>$V_{DD} = 16 \text{ V}$ , $T_J = 150 \text{ }^\circ\text{C}$ | -    | 10.6 |      | ns   |
| $Q_{rr}$       | Reverse recovery charge  |   | -    | 2.8  |      | nC   |
| $I_{RRM}$      | Reverse recovery current |   | -    | 0.5  |      | A    |

1. Pulsed: pulse duration=300 $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

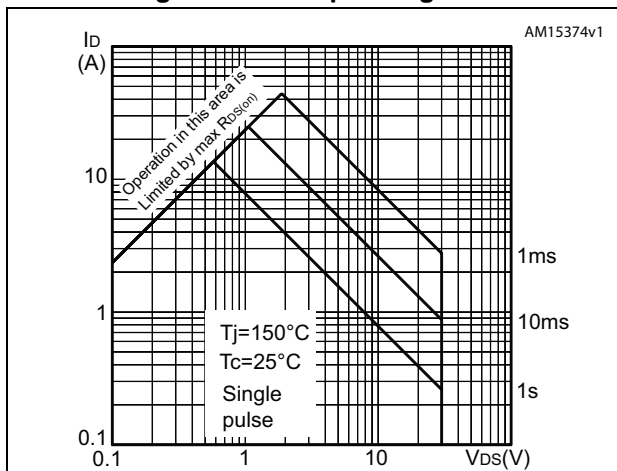


Figure 3. Thermal impedance

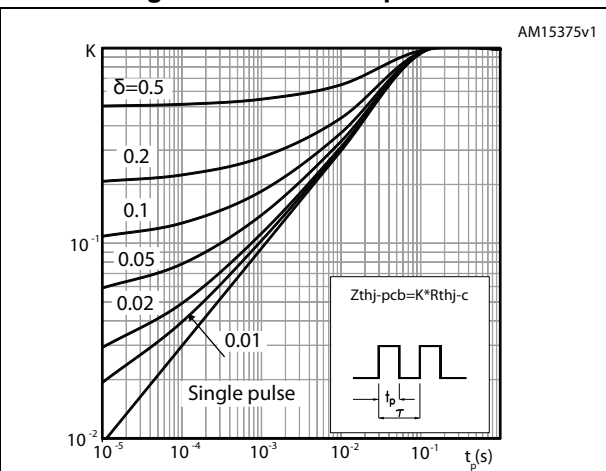


Figure 4. Output characteristics

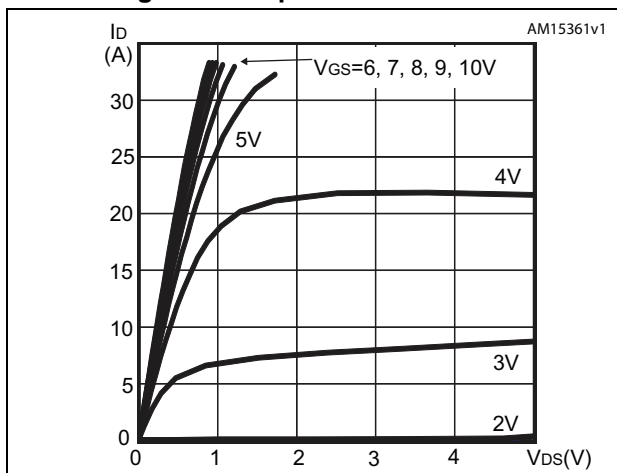


Figure 5. Transfer characteristics

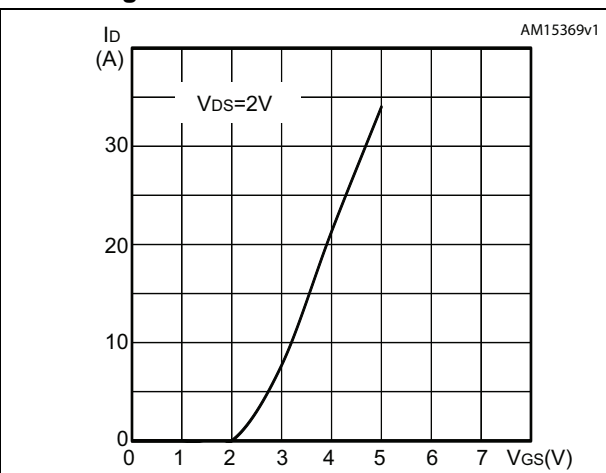


Figure 6. Gate charge vs gate-source voltage

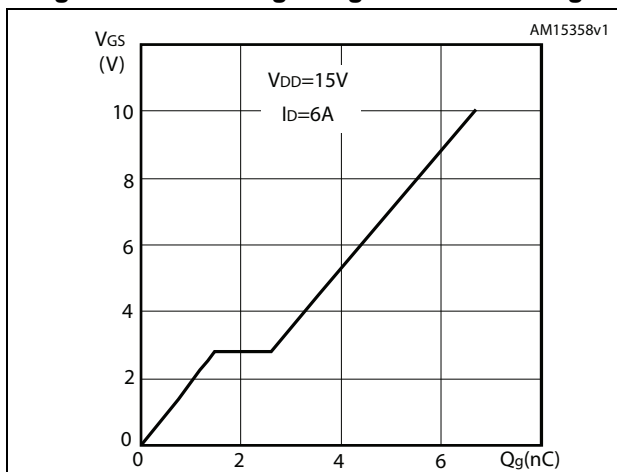


Figure 7. Static drain-source on-resistance

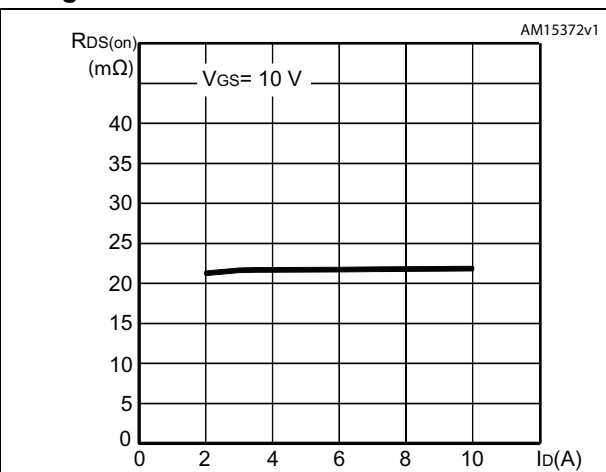


Figure 8. Capacitance variations

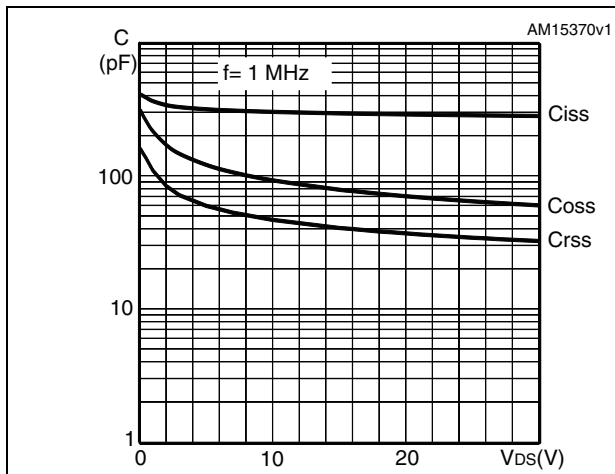


Figure 9. Normalized on-resistance vs temperature

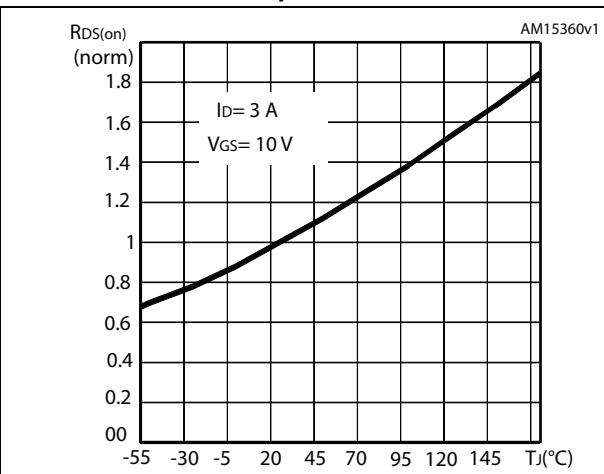


Figure 10. Normalized gate threshold voltage vs temperature

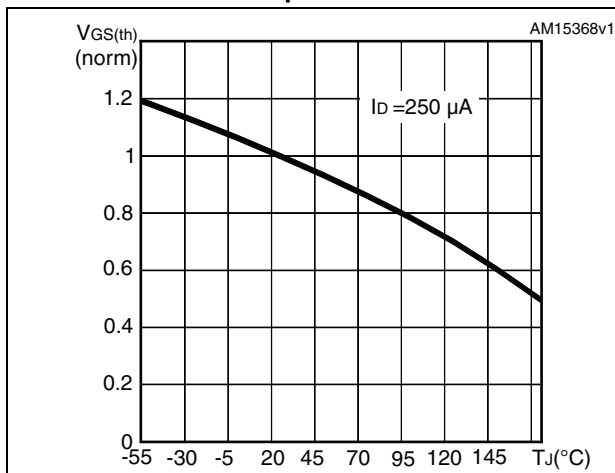


Figure 11. Normalized V<sub>(BR)DSS</sub> vs temperature

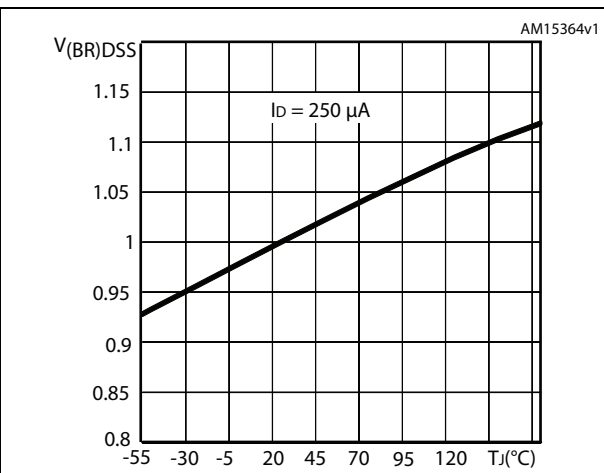
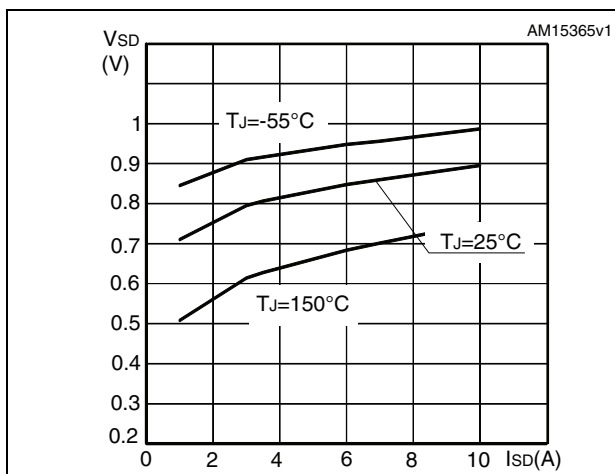


Figure 12. Source-drain diode forward characteristics



### 3 Test circuits

Figure 13. Switching times test circuit for resistive load



Figure 14. Gate charge test circuit

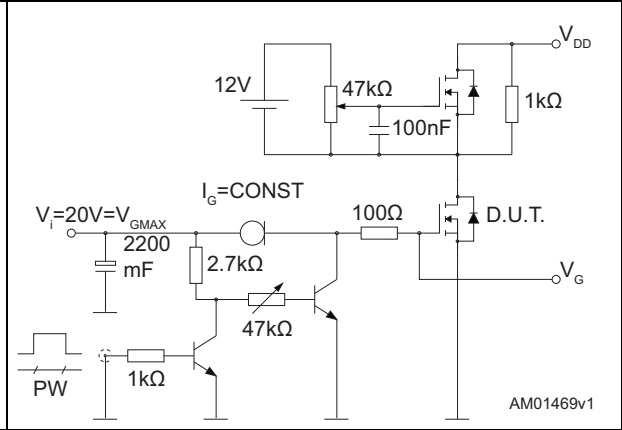


Figure 15. Test circuit for inductive load switching and diode recovery times



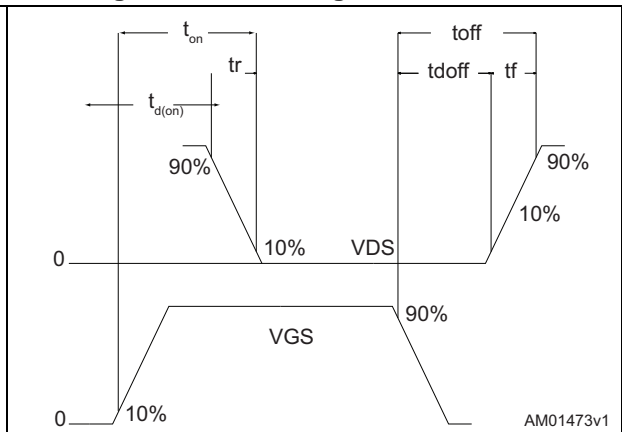
Figure 16. Unclamped inductive load test circuit



Figure 17. Unclamped inductive waveform



Figure 18. Switching time waveform

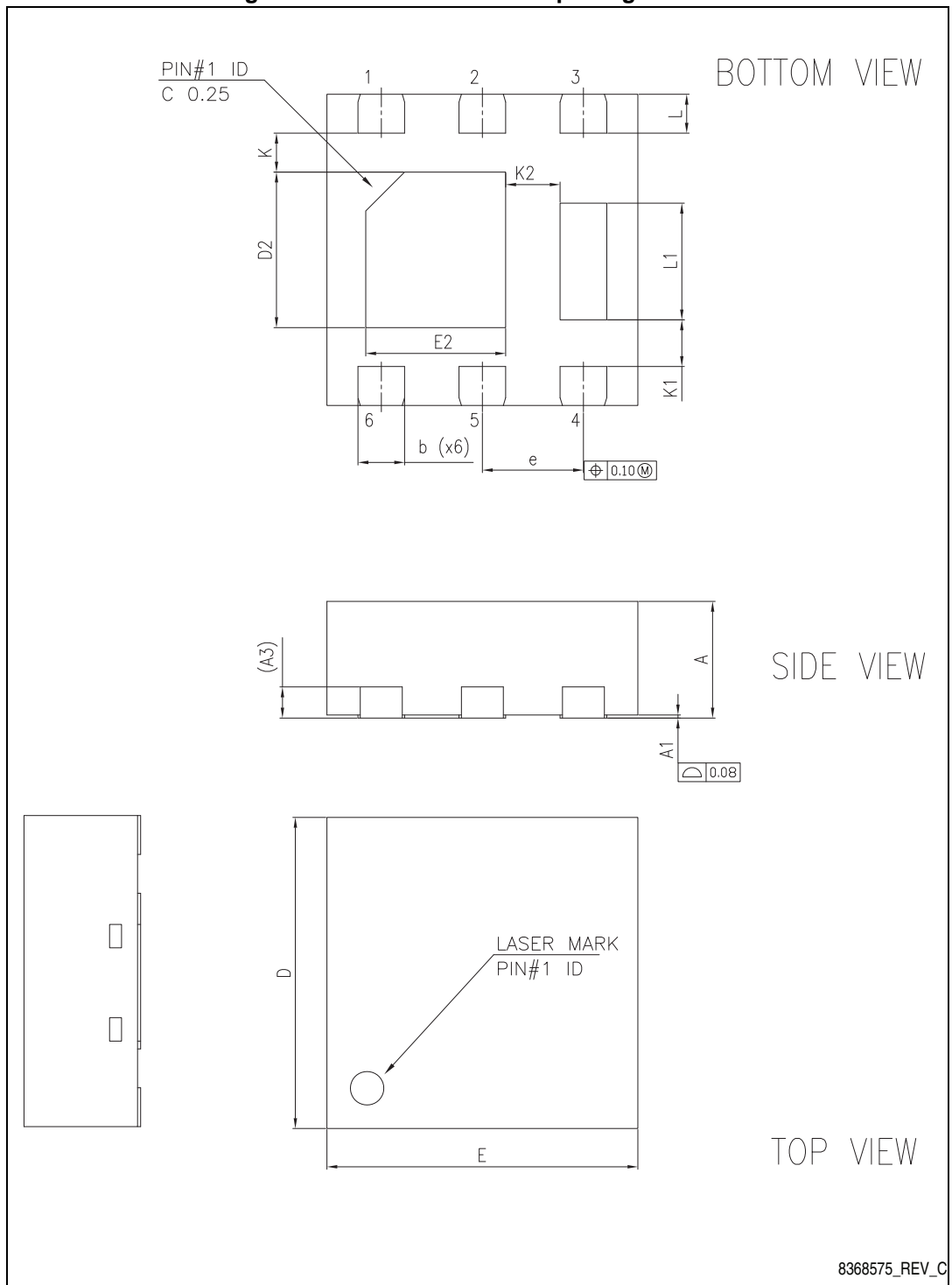




## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

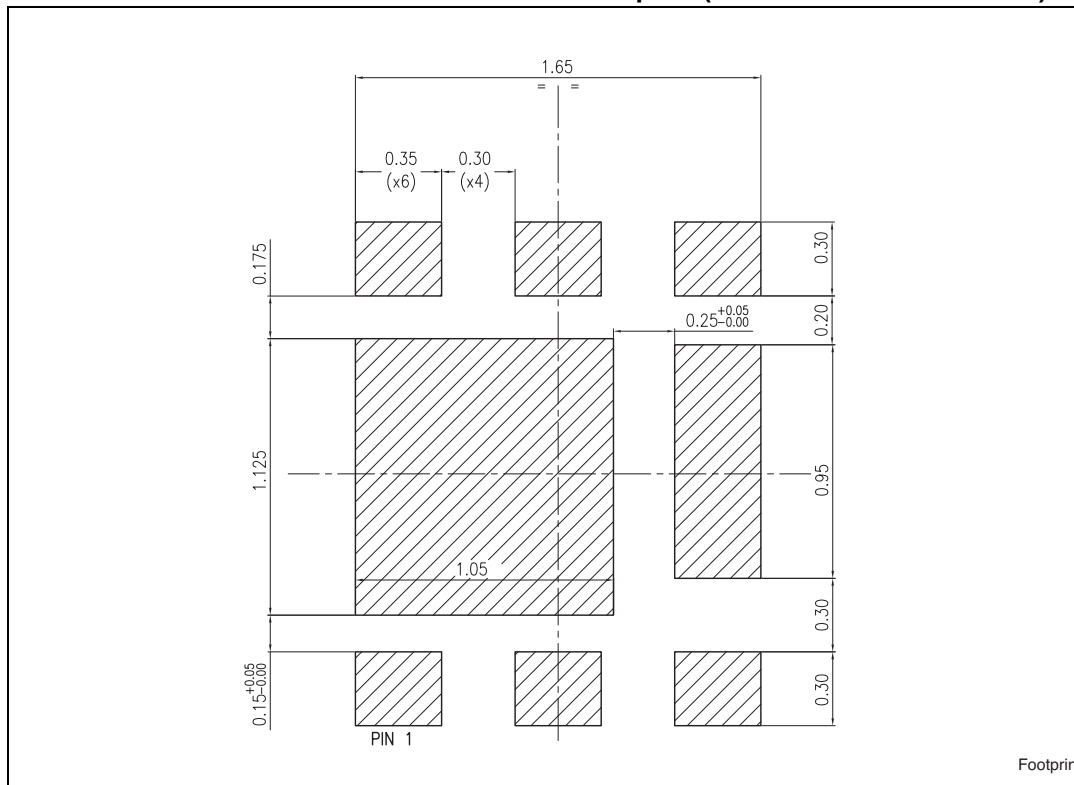
Figure 19. PowerFLAT™ 2 x 2 package outline



**Table 8. PowerFLAT™ 2 x 2 package mechanical data**

| Dim. | mm.  |      |      |
|------|------|------|------|
|      | Min. | Typ. | Max. |
| A    | 0.70 | 0.75 | 0.80 |
| A1   | 0.00 | 0.02 | 0.05 |
| A3   |      | 0.20 |      |
| b    | 0.25 | 0.30 | 0.35 |
| D    | 1.90 | 2.00 | 2.10 |
| E    | 1.90 | 2.00 | 2.10 |
| D2   | 0.90 | 1.00 | 1.10 |
| E2   | 0.80 | 0.90 | 1.00 |
| e    | 0.55 | 0.65 | 0.75 |
| K    | 0.15 | 0.25 | 0.35 |
| K1   | 0.20 | 0.30 | 0.40 |
| K2   | 0.25 | 0.35 | 0.45 |
| L    | 0.20 | 0.25 | 0.30 |
| L1   | 0.65 | 0.75 | 0.85 |

**Table 9. PowerFLAT™ 2 x 2 recommended footprint (dimensions in millimeters)**



## 5 Revision history

**Table 10. Document revision history**

| Date        | Revision | Changes   |
|-------------|----------|---|
| 25-May-2012 | 1        | First release   |
| 11-Oct-2012 | 2        | <ul style="list-style-type: none"><li>– Added Section 2.1: Electrical characteristics (curves).</li><li>– <math>R_{DS(on)}</math> values (typ. and max.) updated</li><li>– Typical values updated in Table 5, 6 and 7</li><li>– Minor text changes.</li></ul>   |
| 21-Oct-2015 | 3        | <ul style="list-style-type: none"><li>– Updated title and description in cover page.</li><li>– Datasheet promoted from preliminary data to production data.</li><li>– Updated <a href="#">Table 2</a>, <a href="#">Table 4</a>, <a href="#">Table 5</a> and <a href="#">Table 7</a>.</li><li>– Updated <a href="#">Figure 6</a> and <a href="#">Figure 7</a>.</li><li>– Minor text changes.</li></ul> |

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