Datasheet

(DOC No. XXXXXXXX)

HX5330
LC Lens Driver

Version 2.0 March 2021

Himax Technologies, Inc.
http://www.himax.com.tw

Datasheet

HX5330

LC Lens Driver

Overview:

The HX5330 is three channels LC Lens driver containing a step-up converter which provides for programmable output voltages to drive the LC Lens with a sufficient voltage. The HX5330 can be operated with 6-bit resolution D/A converter for setting the driver operating voltage up to 15V.

info@liqxtal.com

Revision History

Revision	Date	Revision Description	Originator(s)
Version 1.0	09/29/2020	Initial release.	CC Chen
Version 1.1	10/06/2020	Modify title font size and remove table.	CC Chen
Version 1.2	01/25/2021	All updated.	CC Chen
Version 2.0	03/23/2021	All updated for public version.	CC Chen

info@liqxtal.com

Table of Contents

info@liqxtal.com

info@liqxtal.com

List of Figures

info@liqxtal.com

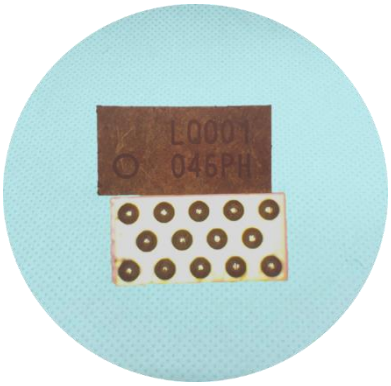
List of Tables

info@liqxtal.com

1. General Description

The HX5330 is three channels LC Lens driver containing a step-up converter which provides for programmable output voltages to drive the LC Lens with a sufficient voltage. The HX5330 can be operated with 6-bit resolution D/A converter for setting the driver operating voltage up to 15V.

2. Features



- VIN input supply voltage range: 2.5V to 3.3V
- Output voltage Maximum is 15V
- Support 6-bit DAC (Digital to Analog Converter)
- 3 channels drivers output for LC diffuser
- Support absence of LC Lens detection (Safety detection)
- Support I^2C programable
- Support GPIO controls output voltage
- Support 8-bit programable AC output frequency (12.8kHz ~ 50Hz)
- 14-pin WLCSP 1.035mm x 2.035 x 0.535mm package

3. Applications

- LC Lens
- Structured-light 3D illuminations

4. Simplified Application Diagram

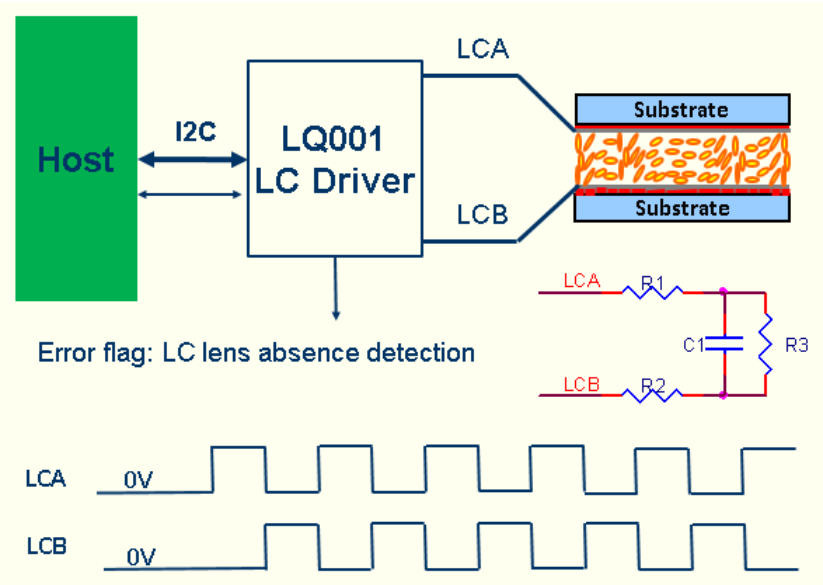


Figure 1 Simplified application diagram

5. Function Block Diagram

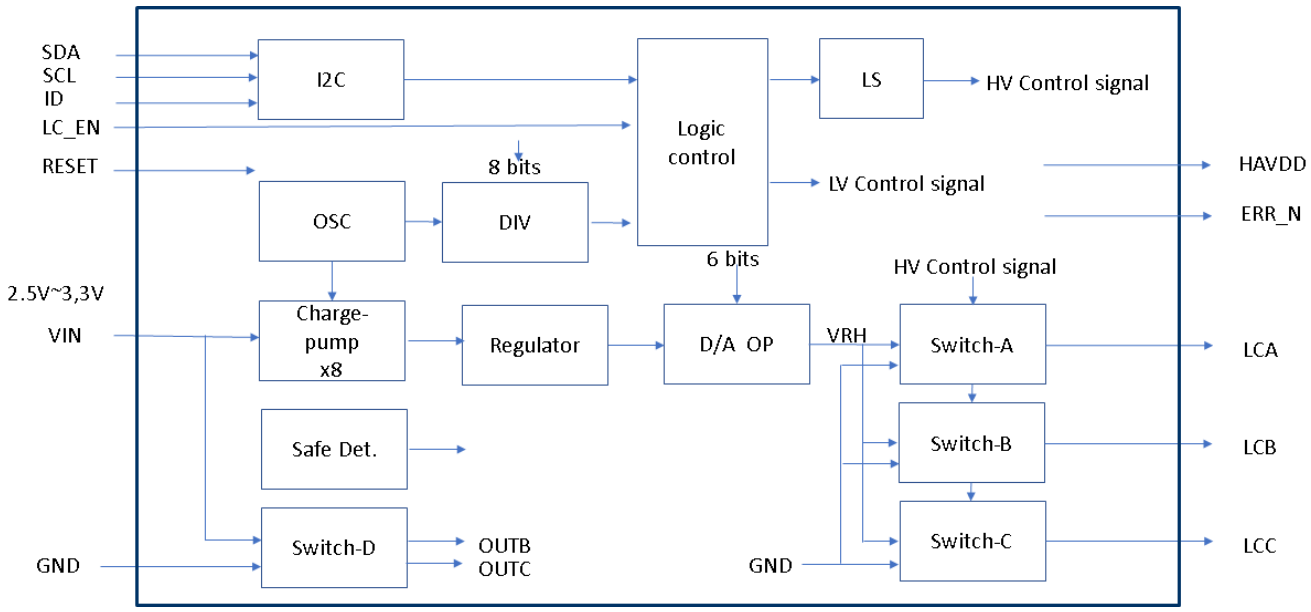


Figure 2 Function block diagram

6. Pin Assignment

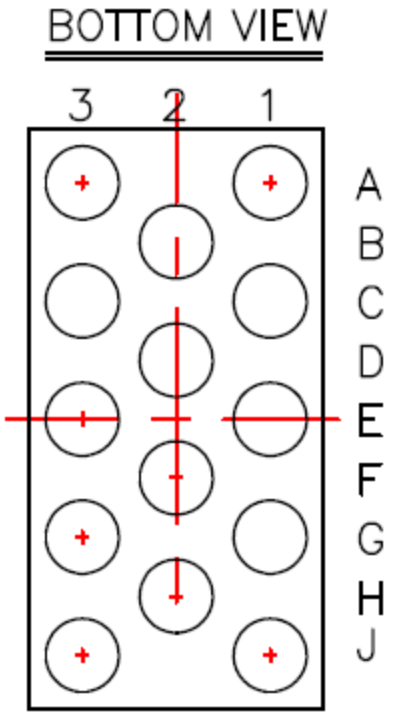


Figure 3 Bottom view

7. Pin Description

P: power pin, G: Ground pin, I: Input pin, O: Output pin, I/O: Inout pin

Pin	Type	Pin name	Description
A1	O	ERR_N	Safety detection flag, Open drain pin, Low is error
C1	I	LC_EN	LC Lens output enable
E1	I	RESET	Reset signal. This pin low for at last 15us
G1	I/O	SDA	I^2C compatible serial data input / output.
J1	I	SCL	I^2C compatible serial clock input.
B2	G	AGND	Analog Power ground
D2	G	AGND	Analog Power ground
F2	G	DGND	Digital Power ground
H2	I	ID	I^2C ID definition (ID=L, I^2C ID=0x74, ID=H I^2C ID=0x75)
A3	P	VIN	Power supply input pin for all the control circuits and step up converter.
C3	P	HAVDD	Step up converter output pin or external power supply.
E3	O	LCA	LC Lens output and safety detection
G3	O	LCB	LC Lens output and safety detection
J3	O	LCC	LC Lens output

8. DC Characteristics

8.1 Absolute maximum rating

Parameter		Spec.			Unit
		Min.	Typ.	Max.	
VIN, SDA, SCL, RESET, LC_EN, ERR_N, ID		-0.3	-	3.6	V
HAVDD to GND		-0.3	-	18	V
LCA, LCB, LCC to GND		-0.3	-	18	V
ESD susceptibility	HBM **(Human Body Mode)**(1)	2	-	-	KV
	MM **(Machine Mode)**(2)	200	-	-	V
Storage temperature range		-40	-	125	°C
Lead temperature **(soldering, 10 sec)**		-	-	260	°C

Note: (1) HBM follow test standard: MIL-STD-883C Method 3015.7.

(2) MM follow test standard: EIAJ-IC-121 Method 20.

8.2 Recommended operating rating

VIN=3.3V, GND=0, T_A=25°C, unless otherwise noted.

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Supply Voltage	VIN	2.5		3.3	V
High Voltage Storage Capacitor	C_{HAVDD}		1		µF
Load (Lens) Capacitance	C_{LOAD}		200		pF
Output Frequency	F_{OUT}		1		KHz
Operating temperature range	T_A	-20	-	85	°C

9. Electrical Characteristics

(VIN=3.3V, GND=0V, T_A=25°C, unless otherwise noted.)

Parameter	Condition	Spec.			Unit
		Min.	Typ.	Max.	
VIN quiescent current	no loading	-	2	-	mA
VIN shutdown current	RESET=GND	-	50	-	μA
VIN sleep current	SLEEP_EN="H"	-	500	-	μA
Input logic high voltage	V_{IH}	1.4	-	-	V
Input logic low voltage	V_{IL}	-	-	0.4	V
Output logic low voltage	V_{OL}, R_{pull-H}=4.7KΩ	-	-	0.3	V

9.1 DC/DC converter

(VIN=3.3V, GND=0V, T_A=25°C, unless otherwise noted.)

Parameter	Condition	Spec.			Unit
		Min.	Typ.	Max.	
HAVDD Output voltage	VIN=3.3V, C_{HAVDD}=1uF	0	-	18	V
HAVDD startup time	VIN=3.3V, C_{HAVDD}=1uF, HAVDD=18V, no load	-	10	-	mS
Switching frequency range	Normal mode	-	1.6	-	MHz
Switching frequency range	Sleep mode		80		KHz

9.2 LC diffuser driver

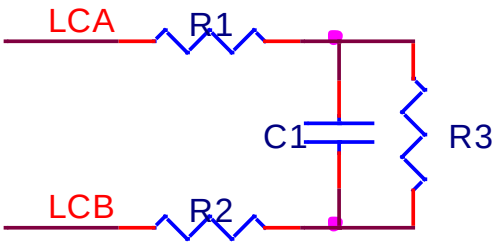
(VIN=3.3V, GND=0V, T_A=25°C, unless otherwise noted.)

Parameter	Condition	Spec.			Unit
		Min.	Typ.	Max.	
Output voltage swing high (V_{max})	LC_EN=H & 0x01h = 0x01h	-	-	15	V
Output voltage swing low	LC_EN=L | 0x01h = 0x00h	0	-	-	V
Output voltage accuracy	VAP[5:0]=0x3Fh	-10	-	+10	%
Output current (*1)	HAVDD=15V, VAP[5:0]=0x3Fh LCA/B/C Output -0.5V	-	-	400	μA

Parameter	Condition	Spec.			Unit
		Min.	Typ.	Max.	
	HAVDD=15V, VAP[5:0]=0x3Fh LCA/B/C Output +0.5V	400	-	-	µA
	HAVDD=15V, VAP[5:0]=0x19h LCA/B/C Output -0.25V	-	-	400	µA
	HAVDD=15V, VAP[5:0]=0x19h LCA/B/C Output +0.25V	400	-	-	µA
Output voltage resolution		-	6	-	Bits
Diffuser driver frequency range		0.05	1	12.8	KHz
Diffuser driver frequency resolution		-	8	-	Bits
Diffuser driver on duty		45	50	55	%
Rising Slew rate (SR) (*2)	LC_EN=H & 0x01h = 0x01h, VAP[5:0] = 0x3Fh Loading capacitor = 470pF	-	5.2	-	V/µS
Rising Slew rate (SR) (*2)	LC_EN=H & 0x01h = 0x01h, VAP[5:0] = 0x3Fh Loading capacitor = 470pF Resistor (R1, R2) = 1KΩ	-	0.35	-	V/uS

Note 1: External HAVDD=15V

Note 2: Loading capacitor (C1) = 470pF, R3 is over few MΩ



9.3 I²C interface

(VIN=3.3V, GND=0, T_A=25°C, unless otherwise noted.)

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
I²C timing characteristics						
Low level input voltage	V_{IL}	VIN=2.5V~3.3V	-	-	0.4	V
High level input voltage	V_{IH}	VIN=2.5V~3.3V	1.4	-	-	V
Serial-clock frequency	F_{SCL}	-	1	-	1000	KHz
Bus free time between STOP and START conditions	T_{BUF}	F_{SCL}=1000KHz	0.4	-	-	µs
		F_{SCL}=400KHz	1.3	-	-	µs
Hold time **(Repeated)** START condition	T_{HD_STA}	F_{SCL}=1000KHz	0.4	-	-	µs
		F_{SCL}=400KHz	0.6	-	-	µs
SCL pulse-width low	T_{LOW}	F_{SCL}=1000KHz	0.4	-	-	µs
		F_{SCL}=400KHz	1.3	-	-	µs
SCL pulse-width high	T_{HIGH}	F_{SCL}=1000KHz	0.4	-	-	µs
		F_{SCL}=400KHz	0.6	-	-	µs
Setup time for a repeated START condition	T_{SU_STA}	F_{SCL}=1000KHz	0.4	-	-	µs
		F_{SCL}=400KHz	0.6	-	-	µs
Data hold time	T_{HD_DAT}	F_{SCL}=1000KHz	0	-	500	ns
		F_{SCL}=400KHz	0	-	900	ns
Data setup time	T_{SU_DAT}	F_{SCL}=1000KHz	100	-	-	ns
		F_{SCL}=400KHz	100	-	-	ns
SDA and SCL receiving rise time	T_R	F_{SCL}=1000KHz	20+0.1CB(*1)	-	100	ns
		F_{SCL}=400KHz	20+0.1CB(*1)	-	300	ns
SDA and SCL receiving fall time	T_F	F_{SCL}=1000KHz	20+0.1CB(*1)	-	100	ns
		F_{SCL}=400KHz	20+0.1CB(*1)	-	300	ns
SDA transmitting fall time	T_F	F_{SCL}=1000KHz	20+0.1CB(*1)	-	100	ns
		F_{SCL}=400KHz	20+0.1CB(*1)	-	300	ns
Setup time for STOP condition	T_{SU_STO}	F_{SCL}=1000KHz	0.4	-	-	µs
		F_{SCL}=400KHz	0.6	-	-	µs
Bus capacitance	CB	-	-	-	400	pF
Pulse width of suppressed spike	T_{SP}	-	0	-	50	ns

Note 1: CB is in pF.

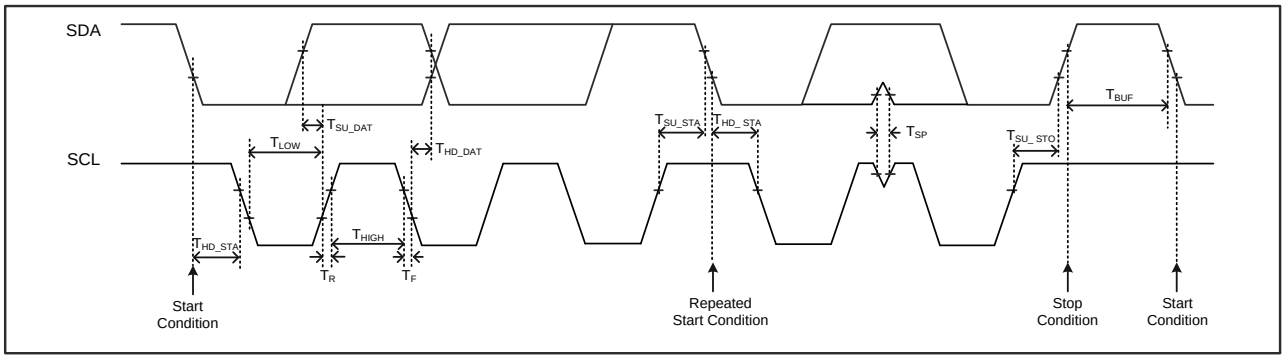


Figure 4 I²C serial-interface timing diagram

10. Function Description

The HX5330 provides I²C programable voltage and frequency AC driving output. It also supports absence LC Lens detection and heater function.

10.1 Digital to analog converter (DAC)

The HX5330 includes **6-bit** Digital to analog converter (DAC). The DAC can support 0V to V_{max} = 15V, VAP[5:0] = decimal equivalent (0~63) of the binary code that is loaded to the DAC register. Determining the output voltage use the following equation:

Output Voltage: $V_{AA} = (V_{max}/64) * (VAP[5:0] + 1)$

10.2 I²C protocol

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW.

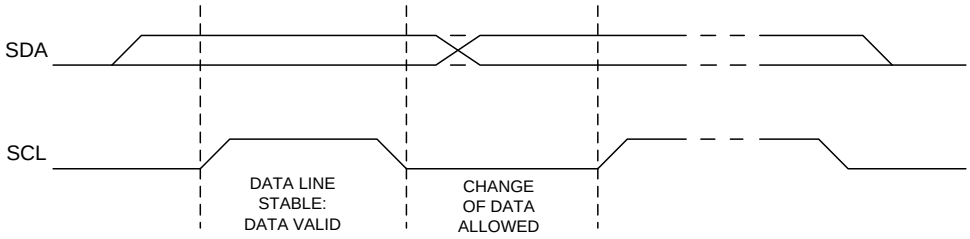


Figure 5 I²C Signal Timing

Within the procedure of the I²C-bus, unique situations arise which are defined as START and STOP conditions. A HIGH to LOW transition on the SDA line while SCL is HIGH is one such unique case. This situation indicates a START condition. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition. START and STOP conditions are always generated by the master. The I²C bus is considered to be busy after the START condition. The I²C bus is considered to be free again a certain time after the STOP condition.

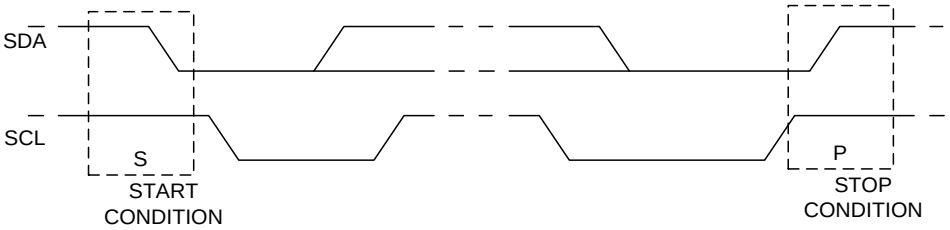


Figure 6 I²C Start/Stop

Every byte put on the SDA line must be 8-bits long. The number of bytes that can be transmitted per transfer is unrestricted. Each byte has to be followed by an acknowledge bit. Data is transferred with the most significant bit (MSB) first.

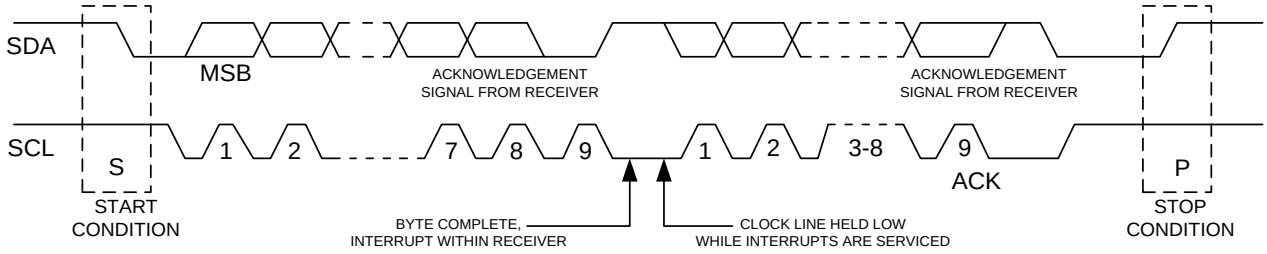


Figure 7 I²C Data Transfer

10.2.1 I²C protocol definition

S	START
AS	ACK SLAVE
AM	ACK MASTER
NA	NO ACK
P	STOP

10.2.2 I²C slave address

HX5330 has two slave address could be select by setting HW pin “ID”. The slave address of I²C selected by ID pin is defined a follow table.

Table 1 Slave Address Table

ID	Slave address (A6-A0)
0	1110100
1	1110101

10.2.2 Write-mode

S	Device address								AS	Register address	AS	First data **(8-bit)**	AS	…	Last data (8-bit)	AS	P
	1	1	1	0	1	0	ID	0		Start address							

10.2.3 Read-mode

<table>
<tr><td rowspan="2">S</td><td colspan="8">Device address</td><td rowspan="2">AS</td><td>Register address</td><td rowspan="2">AS</td><td rowspan="2">P</td><td rowspan="2">S</td><td rowspan="2">1</td><td rowspan="2">1</td><td rowspan="2">1</td><td rowspan="2">0</td><td rowspan="2">1</td><td rowspan="2">0</td><td rowspan="2">ID</td><td rowspan="2">1</td><td rowspan="2">AS</td><td rowspan="2">First data (8-bit)</td><td rowspan="2">AM</td><td rowspan="2">…</td><td rowspan="2">Last data (8-bit)</td><td rowspan="2">NA</td><td rowspan="2">P</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>ID</td><td>0</td><td>Start address</td></tr>
</table>

10.3 I²C command list and description

Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial code
0x00h	W/R	0	1	0	1	1	0	1	0	0x00h
0x01h	W/R	Sleep_EN	LCEN_DIS	Safety_EN	Over_drive	LCBPIN_DS	LCCPIN_EN	LCCOUT_EN	Spot_EN	0x01h
0x02h	R	-	-	-	-	-	-	ERR_FG	MOD	0x00h
0x03h	R/W	-	-	Output Voltage VAP[5:0]						0x3Fh
0x04h	R/W	Frequency FAP[7:0]								0x13h
0x05h	R/W	Safety_Dis	Over_Dis	Over drive Voltage VOP[5:0]						0x40h

Figure 8 I²C command list and description

10.3.1 Write protect register address: 0x00h (Default value)

Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial code
		Write Protection								
0x00h	W/R	0	1	0	1	1	0	1	0	0x00h(*1)

Note 1: Programming correct value (**5A**h) to enable registers' access. Please avoid t0 program A5h and 69h which is reserved for test mode.

10.3.2 Control register address: 0x01h (Default value)

Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial code
		Control register								
0x01h	W/R	Sleep_EN	LCEN_DIS	Safety_EN	Over_drive	LCBPIN_DS	LCCPIN_EN	LCCOUT_EN	Spot_EN	0x01h

The below show the controll bit deltail information:

Spot_EN	Output enable
0	LCA, LCB, LCC keep 0V
1	LCA, LCB, LCC enable output (*2)

Note 2: LCA, LCB, LCC output is controled by LC_EN and Spot_EN. Both LC_EN=H and Spot_EN=H control LCA, LCB and LCC output voltage

LCCOUT_EN	LCC Output phase
0	LCC, LCA with the same output phase
1	LCC, LCA with 180° output phase

LCCPIN_EN	LCC Output enable
0	LCC disable output
1	LCC enable output

LCBPIN_DS	LCB Output phase
0	LCB, LCA with 180° output phase
1	LCB, LCA with the same output phase

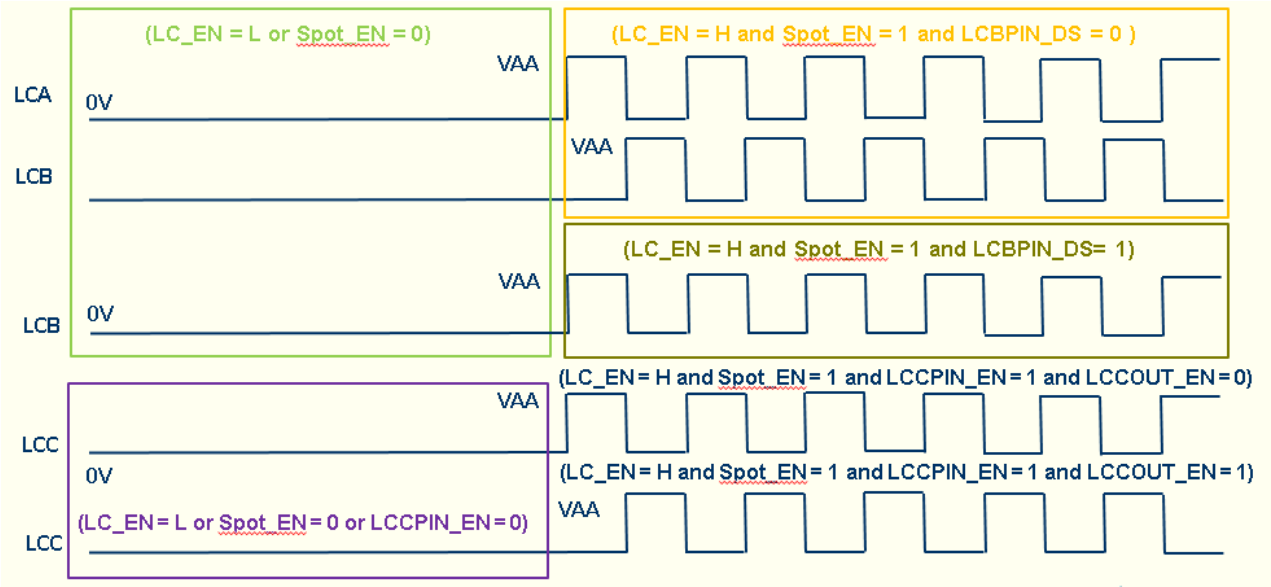


Figure 9 LC_EN, Spot_EN, LCCOUT_EN, LCCPIN_EN, LCBPIN_DS functions

Over_drive	Over drive function enable
0	Disable over drive function
1	Enable over drive function (*3)

Note 3: Over_Drive can be auto clear to 0 by hardware.

Safety_EN	Safety detection function enable
0	Disable safety detection function
1	Enable safety detection function (*4)

Note 4: Safety_EN can be auto clear to 0 by hardware.

LCEN_DIS	Safety detection function enable
0	LC_EN normally function
1	Disable LC_EN function

Sleep_EN	Sleep function enable
0	Normal mode
1	Enter sleep mode

10.3.3 Safety detection status: 0x00h (Default value)

Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial code
		Status								
0x02h	R	-	-	-	-	-	-	ERR_FG	MOD	0x00h

The below show the tatus bit deltail information:

MOD	LCC Output phase
0	LCA, LCB, LCC keep 0V
1	LCA, LCB/LCC has output voltage

ERR_FG	Error detection flag
0	Normally
1	LC Lens damaged

10.3.4 Heater and Output voltage: 0x3Fh (Default value)

Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial code
		-	-	Output Voltage (V_{AA})						
0x03h	R/W	-	-	Output Voltage VAP[5:0]						0x3Fh

The below show the output voltage deltail information:

Output Voltage	D5	D4	D3	D2	D1	D0
V_{AA}	Output Voltage VAP[5:0]					

Output Voltage: $V_{AA} = (V_{max}/64) * (VAP[5:0] + 1)$, $V_{max} = 15V$

10.3.5 Output AC frequency: 0x13h (Default value)

Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial code
		Output AC frequency (f)								
0x04h	R/W	Frequency FAP[7:0]								0x13h

Output frequency: f = (12.8kHz * (FAP[7:0] + 1) / 256), FAP[7:0] = 0x00h, f = 50Hz

10.3.6 Over drive voltage: 0x40h (Default value)

Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial code
		LC_EN Safety disable	Over drive disable	Over drive voltage ($V_{over\ drive}$)						
0x05h	R/W	Safety_ Dis	Over_D is	Over drive Voltage VOP[5:0]						0x40h

The below show the LC_EN trigger to safety detection function deltail information:

Safety_Dis	LC_EN safety disable
0	Normally
1	LC_EN trigger to safety detection function is disable

The below show the Over drive disable function deltail information:

Safety_Dis	LC_EN safety disable
0	Normally
1	Over drive function is disable

The below show the Over drive voltage deltail information:

Over drive Voltage	D5	D4	D3	D2	D1	D0
$V_{over\ drive}$	Over drive Voltage VOP[5:0]					

Over drive voltage: $V_{over\ drive} = (V_{max}/64)^* (VOP[5:0] + 1)$, $V_{max} = 15V$

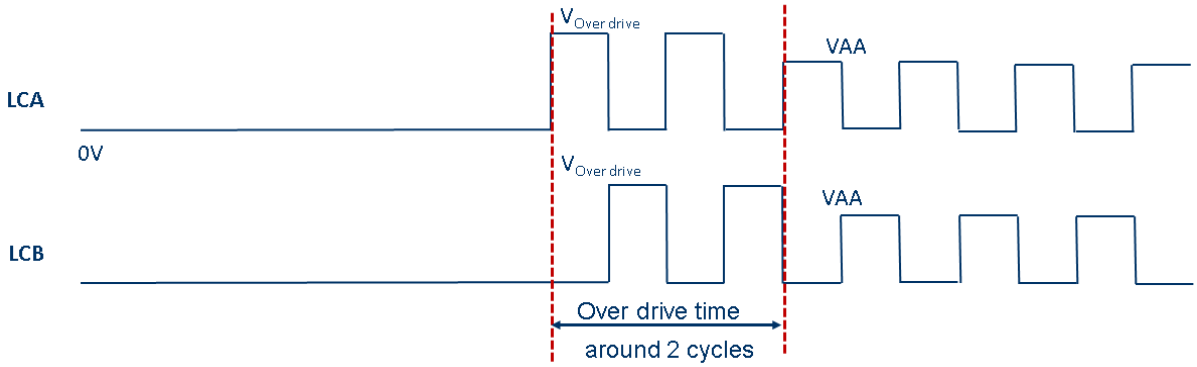


Figure 10 Over drive voltage illustration

11. Application Information

11.1 Operation flow chart

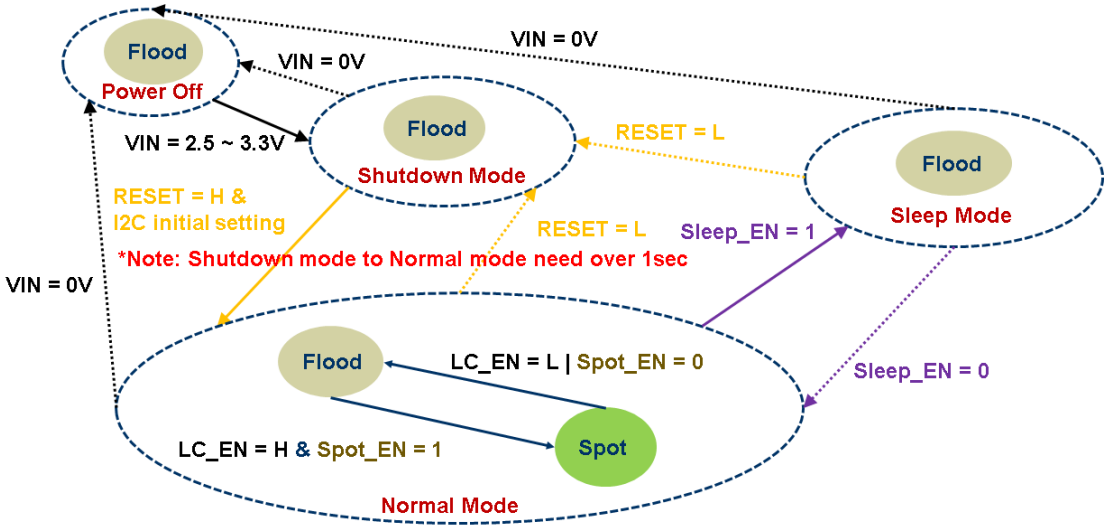


Figure 101 Operation flow chart

11.2 Safety Detection Function

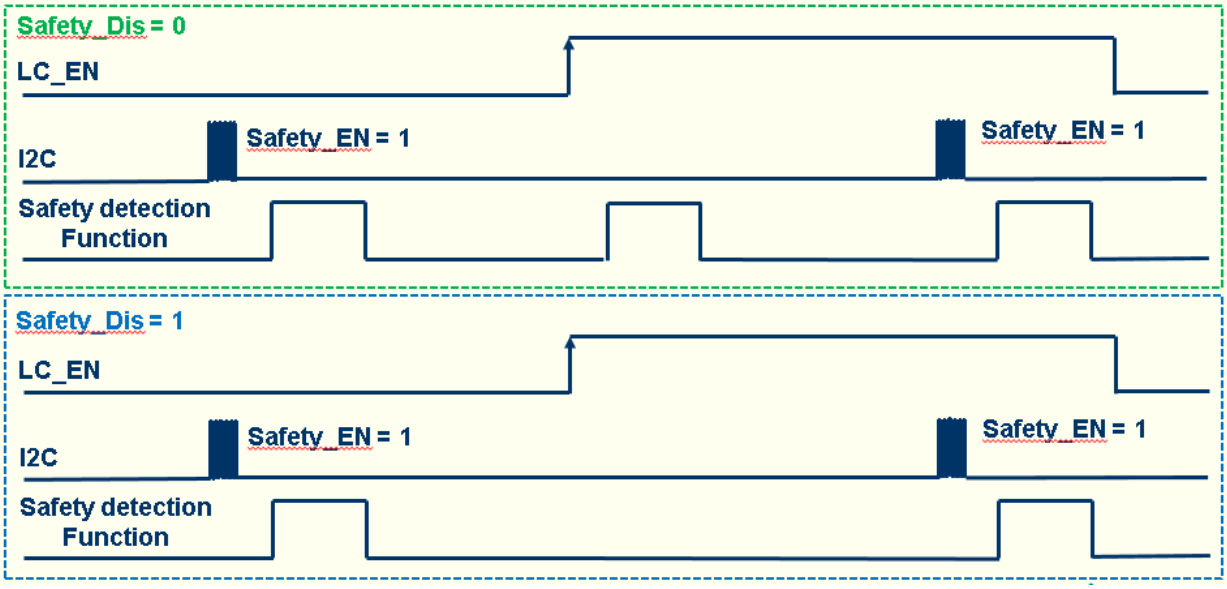


Figure 112 Safety detection function operation

11.3 Over Drive Function

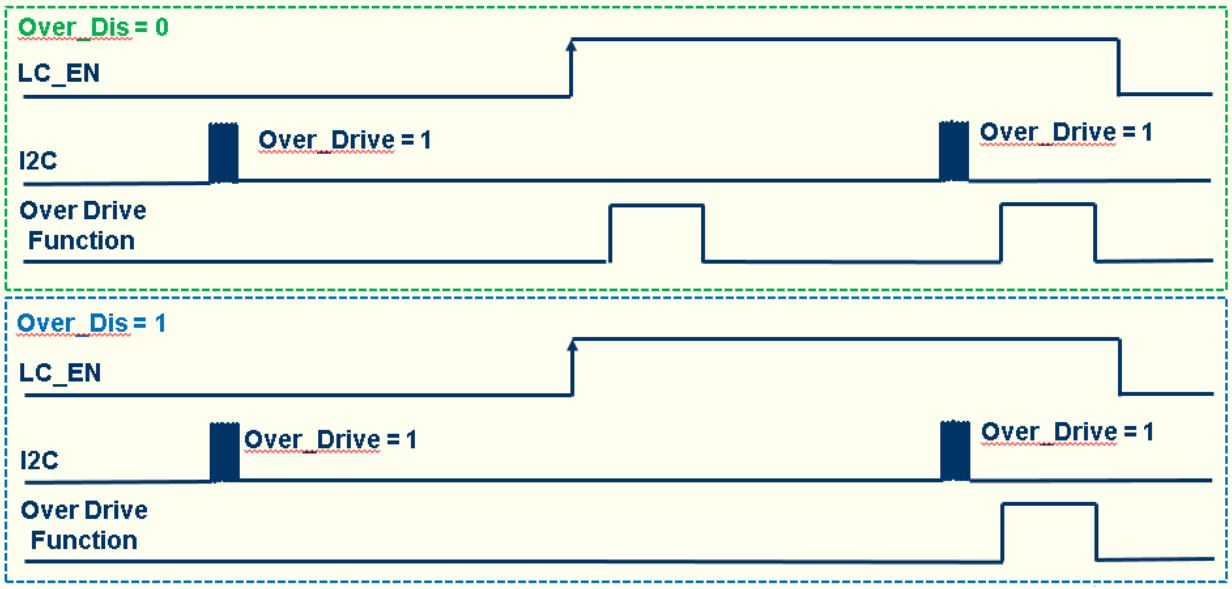


Figure 123 Over drive function operation

11.4 Application Reference Circuit

Case A: without external HAVDD

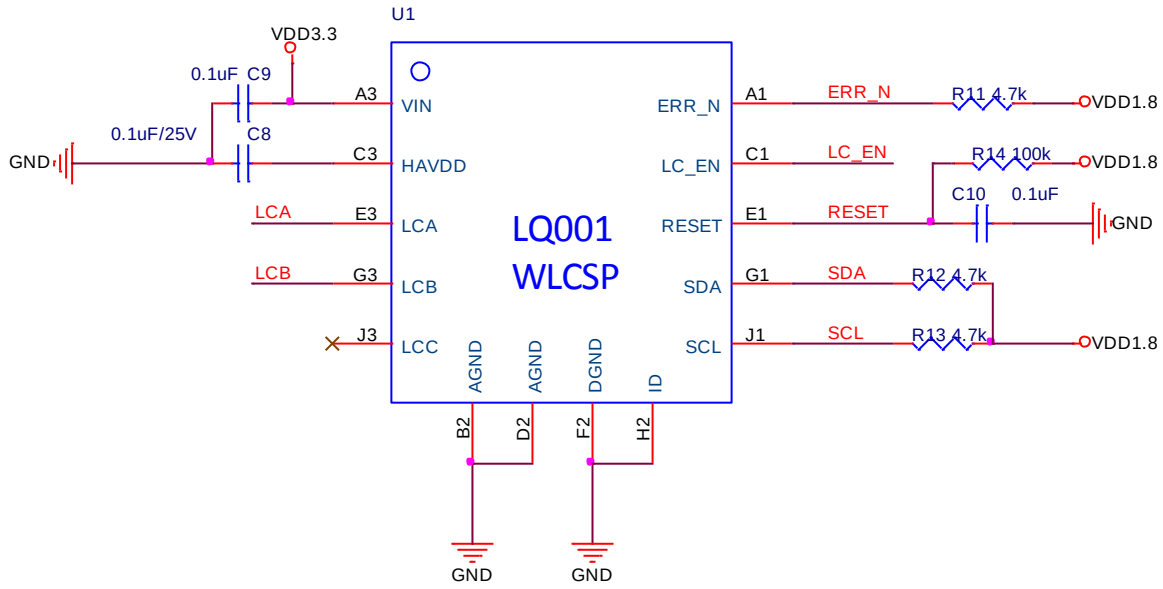


Figure 134 Application circuit (For Load Capacitance < 2uF)

Case B: with external HAVDD (15V)

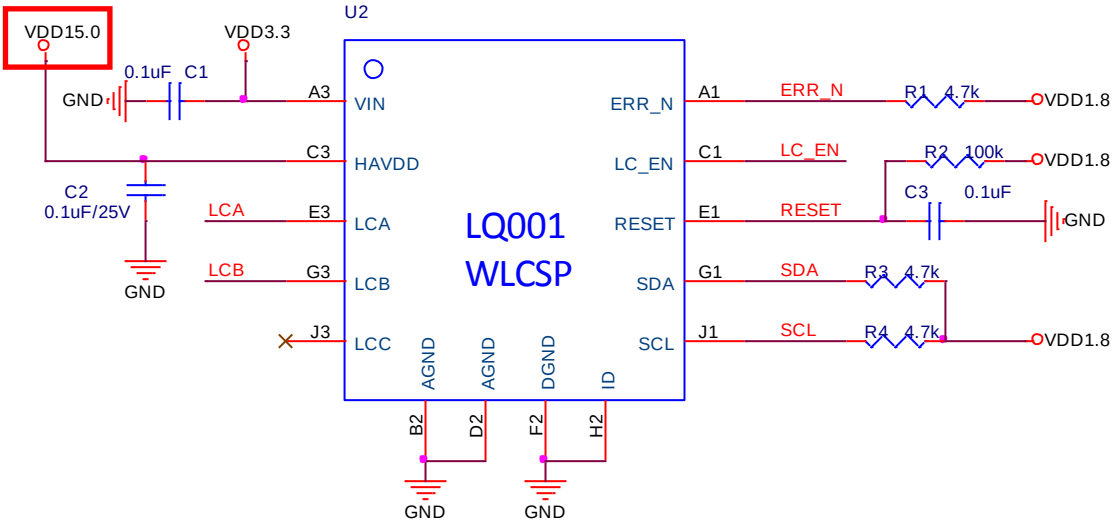


Figure 145 Application circuit (External 15V power)

11.5 Power Sequence

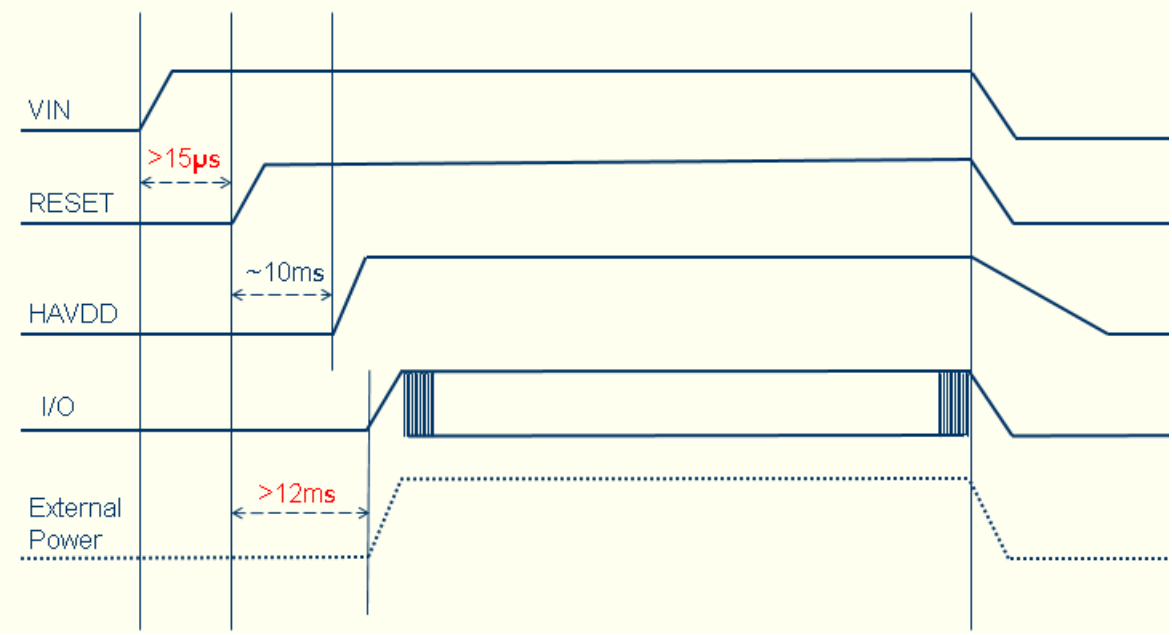


Figure 156 Power sequence

11.6 External Power

If LC Lens's C1 is over 3μF or R1, R2 is over 33kΩ [Fig 17], Please used external power (15V) supply to HAVDD. The external power need follow the power sequence [Fig 16].

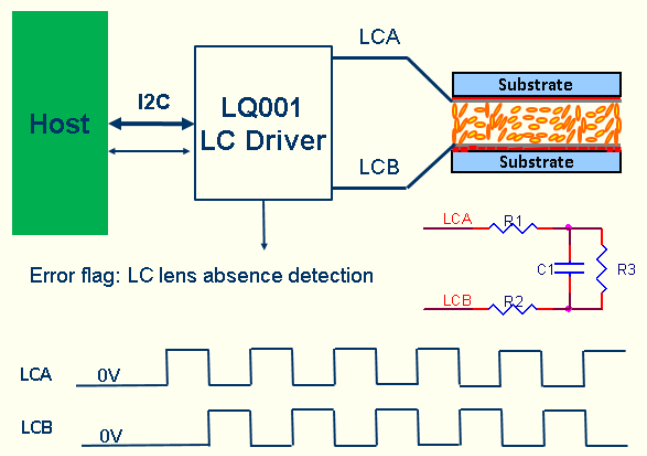
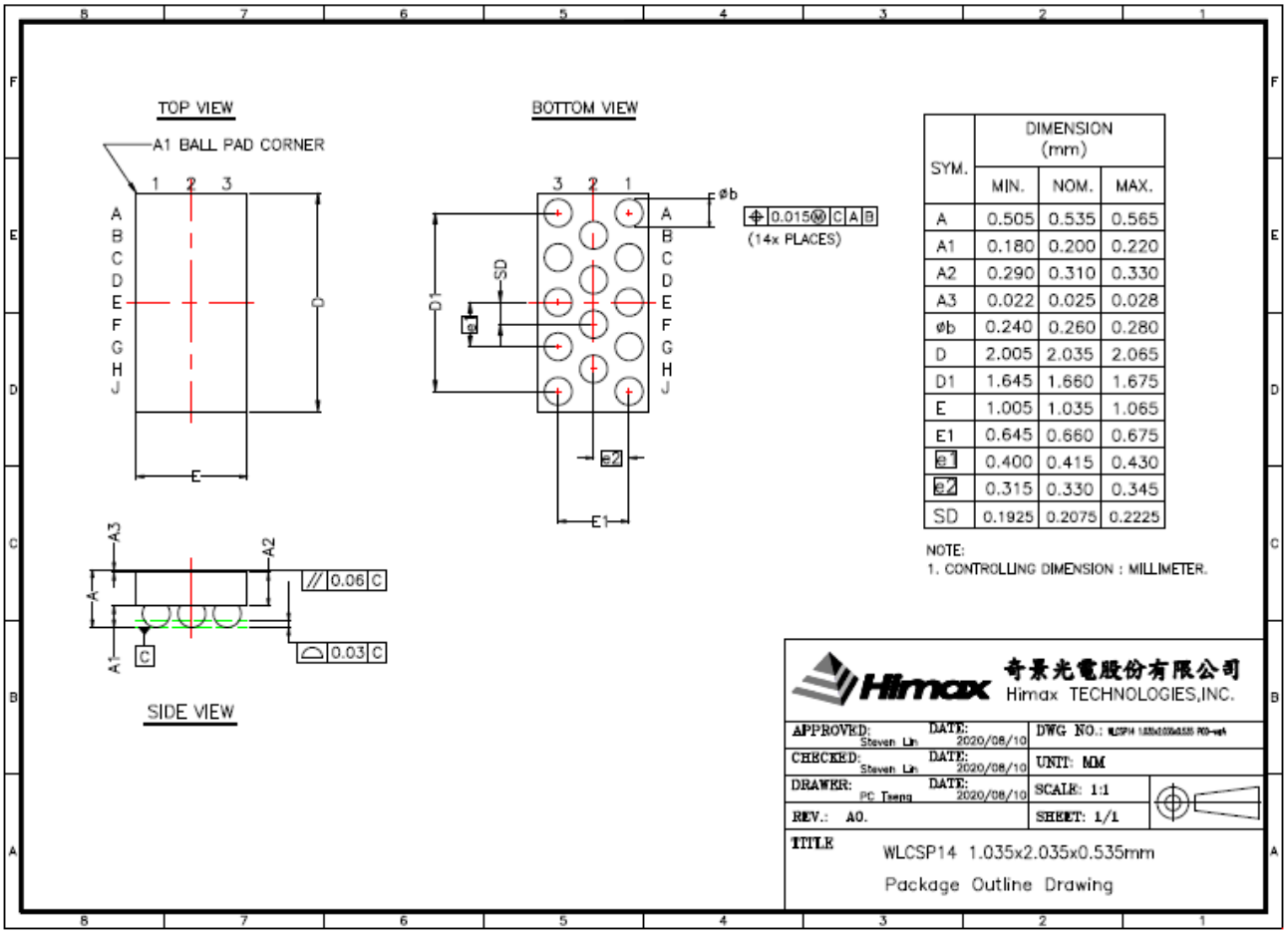


Figure 167 Simplified application diagram with LC Lens RC model

12. Package Outline Dimension



SYM.	DIMENSION (mm)		
	MIN.	NOM.	MAX.
A	0.505	0.535	0.565
A1	0.180	0.200	0.220
A2	0.290	0.310	0.330
A3	0.022	0.025	0.028
øb	0.240	0.260	0.280
D	2.005	2.035	2.065
D1	1.645	1.660	1.675
E	1.005	1.035	1.065
E1	0.645	0.660	0.675
e1	0.400	0.415	0.430
e2	0.315	0.330	0.345
SD	0.1925	0.2075	0.2225

Figure 178 Package Outline Dimension

13. Ordering Information

Part no.	Package
HX5330	WLCSP 14L 1.035x2.035x0.535mm

14. Remarks

HX5330 is also named as LQ001 from Liqxtal technology.