IS61LV256AL

32K x 8 LOW VOLTAGE CMOS STATIC RAM

MARCH 2020

FEATURES

- High-speed access times:
  — 10 ns
- Automatic power-down when chip is deselected
- CMOS low power operation
  — 60 µW (typical) CMOS standby
  — 65 mW (typical) operating
- TTL compatible interface levels
- Single 3.3V power supply
- Fully static operation: no clock or refresh required
- Three-state outputs
- Lead-free available

DESCRIPTION

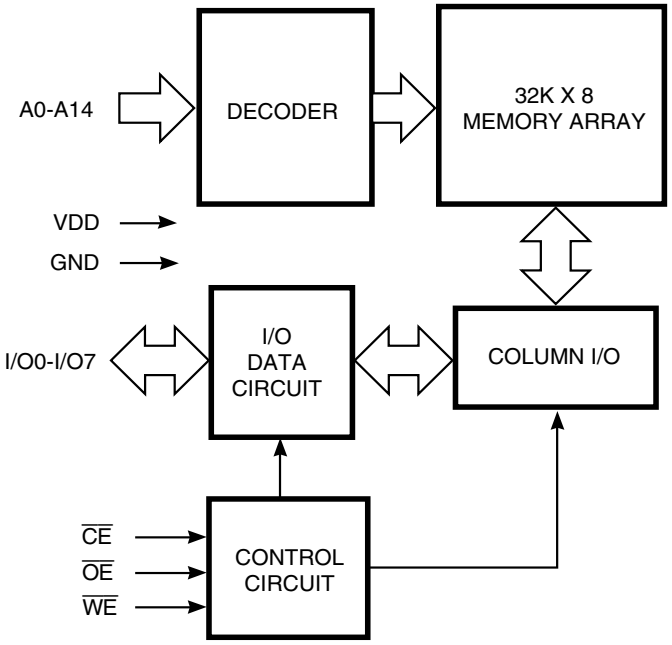
The *ISSI* IS61LV256AL is a very high-speed, low power, 32,768-word by 8-bit static RAM. It is fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields access times as fast as 8 ns maximum.

When $\overline{CE}$ is HIGH (deselected), the device assumes a standby mode at which the power dissipation is reduced to 150 µW (typical) with CMOS input levels.

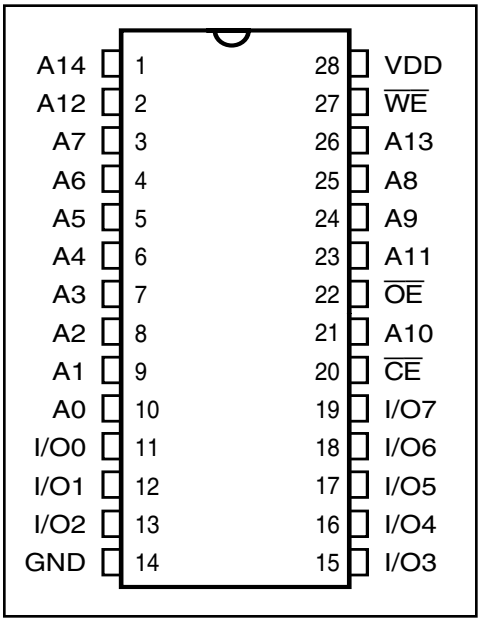
Easy memory expansion is provided by using an active LOW Chip Enable ($\overline{CE}$). The active LOW Write Enable ($\overline{WE}$) controls both writing and reading of the memory.

The IS61LV256AL is available in the JEDEC standard 28-pin, 300-mil SOJ and the 450-mil TSOP (Type I) packages.

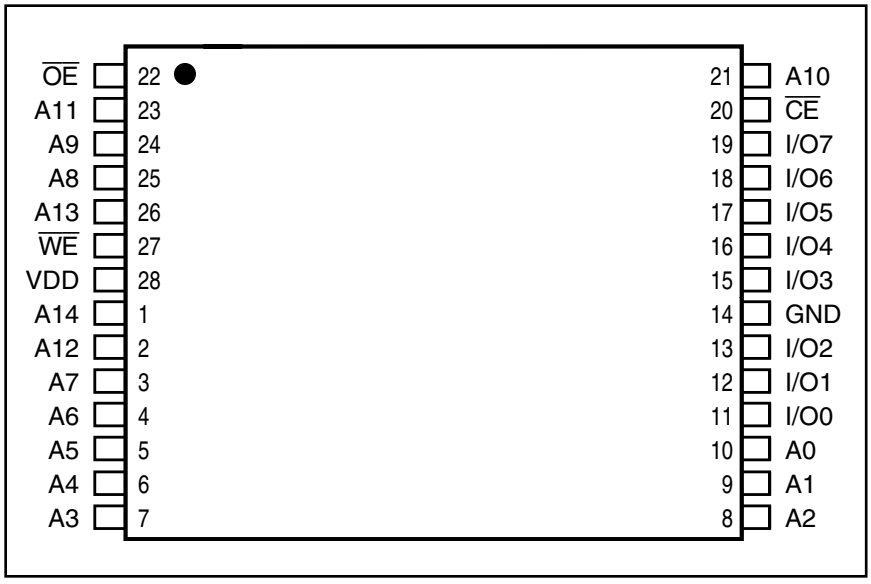
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION
28-Pin SOJ



PIN CONFIGURATION
28-Pin TSOP (Type I)



PIN DESCRIPTIONS

A0-A14	Address Inputs
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
I/O0-I/O7	Input/Output
V_{DD}	Power
GND	Ground

TRUTH TABLE

Mode	$\overline{WE}$	$\overline{CE}$	$\overline{OE}$	I/O Operation	V_{DD} Current
Not Selected (Power-down)	X	H	X	High-Z	I_{SB1}, I_{SB2}
Output Disabled	H	L	H	High-Z	I_{CC}
Read	H	L	L	D_{OUT}	I_{CC}
Write	L	L	X	D_{IN}	I_{CC}

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter	Value	Unit
V_{DD}	Power Supply Voltage Relative to GND	–0.5 to +4.6	V
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +4.6	V
T_{STG}	Storage Temperature	–65 to +150	°C
P_D	Power Dissipation	1	W
I_{OUT}	DC Output Current	±20	mA

Notes:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE

Range	Ambient Temperature	Speed (ns)	V_{DD}[1]
Commercial	0°C to +70°C	10	3.3V, +10%, –5%
Industrial	–40°C to +85°C	10	3.3V + 10%, –5%

Note: 1. If operated at 12ns, V_{DD} range is 3.3V ± 10%.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{DD} = Min., I_{OH} = –2.0 mA		2.4	—	V
V_{OL}	Output LOW Voltage	V_{DD} = Min., I_{OL} = 4.0 mA		—	0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{DD} + 0.3	V
V_{IL}	Input LOW Voltage[1]			–0.3	0.8	V
I_{LI}	Input Leakage	GND ≤ V_{IN} ≤ V_{DD}	Com.	–1	1	µA
			Ind.	–2	2	
I_{LO}	Output Leakage	GND ≤ V_{OUT} ≤ V_{DD}, Outputs Disabled	Com.	–1	1	µA
			Ind.	–2	2	

Notes:
1. V_{IL} (min.) = –0.3V (DC); V_{IL} (min.) = –2.0V (pulse width ≤ 2.0 ns).
   V_{IH} (max.) = V_{DD} + 0.5V (DC); V_{IH} (max.) = V_{DD} + 2.0V (pulse width ≤ 2.0 ns).
2. Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.

POWER SUPPLY CHARACTERISTICS[1] (Over Operating Range)

Sym.	Parameter	Test Conditions		-10 ns Min.	-10 ns Max.	Unit
I_{CC1}	V_{DD} Operating Supply Current	V_{DD} = Max., $\overline{CE}$ = V_{IL} I_{OUT} = 0 mA, f = 1 MHz	Com. Ind.	— —	20 25	mA
I_{CC2}	V_{DD} Dynamic Operating Supply Current	V_{DD} = Max., $\overline{CE}$ = V_{IL} I_{OUT} = 0 mA, f = f_{MAX}	Com. Ind. typ.[2]	— — 20	30 35	mA
I_{SB1}	TTL Standby Current (TTL Inputs)	V_{DD} = Max., V_{IN} = V_{IH} or V_{IL} $\overline{CE}$ ≥ V_{IH}, f = 0	Com. Ind.	— —	1 1	mA
I_{SB2}	CMOS Standby Current (CMOS Inputs)	V_{DD} = Max., $\overline{CE}$ ≥ V_{DD} – 0.2V, V_{IN} ≥ V_{DD} – 0.2V, or V_{IN} ≤ 0.2V, f = 0	Com. Ind. typ.[2]	— — 2	40 50	µA

Notes:
1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.
2. Typical values are measured at V_{DD} = 3.3V, T_A = 25°C and not 100% tested.

CAPACITANCE[1,2]

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	5	pF

Notes:
1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz, V_{DD} = 3.3V.

READ CYCLE SWITCHING CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	-10 ns Min.	-10 ns Max.	-12 ns Min.	-12 ns Max.	Unit
t_{RC}	Read Cycle Time	10	—	12	—	ns
t_{AA}	Address Access Time	—	10	—	12	ns
t_{OHA}	Output Hold Time	2	—	2	—	ns
t_{ACE}	$\overline{CE}$ Access Time	—	10	—	12	ns
t_{DOE}	$\overline{OE}$ Access Time	—	5	—	5	ns
t_{LZOE}[2]	$\overline{OE}$ to Low-Z Output	0	—	0	—	ns
t_{HZOE}[2]	$\overline{OE}$ to High-Z Output	—	5	—	5	ns
t_{LZCE}[2]	$\overline{CE}$ to Low-Z Output	3	—	3	—	ns
t_{HZCE}[2]	$\overline{CE}$ to High-Z Output	—	5	—	6	ns
t_{PU}[3]	$\overline{CE}$ to Power-Up	0	—	0	—	ns
t_{PD}[3]	$\overline{CE}$ to Power-Down	—	10	—	12	ns

Notes:
1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±200 mV from steady-state voltage. Not 100% tested.
3. Not 100% tested.

AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	3 ns
Input and Output Timing and Reference Levels	1.5V
Output Load	See Figures 1 and 2

AC TEST LOADS

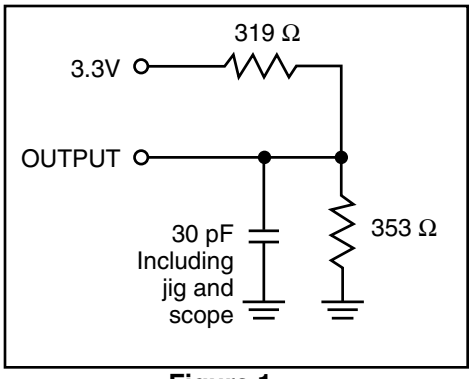


Figure 1.

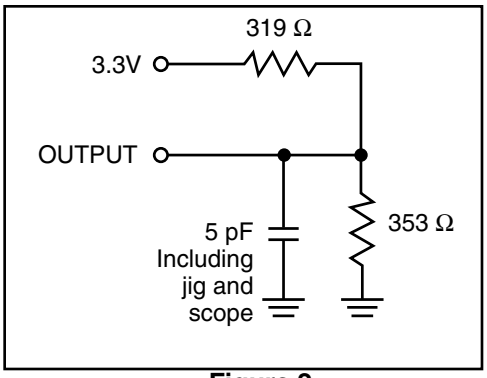
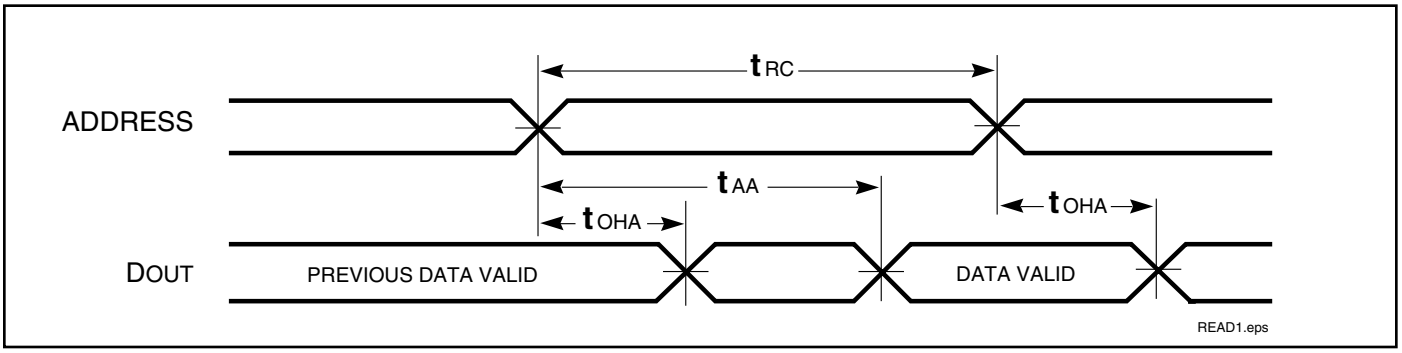


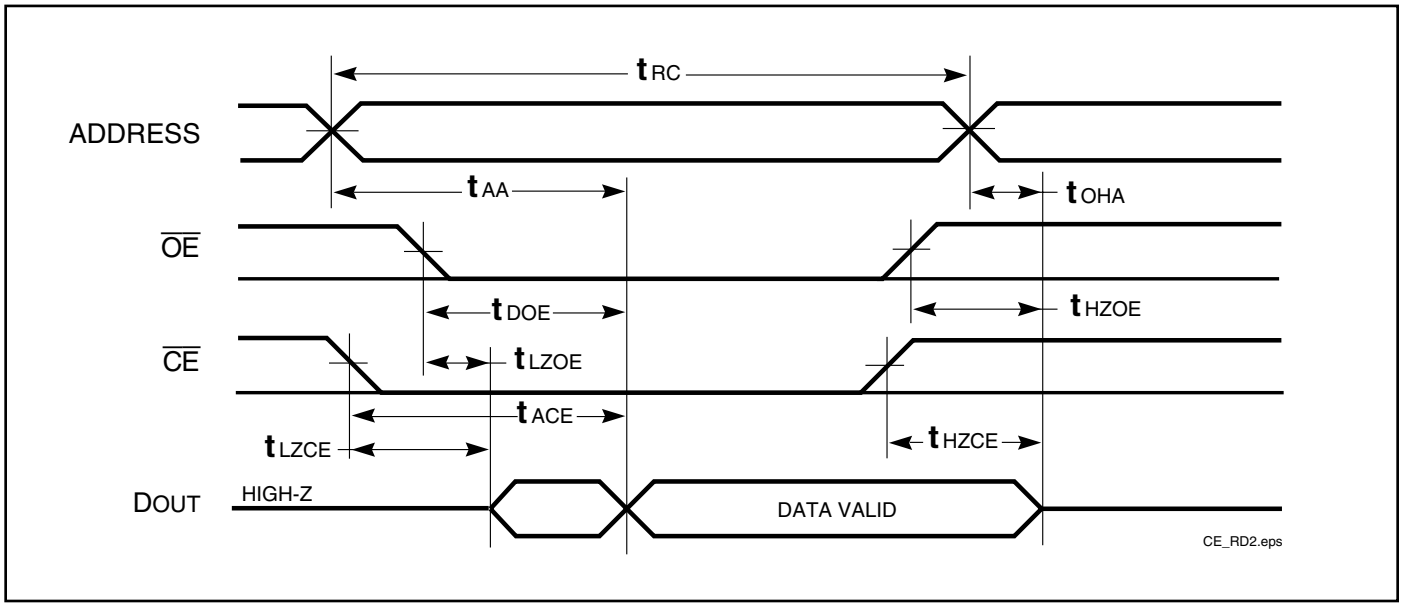
Figure 2.

AC WAVEFORMS

READ CYCLE NO. 1[1,2]



READ CYCLE NO. 2[1,3]



Notes:
1. $\overline{WE}$ is HIGH for a Read Cycle.
2. The device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
3. Address is valid prior to or coincident with $\overline{CE}$ LOW transitions.

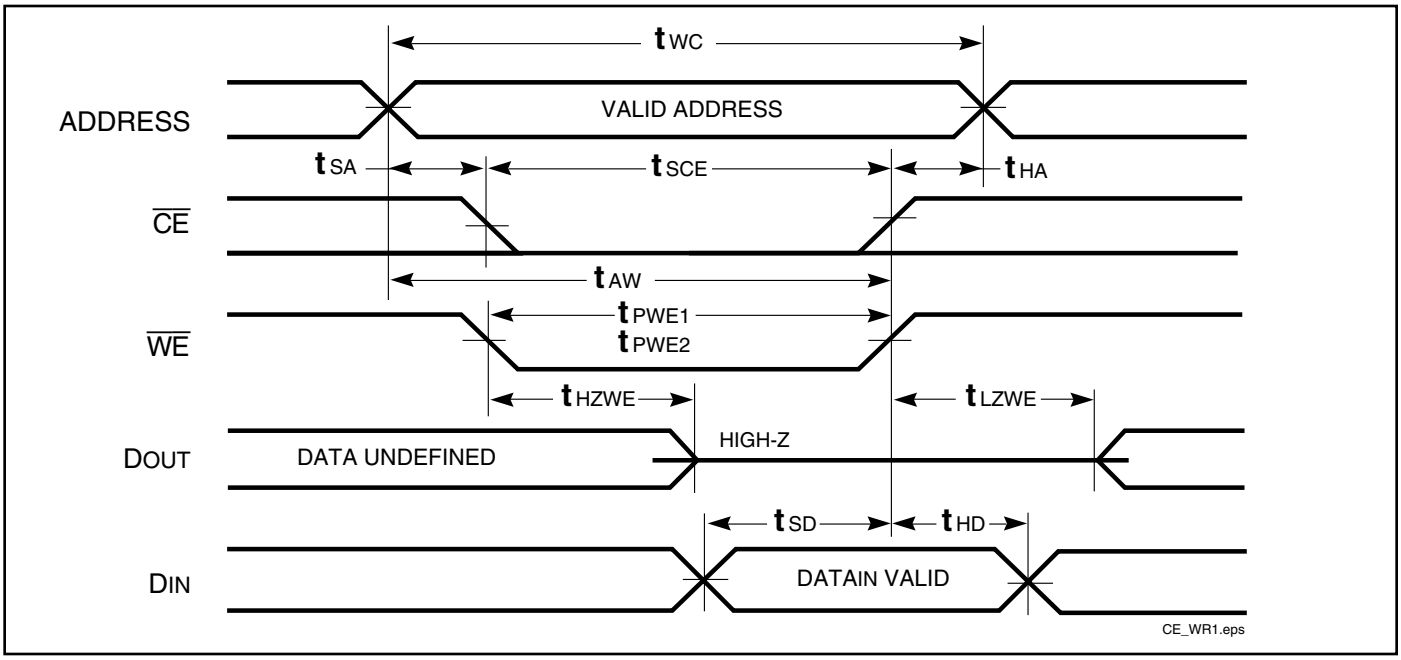
WRITE CYCLE SWITCHING CHARACTERISTICS[1,2] (Over Operating Range)

Symbol	Parameter	-10 ns Min.	-10 ns Max.	-12 ns Min.	-12 ns Max.	Unit
t_{WC}	Write Cycle Time	10	—	12	—	ns
t_{SCE}	$\overline{CE}$ to Write End	8	—	8	—	ns
t_{AW}	Address Setup Time to Write End	8	—	8	—	ns
t_{HA}	Address Hold from Write End	0	—	0	—	ns
t_{SA}	Address Setup Time	0	—	0	—	ns
t_{PWE1}	$\overline{WE}$ Pulse Width ($\overline{OE}$ HIGH)	7	—	8	—	ns
t_{PWE2}	$\overline{WE}$ Pulse Width ($\overline{OE}$ LOW)	10	—	12	—	ns
t_{SD}	Data Setup to Write End	6.5	—	7	—	ns
t_{HD}	Data Hold from Write End	0	—	0	—	ns
t_{HZWE}[3]	$\overline{WE}$ LOW to High-Z Output	—	3.5	—	5	ns
t_{LZWE}[3]	$\overline{WE}$ HIGH to Low-Z Output	0	—	0	—	ns

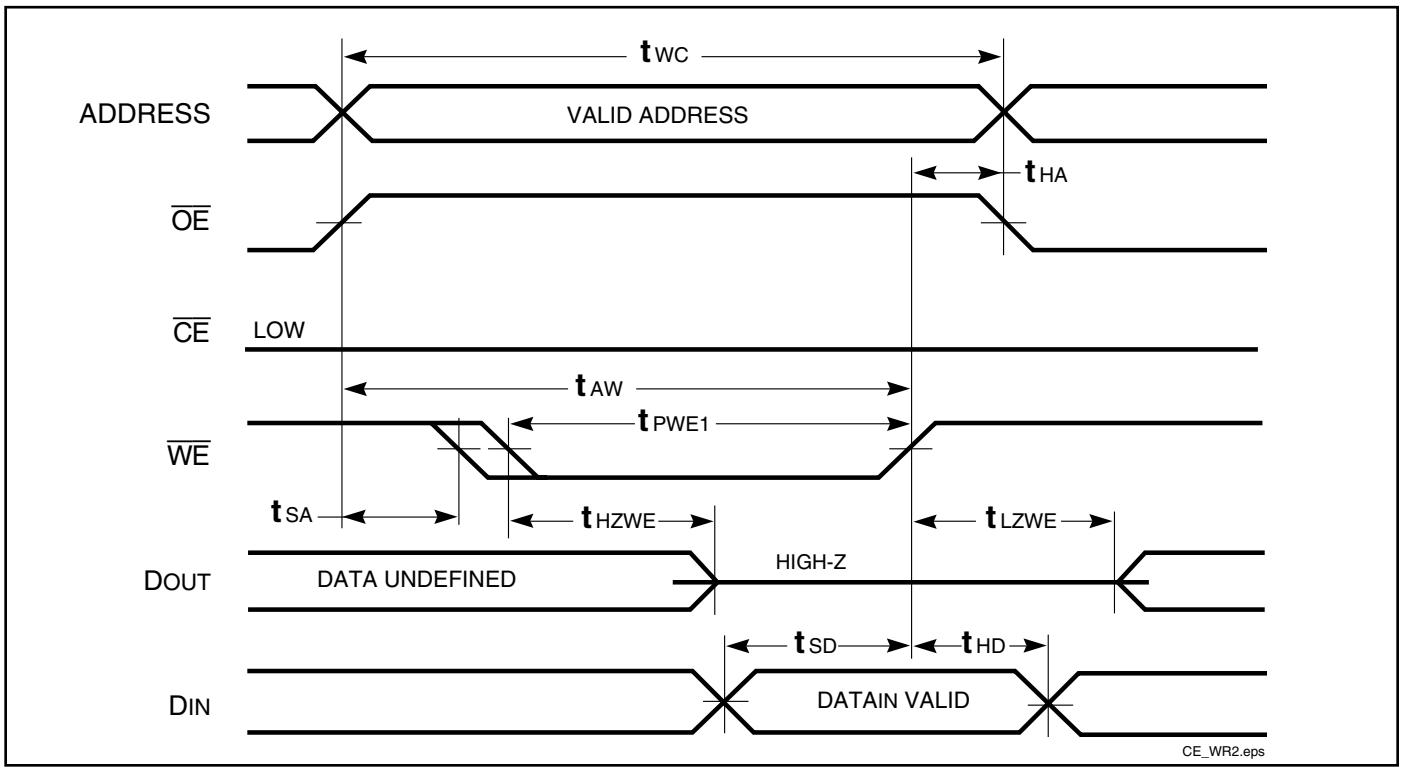
Notes:
1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. The internal write time is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
3. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.

AC WAVEFORMS

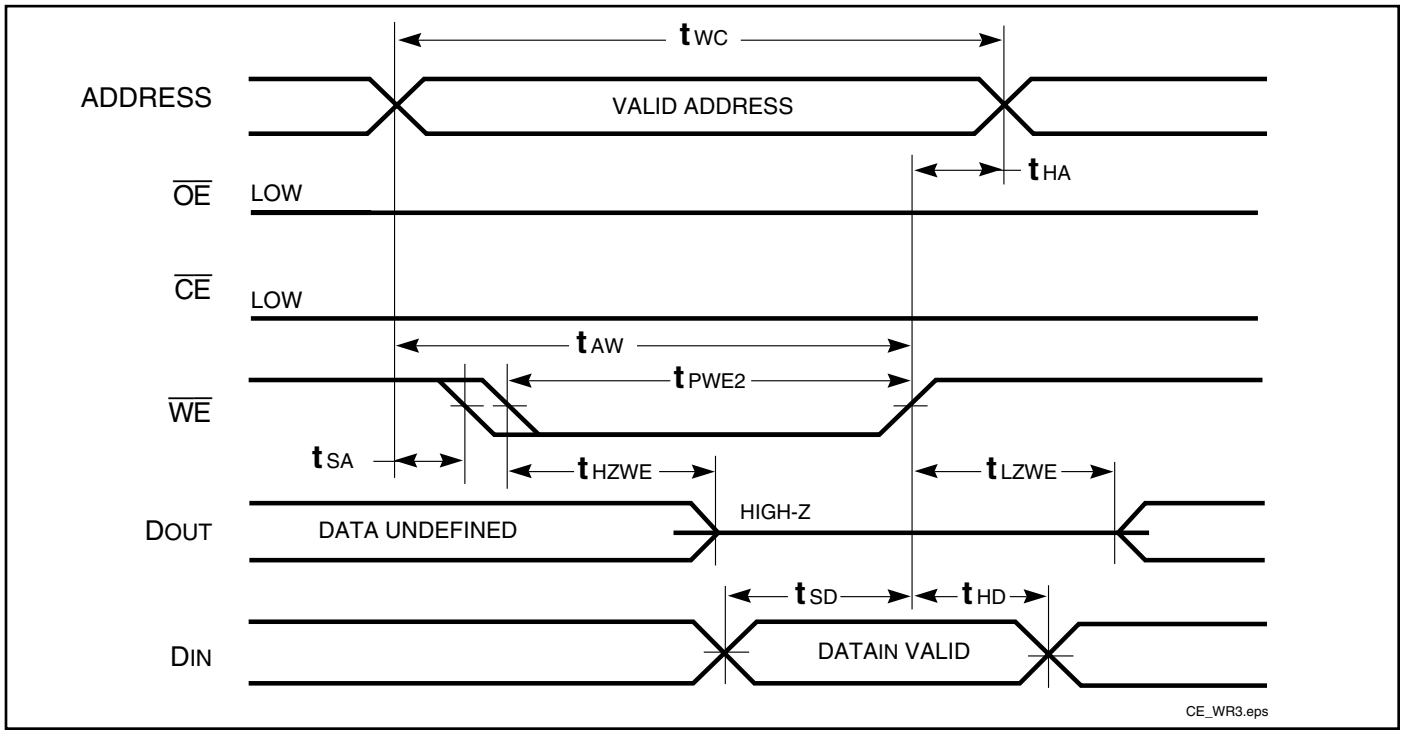
WRITE CYCLE NO. 1 ($\overline{CE}$ Controlled, $\overline{OE}$ is HIGH or LOW) [1]



WRITE CYCLE NO. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ is HIGH During Write Cycle) [1,2]



WRITE CYCLE NO. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ is LOW During Write Cycle) [1]



Notes:

1. The internal write time is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
2. I/O will assume the High-Z state if $\overline{OE} > V_{IH}$.

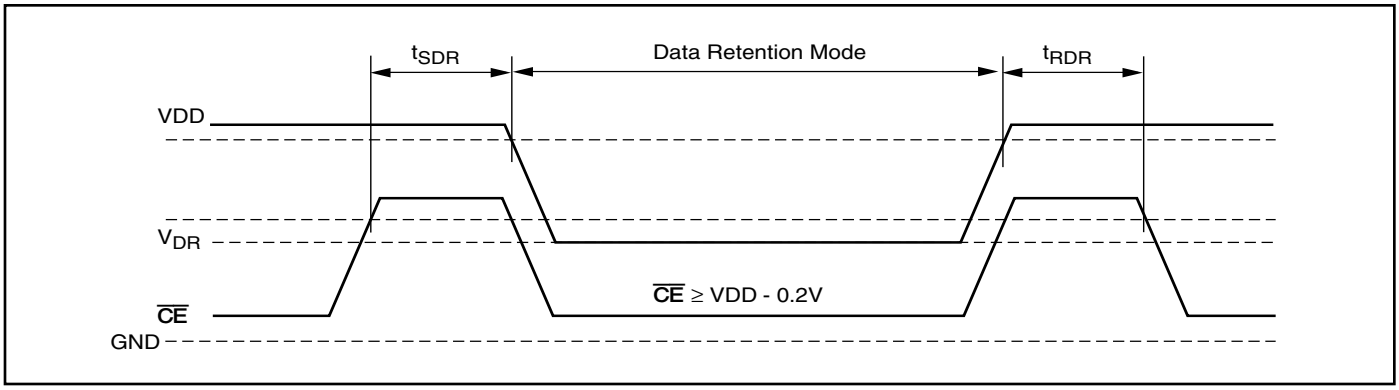
DATA RETENTION SWITCHING CHARACTERISTICS

Symbol	Parameter	Test Condition		Min.	Typ.(1)	Max.	Unit
V_{DR}	V_{DD} for Data Retention	See Data Retention Waveform		2.0		3.6	V
I_{DR}	Data Retention Current	V_{DD} = 2.0V, $\overline{CE} \geq V_{DD} - 0.2V$	Com.	—	2	40	µA
		$V_{IN} \geq V_{DD} - 0.2V$, or $V_{IN} \leq V_{SS} + 0.2V$	Ind.	—	—	50	
t_{SDR}	Data Retention Setup Time	See Data Retention Waveform		0		—	ns
t_{RDR}	Recovery Time	See Data Retention Waveform		t_{RC}		—	ns

Note:

1. Typical Values are measured at V_{DD} = 3.3V, T_A = 25°C and not 100% tested.

DATA RETENTION WAVEFORM ($\overline{CE}$ Controlled)



ORDERING INFORMATION

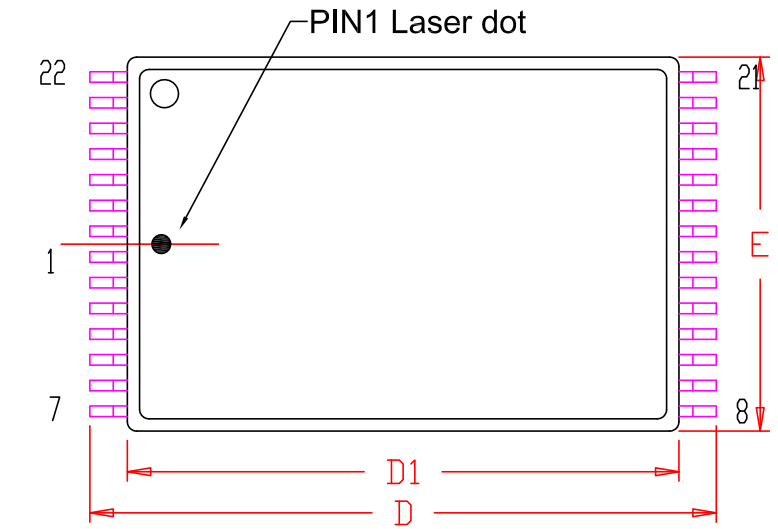
Commercial Range: 0°C to +70°C

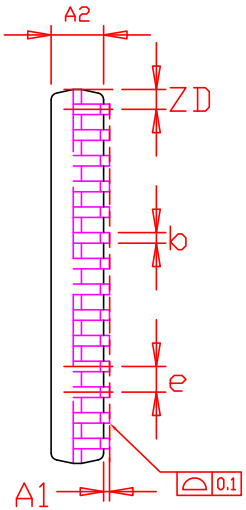
Speed (ns)	Order Part No.	Package
10	IS61LV256AL-10TL	TSOP - Type I, Lead-free
	IS61LV256AL-10JL	300-mil Plastic SOJ, Lead-free

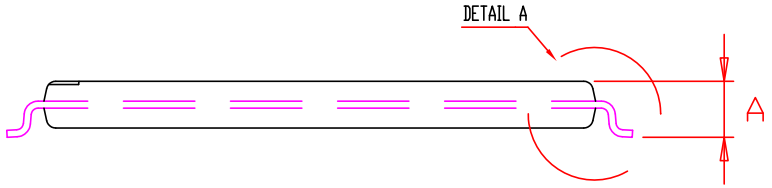
ORDERING INFORMATION

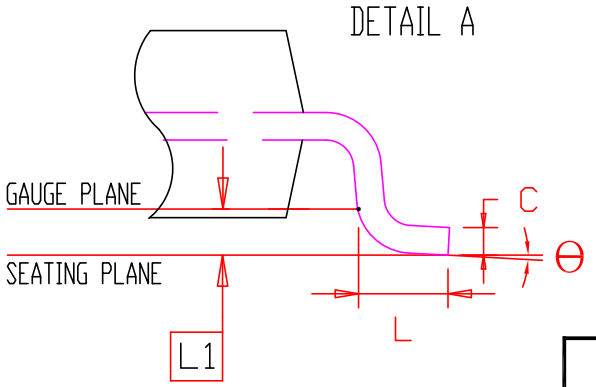
Industrial Range: –40°C to +85°C

Speed (ns)	Order Part No.	Package
10	IS61LV256AL-10TLI	TSOP - Type I, Lead-free
	IS61LV256AL-10JLI	300-mil Plastic SOJ, Lead-free









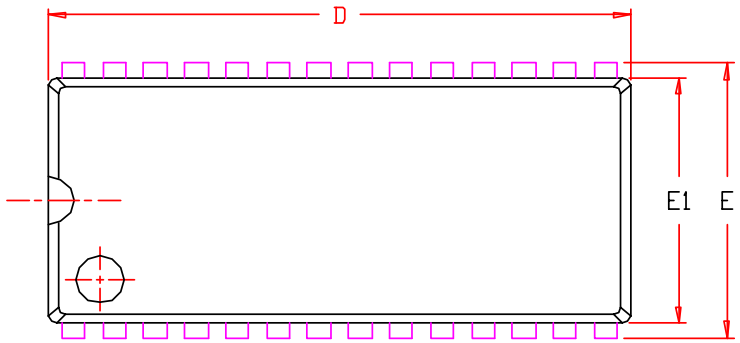
SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.95		1.20	0.037		0.047
A1	0.05		0.20	0.002		0.008
A2	0.90		1.05	0.035		0.041
b	0.17	0.22	0.27	0.007	0.009	0.011
D	13.20	13.40	13.60	0.520	0.528	0.535
D1	11.70	11.80	11.90	0.461	0.465	0.469
E	7.90	8.00	8.10	0.311	0.315	0.319
e	0.55 BSC.			0.022 BSC.		
L	0.30	0.50	0.70	0.012	0.020	0.028
L1	0.25 BSC.			0.010 BSC.		
ZD	0.425 REF.			0.017 REF.		
Θ	0	3°	5°	0	3°	5°
C	0.12		0.21	0.12		0.21

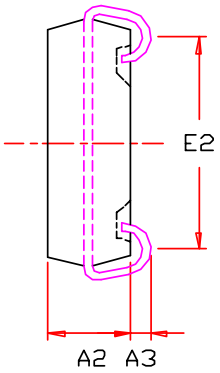
NOTE :

1. CONTROLLING DIMENSION : MM
2. DIMENSION D1 AND E DO NOT INCLUDE MOLD PROTRUSION.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.
4. Referedce Document : JEDEC MO-183

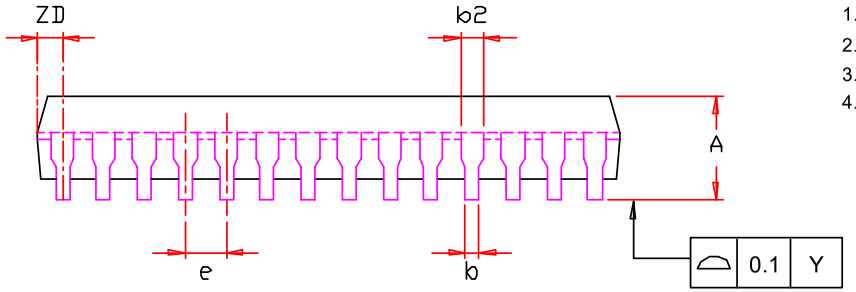
	TITLE	28L 8x13.4mm TSOP-1 Package Outline	REV.	G	DATE	10/28/2019

Integrated Silicon Solution, Inc. — 1-800-379-4774
Rev. C1
03/02/2020





SYMBOL	DIMENSION IN MM		
	MIN.	NOM.	MAX.
A	3.05		3.76
A2	2.41	2.54	2.67
A3	0.64		1.09
b	0.36		0.56
b2	0.66		0.81
D	17.70		18.54
E	8.26	8.56	8.81
E1	7.42		7.75
E2	6.22		7.29
e	1.27 BSC		
ZD	0.95 REF.		
Y	0.1		



NOTE :

1. Controlling dimension : mm
2. Dimension D1 adn E do not include mold protrusion .
3. Dimension b2 does not include dambar protrusion/intrusion.
4. Formed leads shall be planar with respect to one another within 0.1mm at the seating plane after final test.

ISSI®	TITLE	28L 300mil SOJ Package Outline	REV.	C	DATE	07/05/2006