

**1.1 Scope.**

This specification covers the detail requirements for a monolithic CMOS 14-bit digital-to-analog converter for direct interfacing to both 8- and 16-bit microprocessor systems. A novel low-leakage configuration enables the AD7535 to exhibit excellent output leakage current characteristics over the specified temperature range.

**1.2 Part Number.**

The complete part numbers per Table 1 of this specification are as follows:

Device	Part Number <sup>1</sup>
-1	AD7535S(X)/883B
-2	AD7535T(X)/883B

**NOTE**

<sup>1</sup>See paragraph 1.2.3 for package identifier.

**1.2.3 Case Outline.**

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
E	E-28	28-Contact LCC
Q	Q-28	28-Pin Cerdip

**1.3 Absolute Maximum Ratings.** ( $T_A = +25^\circ\text{C}$  unless otherwise noted)

$V_{DD}$ (Pin 26) to DGND	-0.3V, +17V
$V_{SS}$ (Pin 27) to AGND	-15V, +0.3V
$V_{REFS}$ (Pin 1) to AGND	±25V
$V_{REFE}$ (Pin 2) to AGND	±25V
$V_{RFB}$ (Pin 3) to AGND	±25V
Digital Input Voltage (Pins 8-25) to DGND	-0.3V, $V_{DD}$
$V_{PIN4}$ to DGND	-0.3V, $V_{DD}$
AGND to DGND	-0.3V, $V_{DD}$
Power Dissipation	
Up to +75°C	1000mW
Derates above +75°C	10mW/°C
Operating Temperature Range	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Lead Temperature (Soldering 10sec)	+300°C

**1.5 Thermal Characteristics.**

Thermal Resistance  $\theta_{JC} = 35^\circ\text{C}/\text{W}$  for Q-28 and E-28  
 $\theta_{JA} = 120^\circ\text{C}/\text{W}$  for Q-28 and E-28

# AD7535—SPECIFICATIONS

Table 1.

Test	Symbol	Device	Design Limit $T_{min}, T_{max}$	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition <sup>1</sup>	Units
Resolution	RES	-1, 2	14					Bits
Relative Accuracy	RA	-1	±2	±2	±2			LSB max
		-2	±1	±2	±1	±1		
Differential Nonlinearity	DNL	-1, 2	±1	±1	±1		Guaranteed Monotonic to 14-Bits	LSB max
Gain Error <sup>2</sup>	$A_E$	-1	±8	±8	±8			LSB max
		-2	±4	±8	±4	±4		
Gain Tempo	$TC_{AE}$	-1	±5					ppm/°C max
		-2	±2.5					
Supply Rejection ( $\Delta$ Gain/ $\Delta V_{DD}$ )	PSRR	-1, 2	±0.02	±0.01	±0.02		$\Delta V_{DD} = \pm 5\%$	% per % max
Output Leakage Current (Pin 4)	$I_{OUT}$	-1, 2	±20	±5	±20		$V_{SS} = -300mV$ (All Digital Inputs 0V)	nA max
			±150	±5	±150		$V_{SS} = 0V$ (All Digital Inputs 0V)	
Output Current Settling Time (@ 25°C)	$t_{SL}$	-1, 2	1.5				To 0.003% of FSR. $I_{OUT}$ LOAD = 100Ω, $C_{EXT} = 13pF$ . DAC Register Alternately Loaded with All 1's and All 0's.	μs max
Feedthrough Error <sup>3</sup>	FT	-1, 2	10				$V_{REF} = \pm 10V$ , 10kHz Sine Wave DAC Register Loaded with All 0's	mV p-p max
Reference Input Resistance (Pin 1)	$R_{IN}$	-1, 2	3.5	3.5	3.5		Typical Input Resistance = 6kΩ	kΩ min
			10	10	10			kΩ max
Digital Input High Voltage	$V_{IH}$	-1, 2	2.4	2.4	2.4			V min
Digital Input Low Voltage	$V_{IL}$	-1, 2	0.8	0.8	0.8			V max
Input Leakage Current	$I_{IN}$	-1, 2	±10	±1	±10		$V_{IN} = 0V$ or $V_{DD}$	μA max
Input Capacitance	$C_{IN}$	-1, 2	7					pF max
Analog Output Capacitance Pin 3	$C_{OUT}$	-1, 2	260				DAC Register Loaded with All 1's	pF max
			130				DAC Register Loaded with All 0's	
CSMSB or CSLSB to $\overline{WR}$ Setup Time	$t_{CWS}$	-1, 2	0					ns min
CSMSB or CSLSB to $\overline{WR}$ Hold Time	$t_{CWH}$	-1, 2	0					ns min
LDAC Pulse Width	$t_{LDAC}$	-1, 2	240					ns min
Write Pulse Width	$t_{WR}$	-1, 2	240					ns min
Data Setup Time	$t_{DS}$	-1, 2	180					ns min
Data Hold Time	$t_{DH}$	-1, 2	30					ns min
Power Supply Voltage Range	$V_{DD}$	-1, 2	11.4				Specs Guaranteed Over This Range	+ V min
			15.75					+ V max
	$V_{SS}$	-1, 2	-200					mV min
			-300					mV max
Power Supply Current	$I_{DD}$	-1, 2	4	4	4		All Digital Inputs $V_{IL}$ or $V_{IH}$	mA max
			500	500	500		All Digital Inputs 0 or $V_{DD}$	μA max

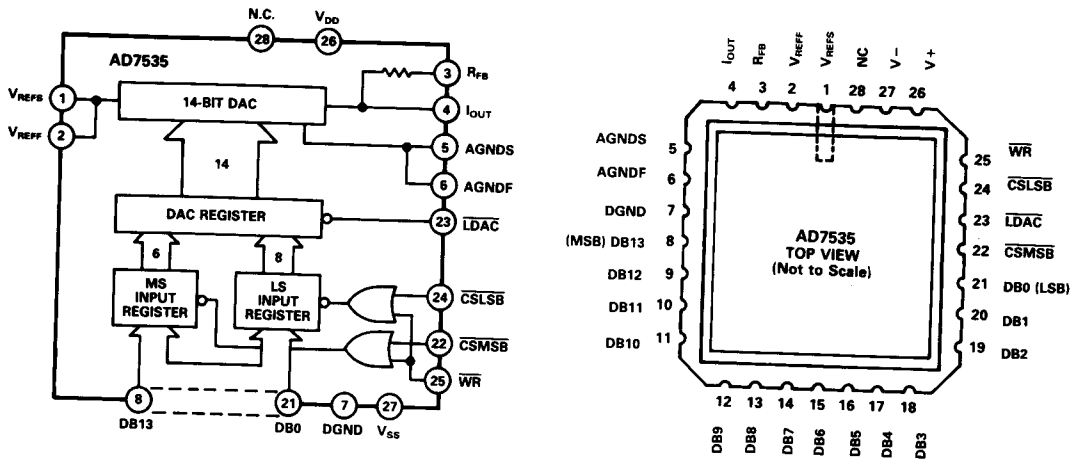
**NOTES**

<sup>1</sup> $V_{DD} = +12V$  to  $+15V$ ;  $V_{REF} = +10V$ ,  $V_{PIN3} = V_{PIN4} = 0V$ ,  $V_{SS} = -300mV$  unless otherwise stated. Specifications are guaranteed for a  $V_{DD}$  of  $+12V$  to  $+15V$  with a tolerance of  $\pm 5\%$ , testing is performed at 12V and 15V only.

<sup>2</sup>Measured using internal feedback resistor and includes effects of leakage current and gain T.C.

<sup>3</sup>Feedthrough can be further reduced by connecting the metal lid to ground.

## 3.2.1 Functional Block Diagram and Terminal Assignments.



## 3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (80).

## 4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883, Method 1005. Burn-in is per MIL-STD-883 Method 1015, Test Condition (B).

