ICs for Communications

Quad ISDN High Voltage Power Controller
QIHPC

PEB/F 2426 Version 1.1

Preliminary Data Sheet 06.99

DS 1

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1 Overview

The Quad ISDN High Voltage Power Controller provides a power source for up to four U-line interfaces. The power source to the device is a local battery or a centralized power supply.

Each powered line is individually controlled and monitored by the device interface. Line powering can be switched on or off by command. The QIHPC indicates, when the output current is above a threshold for longer than the programmable time t_{OC}. At a second (higher) value the current is limited. The values of the current limitation and the overcurrent indication threshold are defined with external resistors, the overcurrent indication setup delay is selected by external capacitances.

The status information of each line (acknowledge of requested power feed) is returned to the system. The status information enables an easy detection of overloads and faults and a fast localization even on a large system.

The integrated intelligent chip temperature control guards the QIHPC in case of overloads.

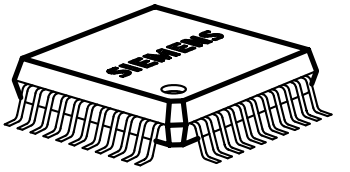
Additionally eight drivers for external relays and their control logic are integrated on the QIHPC. These relay drivers provide open collector output stages with high current capability.

Quad ISDN High Voltage Power Controller QIHPC

PEB 2426

Version 1.1 **SPT 170**

1.1 Features



P-MQFP-44

- ISDN Line Feed Supply Voltage up to 130 V
- Supplies power for up to four ISDN transmission lines
- ETSI TS 102 080 compatible
- Separate Current Monitoring and Limiting for each line
- Current Limiting Level can be programmed by an external resistor
- Overcurrent indication threshold can be programmed with external resistors independently from the current limitation.
- The overcurrent indication setup delay can be programmed by external capacitors, separately for each line
- Intelligent Chip Temperature Control
- Automatically switching off lines in current limitation when expecting over temperature problems
- Automatically switching off all four lines in case of real overtemperature
- Integrated Relay Drivers and Relay Driver Controlling for eight relays
- Optimized for working in conjunction with PEB 24901 (DFE-T), PEB 24911 (DFE-Q), and PEB 2491 (QUAD-U)
- Small P-MQFP-44 Package
- Reliable 170 V Smart Power Technology

Type	Package
PEB 2426	P-MQFP-44

1.2 Logic Symbol

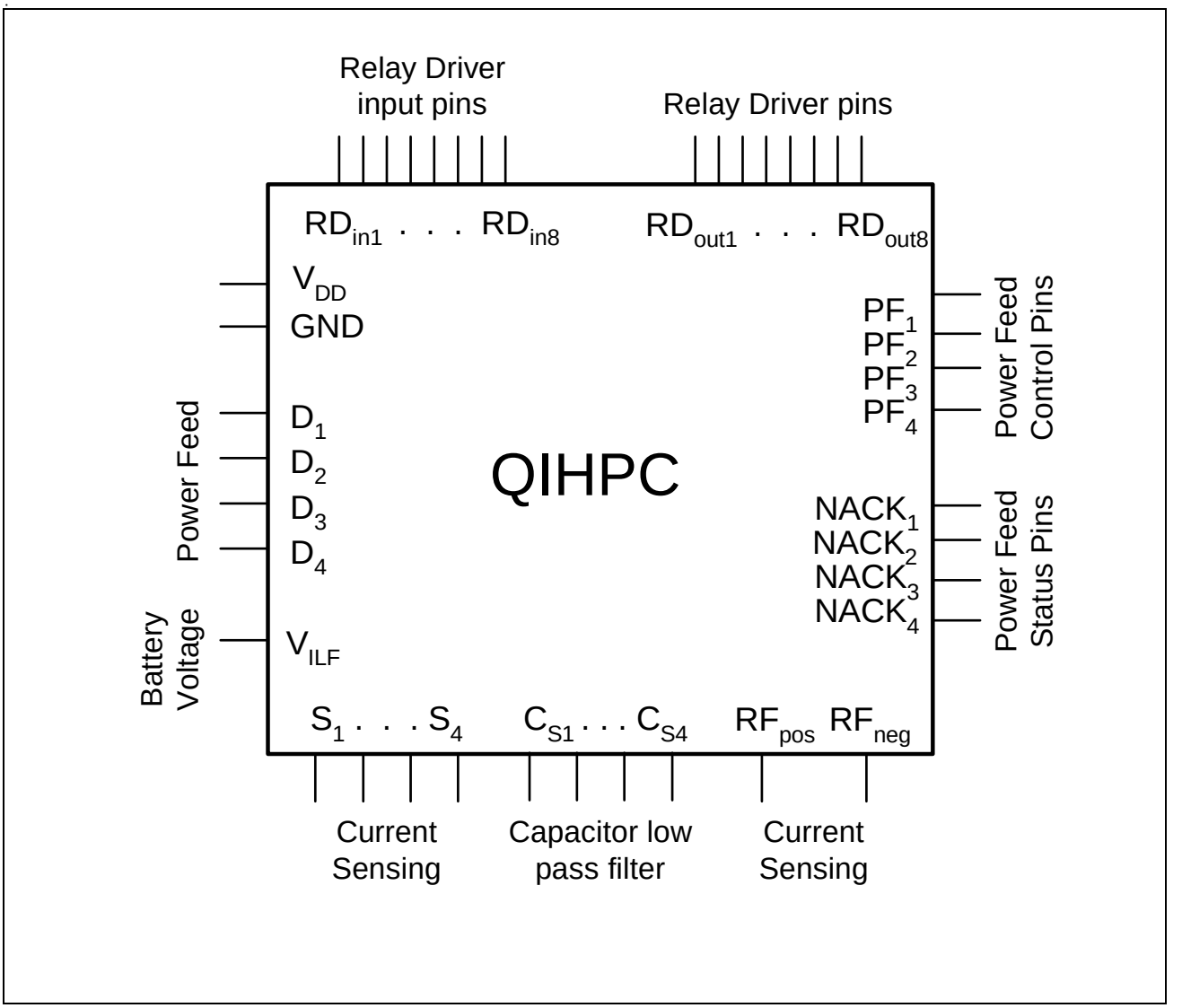


Figure 1 Logic Symbol

1.3 Typical Applications

The QIHPC is an integrated power controller especially designed for feeding two-wire ISDN-transmission lines. Four U interface lines can be powered by one QIHPC.

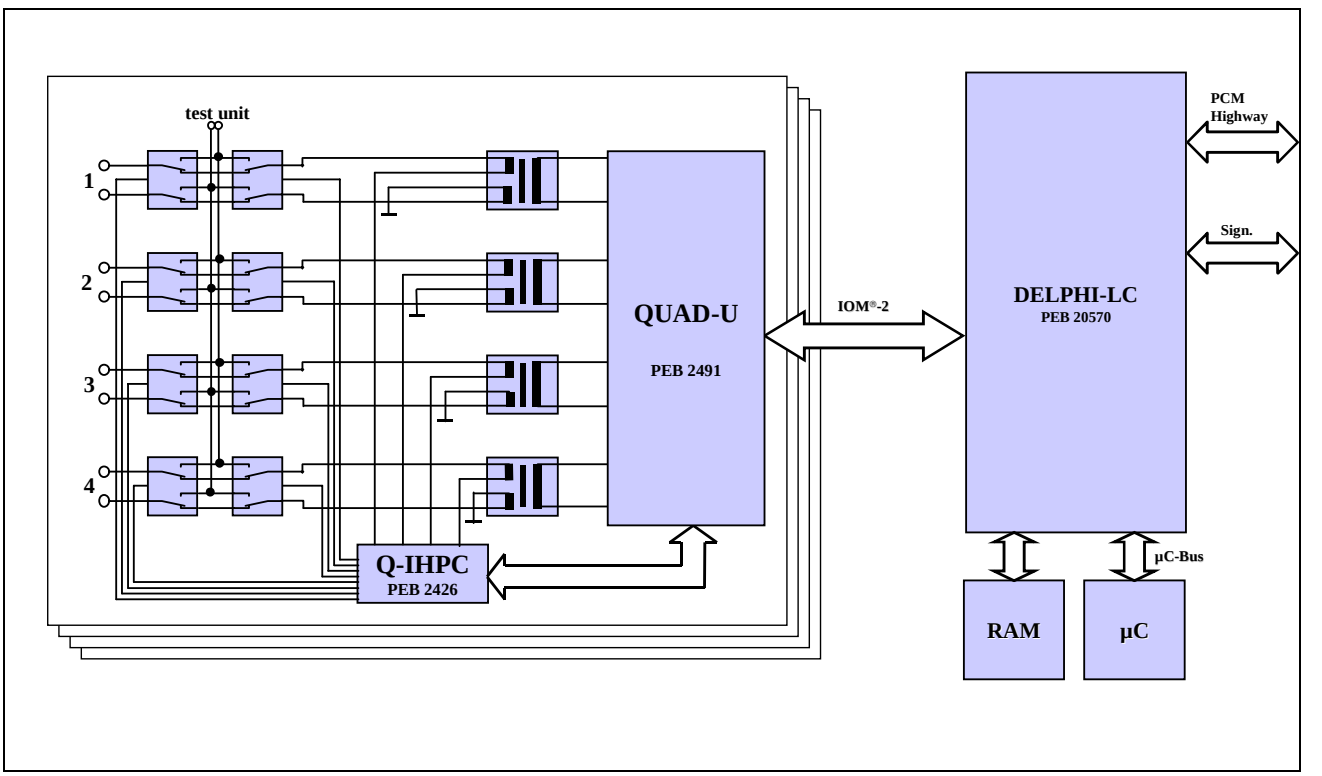


Figure 2 16-Line Card Application with DELPHI and QUAD-U

Figure 3 gives general overview of the system integration of the QIHPC.

Because of integrated “pull-down current-sinks” on the input pins $PF_{1..4}$ and $RD_{in1..8}$ only connections to V_{DD} are necessary to switch on power feeding to the lines or to switch on the relay drivers. When power feeding to a line is switched on, and this line is in a normal feeding condition (current less than 50 mA), then the QIHPC shows a resistive connection from D_x to S_x. D_x and S_x are the drain and source of the integrated DMOS-transistor of channel x. The resistance value (DMOS-R_{on}) is typically 1.4 Ω with a total tolerance of about +/- 0.35 Ω.

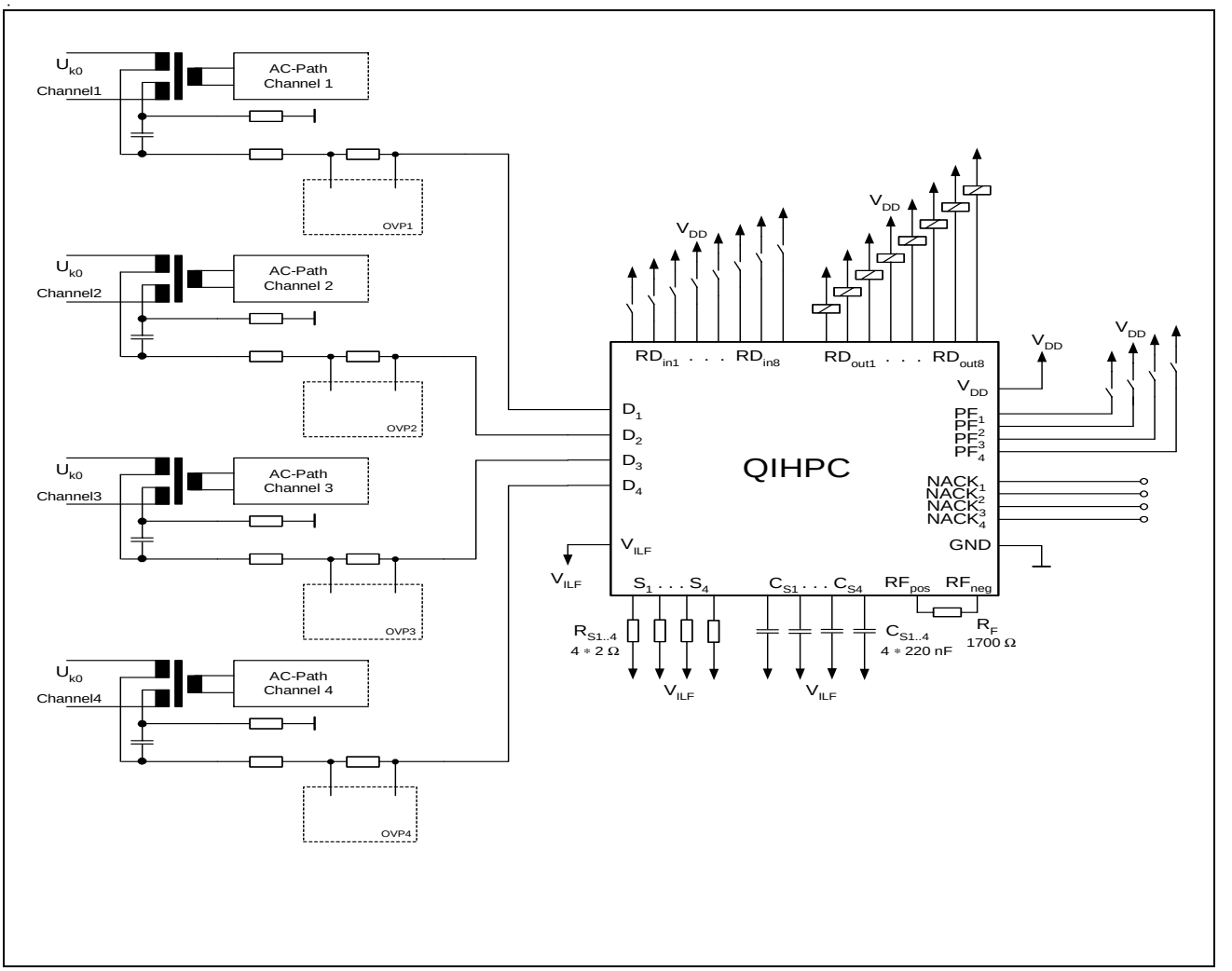


Figure 3 System integration

2 Pin Descriptions

2.1 Pin Configuration

(top view)

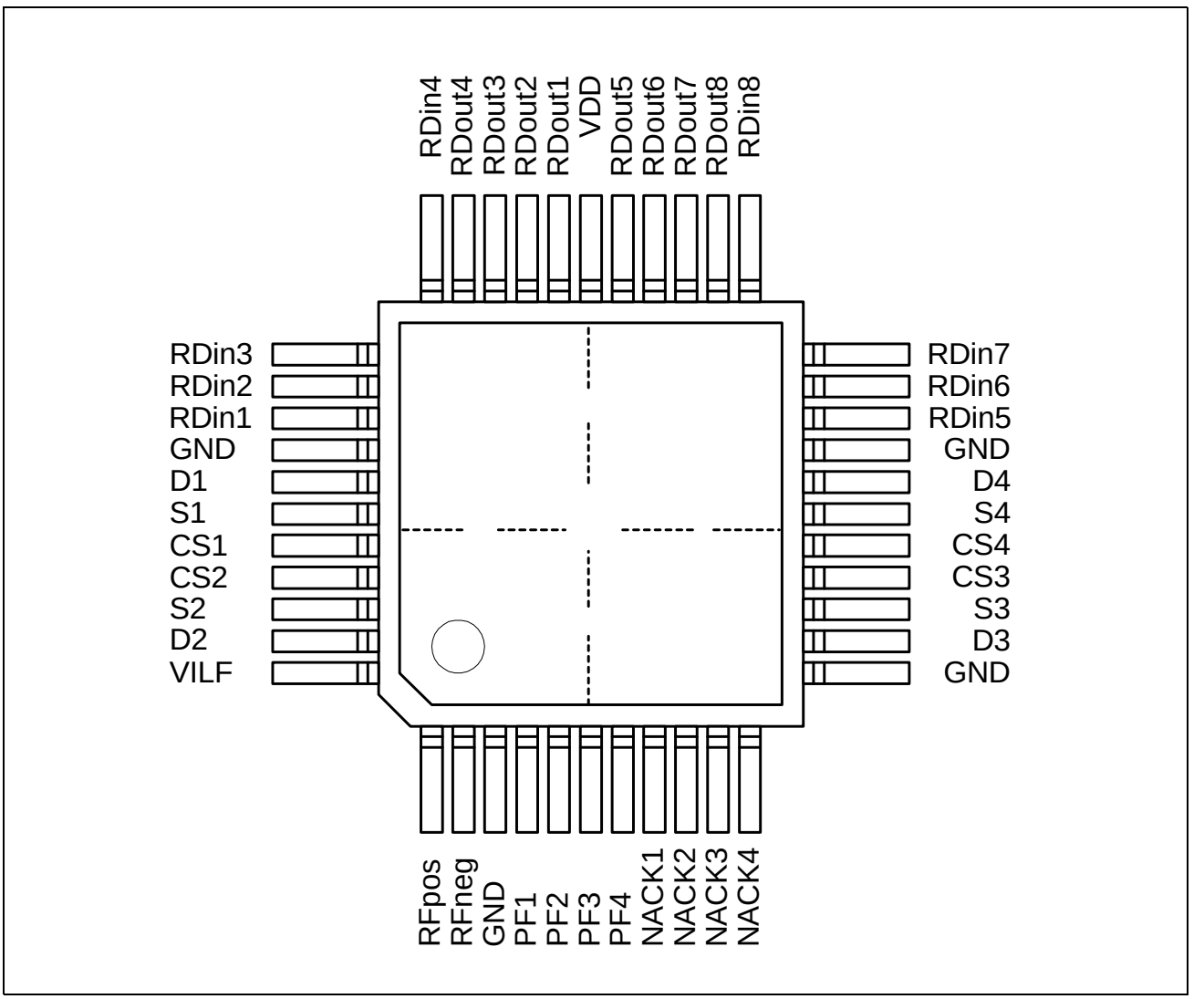


Figure 4 Pin Configuration

2.2 Pin Definitions and Functions

Table 1 Pin Definitions and Functions

Pin No.	Symbol	Input (I) Output (O)	Function
28	V_{DD}	Supply	**Positive Supply Voltage, referred to GND.** Operating Voltage Range from 3.0 V to 6.0 V.
3 12 19 37	GND	Supply	Ground
44	V_{ILF}	Supply	**ISDN Line Feed Voltage, referred to GND.** Operating Voltage Range from -130 V to -30 V.
38 43 13 18	D_1 D_2 D_3 D_4	O	**Drain Connections of the Output Transistors of Channels 1..4.** These pins have to be connected (via external resistors) to ISDN lines a (ring) of channels 1..4.
1 2	RF_{pos} RF_{neg}	O	**Current limitation of Channels 1..4.** These pins have to be connected to an external resistor R_F. R_F and $R_{S1..4}$ are defining the output current limit for all four lines.
39 42 14 17	S_1 S_2 S_3 S_4	O	**Overcurrent indication threshold.** These pins have to be connected via external resistors $R_{S1..4}$ to V_{ILF} defining the overcurrent indication threshold of each line individually.
40 41 15 16	C_{s1} C_{s2} C_{s3} C_{s4}	O	**External capacitors defining t_{oc}-delays of Channels 1..4.** These pins have to be connected via external capacitors to V_{ILF} defining the overcurrent indication delay.
4 5 6 7	PF_1 PF_2 PF_3 PF_4	I	**Power Feed Signal of Channels 1..4.** Logic high on $PF_{1..4}$ switches on the power feeding to the line of channel 1..4.
8 9 10 11	$NACK_1$ $NACK_2$ $NACK_3$ $NACK_4$	O	**Not Acknowledged Signal of Channels 1..4.** Logic low on $NACK_{1..4}$ signals that either the ISDN line of channel 1..4 is powered and in a normal power on condition or that power feed is not requested..

Table 1 Pin Definitions and Functions (Continued)

Pin No.	Symbol	Input (I) Output (O)	Function
36 35 34 33 20 21 22 23	RD_{in1} RD_{in2} RD_{in3} RD_{in4} RD_{in5} RD_{in6} RD_{in7} RD_{in8}	I	**Switch-On-Signal of Relay-Channels 1..8.** Logic high on $R_{in1..8}$ switches on the relay driver npn-transistor of channel 1..8.
29 30 31 32 27 26 25 24	RD_{out1} RD_{out2} RD_{out3} RD_{out4} RD_{out5} RD_{out6} RD_{out7} RD_{out8}	O	**Open Collector Output of Relay-Channels 1..8.** When the relay driver npn-transistor of channel 1..8 is switched on, than this pin sinks a current of up to 40 mA. An integrated zener diode guards the QIHPC against inductive voltage peaks from the relay coil.

3 Functional Description

3.1 Functional Block Diagram

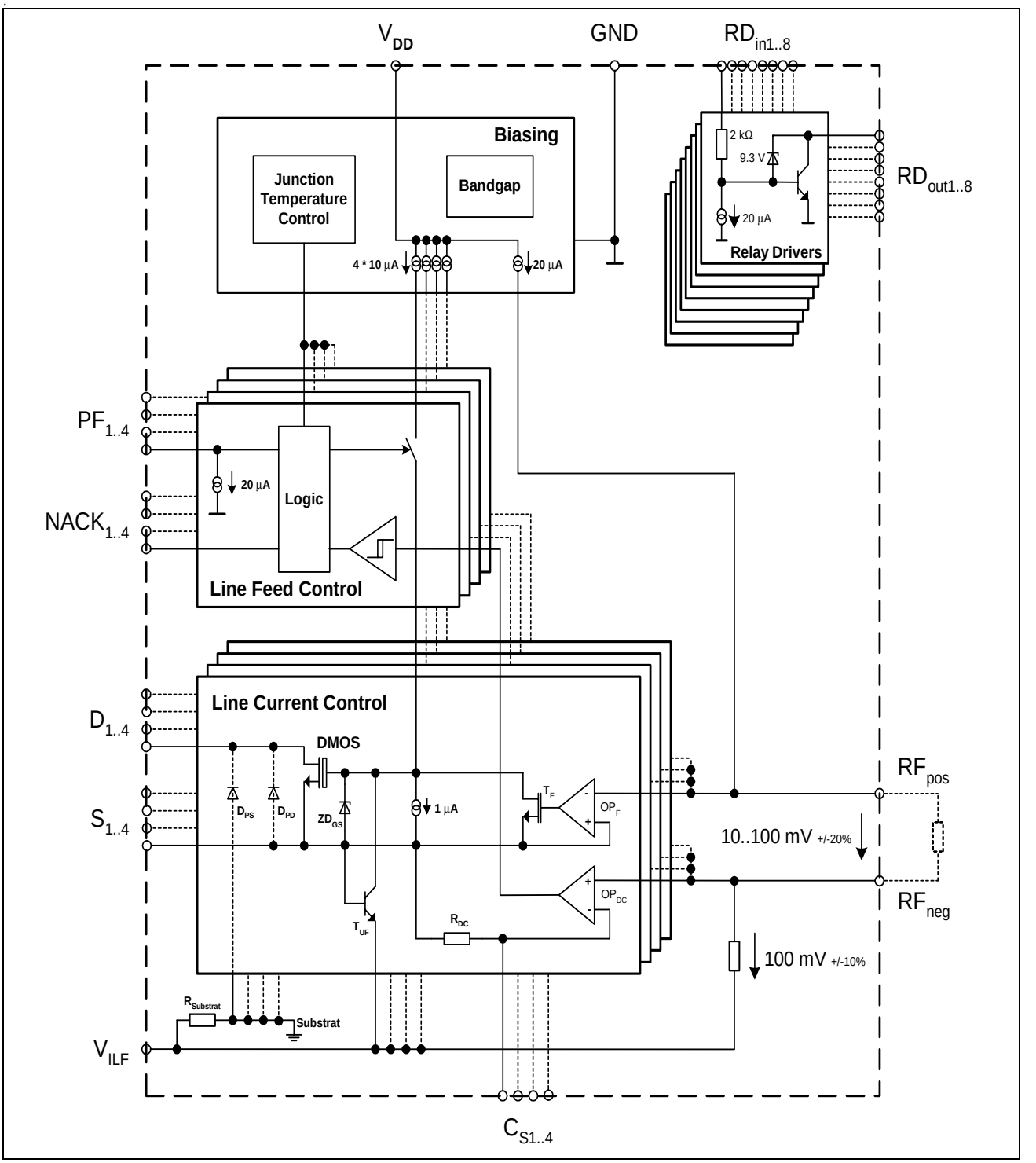


Figure 5 Functional Block Diagram

In the Functional Block Diagram, **Figure 5**, we can see four different types of circuit blocks: one biasing circuit, four line feed control circuits, four line current control circuits and eight relay driver circuits.

3.2 Biasing Circuit

The bandgap circuit generates a constant voltage with respect to GND. This reference voltage is converted into a current of about 20 µA which is necessary for level shifting. This current is converted back into 100 mV and 10..100 mV (depending on the value of the external resistor R_F) reference voltages with respect to V_{ILF}. These reference voltages and the external resistors connected between pins $S_{1..4}$ and V_{ILF} defines the line current limit and the overcurrent indication threshold.

Currents of about 10 µA are used for level shifting the power feed information. In the biasing block also all other biasing currents used on the chip are generated.

Intelligent junction temperature control in coordination with line current limiting protects the QIHPC against overloads. Also a fault condition on one line shall under no circumstance disturb a connection on another line. Therefore a junction temperature control circuit is necessary.

The junction temperature of the QIHPC will be monitored by an integrated thermal detector with three threshold levels, as defined in **Table 2**

Table 2 Thermal Detector Threshold Levels

Symbol	Parameter Description	Test Conditions	Limits			Unit
			Min	Typ	Max	
T_{j1}	130 °C Thermal Detector threshold	guaranteed by design	120	130	140	°C
T_{h1}	130 °C Thermal Detector hysteresis	guaranteed by design		10		°C
T_{j2}	170 °C Thermal Detector threshold	guaranteed by design	160	170	180	°C
T_{h2}	170 °C Thermal Detector hysteresis	guaranteed by design		10		°C
T_{j3}	190 °C Thermal Detector threshold	guaranteed by design	180	190	200	°C
T_{h3}	190 °C Thermal Detector hysteresis	guaranteed by design		10		°C

Power on requests will only be executed if the junction temperature is below T_{j1} (typical 130 °C) and if no other line is in overcurrent condition. If the device junction temperature reaches the second threshold T_{j2} (typical 170 °C), then all the line drivers in the current-

overload condition will be switched off by the QIHPC. If the device junction temperature then still continues to increase to T_{j3} (typical 190 °C), all the line drivers will be turned off by the QIHPC.

The line(s) in current overload will be switched off sufficiently fast once the second threshold T_{j2} is reached, i.e. before the T_{j3} threshold is reached. This guarantees a disturbance free operation on lines not affected by a fault condition. Once a line had been switched off the relevant PF-pin has to be set to low and subsequently to high, for attempting to power this line again.

The internal protection mechanisms (current limiting and junction temperature control) already provide full protection of the $D_{1..4}$ outputs against short circuits to a voltage between GND and V_{ILF}.

Note: The thermal protection mechanism of the QIHPC is a protection against instant damages due to overload at the outputs. Continuous high temperatures during operation, however, will reduce the life time of the QIHPC. Measures have to be taken to switch off the QIHPC in case of a short-circuit. E.g. if pin $NACK_x$ indicates an current overload condition, the QIHPC should be deactivated after few seconds using pin PF_x.

3.3 Line Feed Control Circuit

The QIHPC can supply the power for up to four transmission lines simultaneously. The exchange of activation commands and status information with the QIHPC will occur via a parallel interface, consisting of one input (PF) and one output (NACK) per line. The power switch can be controlled (PF) for each line individually. The status information (NACK) can be monitored for each line separately.

Integrated “pull-down current-sinks” are connected to the input pins $PF_{1..4}$. If one of these pins is not connected externally, the logic level at this pin is “0”.

Logic level “0” means that the voltage on this pin is about 0 and logic level “1” means that the voltage level on this pin is about V_{DD}.

A diagnostic of possible fault conditions is available on the status information pins (NACK) for each line separately.

The NACK pin is set to “1” when PF=”1” and:
- Current on the line reaches the overcurrent indication threshold for longer than t_{OC}.
- Over temperature ($T_j > T_{j3}$) is detected.
- Power feed setting is not acknowledged by the QIHPC.

See also **Table 3**.

Table 3 Function Table for Controlling One Line

PF	current (other channels)	current (this channel)	T_j	NACK	Comment
0	don't care	don't care	don't care	0	line feeding not requested
0 → 1	at least one above indication threshold	don't care	don't care	1	power feeding not acknowledged and the line is not powered as long as an other line is in overcurrent condition
0 → 1	don't care	don't care	> T_{j1}	1	power feeding not acknowledged and the line is not powered, as long as the junction temperature is to high
1	don't care	above indication threshold	< T_{j2}	1	feeding: this line is in over current condition
1	don't care	below indication threshold	< T_{j3}	0	normal line feeding
1	don't care	don't care	> T_{j3}	1	overtemperature condition, feeding is switched off

In case of simultaneous power up requests ($PF_{1..4}$) the QIHPC take care of a proper start-up sequencing. The four channels have different priority. First priority for channel 1, second priority for channel 2 etc.

By simultaneous power up requests on more than one channel, the channel with the highest priority will be powered first and only, and will normally start with current limiting condition. When this channel is powered up and the drawn current drops below the current indication level, the next channel will be powered. And so on (see also figure 6 and table 3).

3.4 Line Current Control Circuit

Two different current limiting circuits are integrated to control the DMOS power switch. An ultrafast and a fast current limiting circuit. See also **Figure 5**.

The ultrafast current limiting circuit consists of a bipolar npn-transistor T_{UF}. Note that bipolar npn-transistors are the fastest devices from the used technology. If the voltage between $S_{1..4}$ and V_{ILF} exceeds about 0.7 V the DMOS is switched off as fast as possible.

0.7 V divided by $R_{S1..4}$ = 2 Ω results in an ultrafast current limiting level of about 350 mA. This level has a strong temperature dependence (-40 °C junction temperature gives about 420 mA and +120 °C results in about 300 mA). The ultrafast current limiting circuit protects the QIHPC against short circuit on the line side with a resulting current rising as fast as 2 A/100 nsec.

The fast current limiting circuit keeps the voltage between $S_{1..4}$ and V_{ILF} below a programmable voltage level. This results in a current limitation.

Zener diode ZD_{GS} protects the DMOS-gate.

Diodes D_{PD} and D_{PS} are the parasitic drain-bulk-diode and drain-substrate-diode of the DMOS transistor (junction isolated technology). The diodes do not provide overvoltage protection, negative surges would pass through to $S_{1..4}$ and V_{ILF} affecting the battery voltage. Extra overvoltage protection circuitry is necessary to conduct voltage surges form the line to ground, and to prevent that any current can flow into Diodes D_{PD} and D_{PS}.

Typical value of DMOS-on-resistance including internal wiring-resistance to the pins $D_{1..4}$ and $S_{1..4}$ is 1.4 Ω.

To identify overcurrent, the voltage between $S_{1..4}$ and V_{ILF} is compared to 100 mV. If the voltage exceeds this level, this is indicated to the line current control circuits. A resistor and the external capacitor C_S define a lowpass filter (time delay) to suppress the changes on NACK due to short overcurrent surges. This enables to filter the effects of longitudinal AC current.

An external capacitor with a value of about 220 nF results in a delay time (t_{OC}) of about 25 msec.

3.5 Relays Driver Circuit

The output transistor is a bipolar npn. The maximal collector current should not exceed 40 mA. When switching off an inductive load, zener diode and npn clamps the voltage level on pin $RD_{out1..8}$ at about 10 V. The 2 kΩ resistor limits the input current on pin $RD_{in1..8}$ and additionally the npn collector current.

If a pin $RD_{in1..8}$ is not connected, the integrated “pull-down current-sink” holds the respective relay driver in switched-off condition.

4 Application Hints

4.1 Resistor $R_{S1..4}$

The value of this resistor defines the overcurrent indication level. Note, that the value of this resistor must be considered for line symmetry. The typical overcurrent indication level I_{ind} can be programmed by using the following formula.

$$I_{ind} = \frac{100mV}{R_{S1...4}}$$

4.2 Resistor R_F

The values of resistors R_F and $R_{S1..4}$ define the current limiting level. The typical overcurrent limitation level I_{lim}can be programmed by using the following formula.

$$I_{lim} = \frac{100mV + R_F \cdot 20\mu A}{R_{S1...4}}$$

4.3 Capacitor $C_{S1..4}$

The value of this capacitor define the resulting delay time t_{OC} for the overcurrent indication. For typical values of t_{OC} as a function of $C_{S1..4}$ see **Figure 6**.

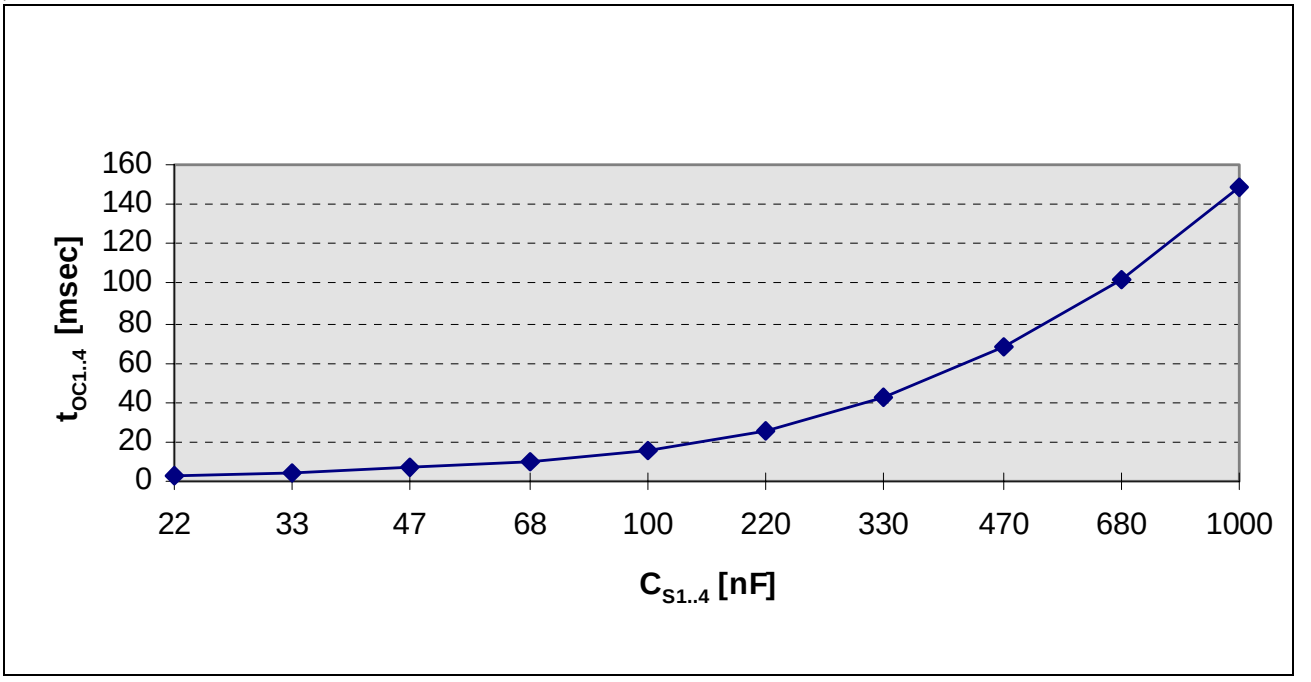


Figure 6 Delay time t_{OC} as a function of the value of $C_{S1..4}$ (typical values)

4.4 Protection Circuitry

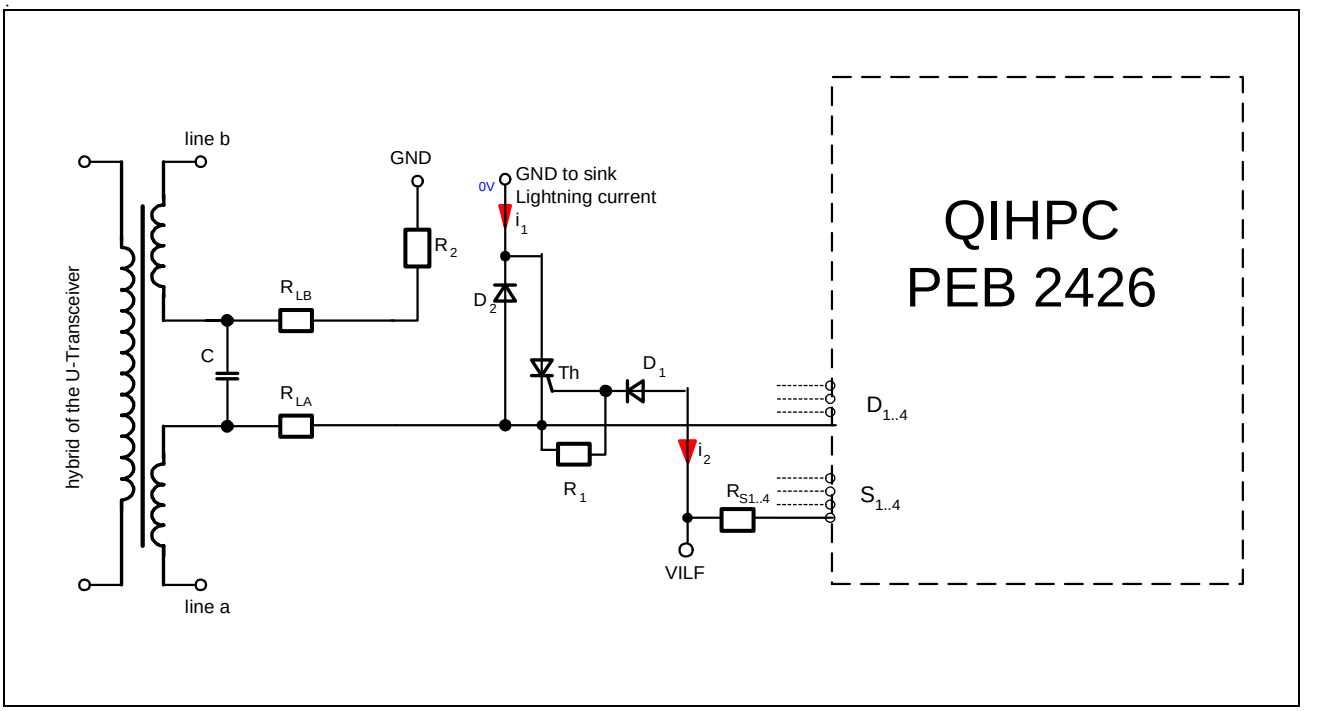


Figure 7 Proposal for a Protection Circuitry

An external circuitry is needed to protect the QIHPC against damages due to high voltages from the line. High voltages can be caused by lightning surges or foreign voltage contact.

Capacitor C and resistors R_{LA} and R_{LB} are used to filter noise from the battery voltage V_{ILF} , and reduces mismatches of the input resistance for AC-signals. R_2 mirrors the resistive path to the QIHPC at wire, i.e. the resistance of D-MOS and $R_{S1..4}$. These resistors and capacitor C shall provide compatibility with the requirements for longitudinal balance.

The diode D_2 clamps a high positive voltage surge to GND. The thyristor Th conducts negative surges to GND. Th has to fire fast enough before high negative voltage could damage the QIHPC or overload the voltage supply of V_{ILF}.

Shorting voltage surges to GND is sensed by the QIHPC equivalent to a short-circuit at the line. It will react according to the programmed overcurrent indication and overcurrent limitation.

5 Operational Description

The QIHPC is compliant to the ETSI TS 102 080 “Dynamic power feeding requirements” using the LT power test load (see **Figure 8**). There is no requirement for the order of powering up the lines, or for dependencies of controlling between the lines.

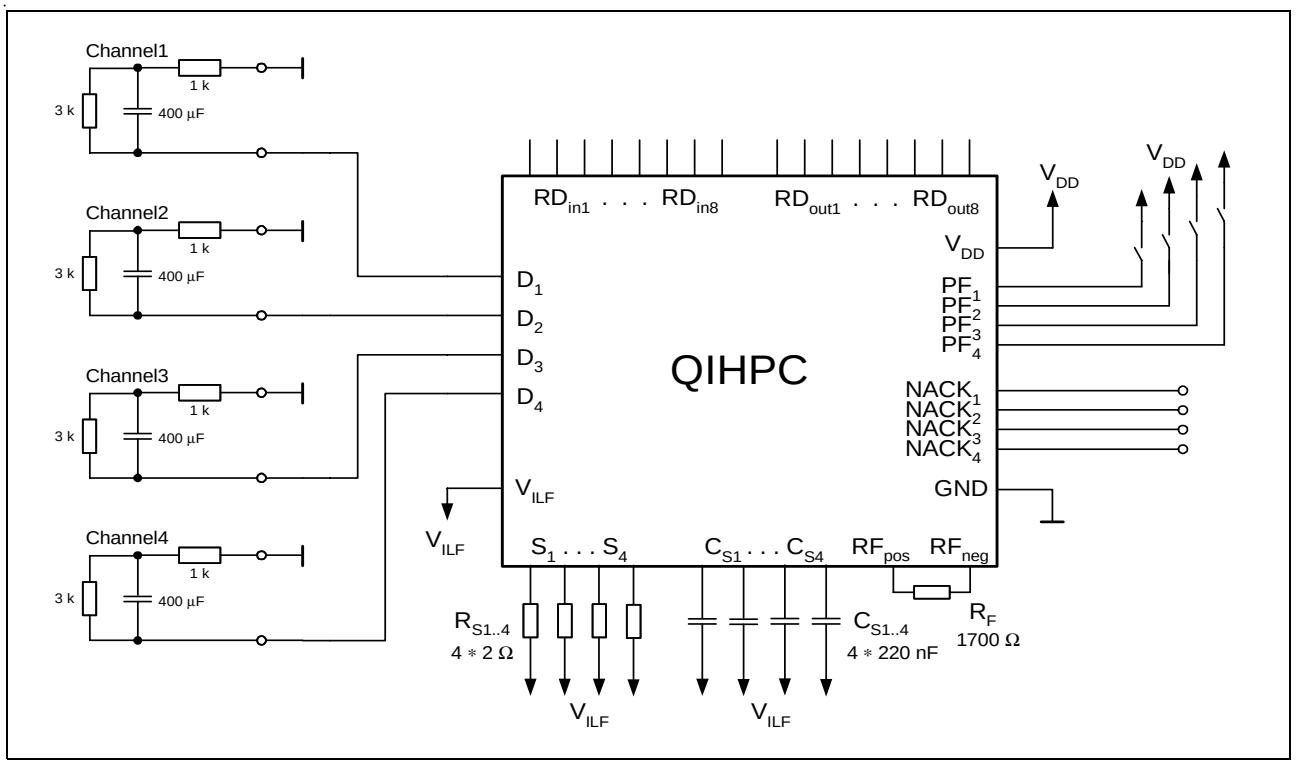


Figure 8 Circuit with “LT Power Source Test Loads”

With the LT power source test load from TS 102 080 the QIHPC can power up four U line interfaces within about 2 seconds “quasi simultaneous”. The input sequence and expected output sequence with power dissipation diagram is shown in **Figure 9**. The power dissipation in the chip is quite small.

A fault condition (short circuit) on one line does not affect the power up of the other lines.

Example:

Assumed a short circuit on line 3. A simultaneous power up request is applied to the QIHPC. The power up of lines 1 and 2 will proceed as expected. When powering up line 3, the chip temperature control (T_{j2}) will switch off this line. Lines 1 and 2 are still powered and remain in normal power on condition. When the junction temperature is decreased to T_{j1} the QIHPC will try to power up line 4. If there is no fault condition on line 4 the lines 1, 2 and 4 are finally in a normal power on condition. Line 3 is still in power off. To to repeat the trial to powering up line 3, the input signal PF_3 must set to “0” and “1” again.

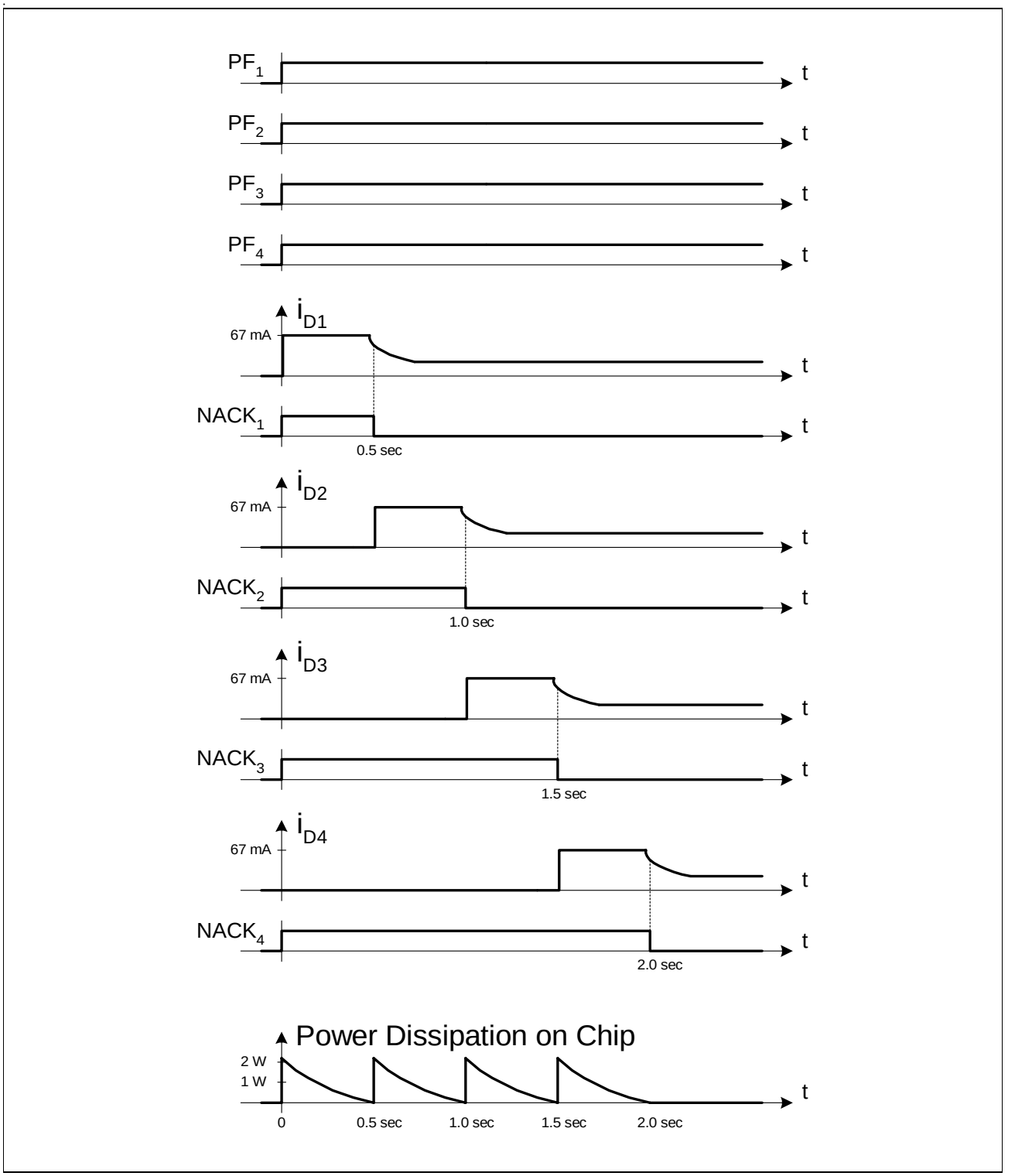


Figure 9 Simultaneous Power Up Sequence

6 Electrical Characteristics

6.1 Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Operating ambient temperature range:PEB PEF	T_A T_A	0 to 70 – 40 to 85	°C °C
Storage temperature range	T_{stg}	– 65 to 125	°C
Voltage on pin V_{DD} with respect to ground	V_{DDmax}	– 0.4 to + 8	V
Voltage on pin V_{ILF} with respect to ground	V_{ILFmax}	– 140 to V_{DD} + 0.4	V
Voltages on pins $D_{1..4}$ with respect to V_{ILF}	$V_{D1..4max}$	– 0.4 to + 150	V
Voltages on pins $D_{1..4}$ with respect to V_{ILF} with series resistor R_S = 5 Ω /figure 15	$V_{D1..4maxRs}$	– 3 to + 150	V
Pulse voltages on pins $D_{1..4}$ with respect to V_{ILF} with series resistor R_S = 5 Ω /figure 15: t = 200 msec / f = 50 Hz or t = 50 msec / f = 16.7 Hz	$V_{D1..4pulse}$	– 3 to + 150	V_P
Impulse voltages on pins $D_{1..4}$ with respect to V_{ILF} with series resistor R_S = 5 Ω /figure 15: T_{dur} = 20 µsec / T_{rise} = 25 nsec / non repetitive	$V_{D1..4impulse}$	– 5 to + 160	V_P
Voltages on pins $S_{1..4}$ with respect to V_{ILF}	$V_{S1..4max}$	– 0.4 to + 8	V
Voltages on pins $D_{1..4}$ with respect to voltages on pins $S_{1..4}$	$V_{DS1..4max}$	– 0.4 to + 140	V
Voltages on pins $C_{S1..4}$ with respect to V_{ILF}	$V_{CS1..4max}$	– 0.4 to + 8	V
Voltages on pins $PF_{1..4}$ with respect to ground	$V_{PF1..4max}$	– 0.4 to V_{DD} + 0.4	V
Voltages on pins $NACK_{1..4}$ with respect to ground	$V_{NA1..4max}$	– 0.4 to V_{DD} + 0.4	V
Voltages on pins $R_{in1..4}$ with respect to ground	$V_{Ri1..4max}$	– 0.4 to V_{DD} + 0.4	V
Voltages on pins $R_{out1..4}$ with respect to ground	$V_{Ro1..4max}$	– 0.4 to V_{DD} + 0.4	V
ESD-voltage, all pins (Human body model)	$V_{ESD-HBM}$	- 1 to + 1	kV

Note: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

6.2 Operating Range

Parameter	Symbol	Limit Values	Unit
V_{DD} supply voltage	V_{DD}	+ 3.0 to + 6.0	V
V_{ILF} supply voltage	V_{ILF}	- 130 to - 30	V

Note: In the operating range the functions given in the circuit description are fulfilled.

6.3 Static Thermal Resistance

Parameter	Symbol	Limit Values	Unit
Junction to ambient	$R_{th, jA}$	< 62.9	K/W
Junction to case	$R_{th, jC}$	< 14.6	K/W

6.4 AC/DC-Characteristics

General Test Conditions:

$R_{S1..4}$ = 2 Ω ± 0.1 % $C_{S1..4}$ =220 nF ± 1 %(63 V)
R_F = 1700 Ω ± 0.1 %

Supply voltages for typical characteristics:

V_{DD} = 5 V ± 1 % V_{ILF} =–100 V ± 1 %

Note: The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at T_A = 25°C and the given supply voltage

Table 4 DC Characteristics

No.	Parameter	Symbol	Limit Values			Unit	Test Condition	Test Fig.
			min.	typ.	max.			
Supply Currents								
1	V_{DD} current	I_{DD}		0.7	1.5	mA		10
2	V_{ILF} current	I_{ILF}		0.4	1	mA	excluding line currents	10
Line Currents, Delay Time t_{OC} and DMOS-R_{ON} resistance								
3	Overcurrent Indication Level	$I_{maxOC1..4}$	45	50	55	mA	$PF_{1..4}$ = ”1”	11
4	Current Limiting Level	$I_{max1..4}$	59	67	75.5	mA	$PF_{1..4}$ = ”1”	11
5	Line Current in “off”-condition	$I_{maxOFF1..4}$		0	10	µA	$PF_{1..4}$ = ”0”	11
6	Delay Time t_{OC}	$t_{OC1..4}$	10	25	40	msec	$PF_{1..4}$ = ”1”, I_{Line} >= 55 mA	11
7	DMOS-R_{ON} resistance	$R_{ON1..4}$ PEB2426	1.05	1.4	1.75	Ω	$PF_{1..4}$ = ”1”, I_{Line} = 25 mA	12
		$R_{ON1..4}$ PEF2426	0.8	1.4	2.0	Ω		
$PF_{1..4}$, Logic Input Levels								
8	“1” - Input Voltage	$V_{HPF1..4}$	2			V		13
9	“0” - Input Voltage	$V_{LPF1..4}$			0.8	V		13
10	“pull down” Input Current	$I_{PF1..4}$	10	20	30	µA	0.8 V < $V_{PF1..4}$ < V_{DD}	13
$NACK_{1..4}$, Logic Output Levels								
11	“1” - Output Voltage	$V_{HNACK1..4}$	V_{DD} – 0.4			V	$I_{Source1..4}$ = 100 µA	13
12	“0” - Output Voltage	$V_{LNACK1..4}$			0.4	V	$I_{Sink1..4}$ = 100 µA	13

Table 4 DC Characteristics (Continued)

No.	Parameter	Symbol	Limit Values			Unit	Test Condition	Test Fig.
			min.	typ.	max.			
$RD_{in1..8}$, Relay Driver Inputs								
13	"ON" - Input Voltage	$V_{on,RDin1..8}$	2.0		V_{DD}	V		14
14	"OFF" - Input Voltage	$V_{off,RDin1..8}$			0.4	V		14
15	"pull down" Input Current	$I_{pd,RDin1..8}$		20	30	µA	$0 < V_{RDin1..8} < 0.4$ V	14
$RD_{out1..8}$, Relay Driver Outputs								
16	Saturation Voltage	$V_{sat1,RD1..8}$		0.25	0.4	V	$V_{RDin1..8}$ = 2,4 V, $I_{RDout1..8}$ = 33 mA	14
17	Saturation Voltage	$V_{sat2,RD1..8}$	0.2	0.4	0,5	V	$V_{RDin1..8}$ = 2,4 V, $I_{RDout1..8}$ = 40 mA	14
18	Current in "off"-condition	$I_{off,RD1..8}$		0	20	µA	$V_{RDin1..8}$ = 0.4 V	14

6.5 Testing the Electrical Parameters

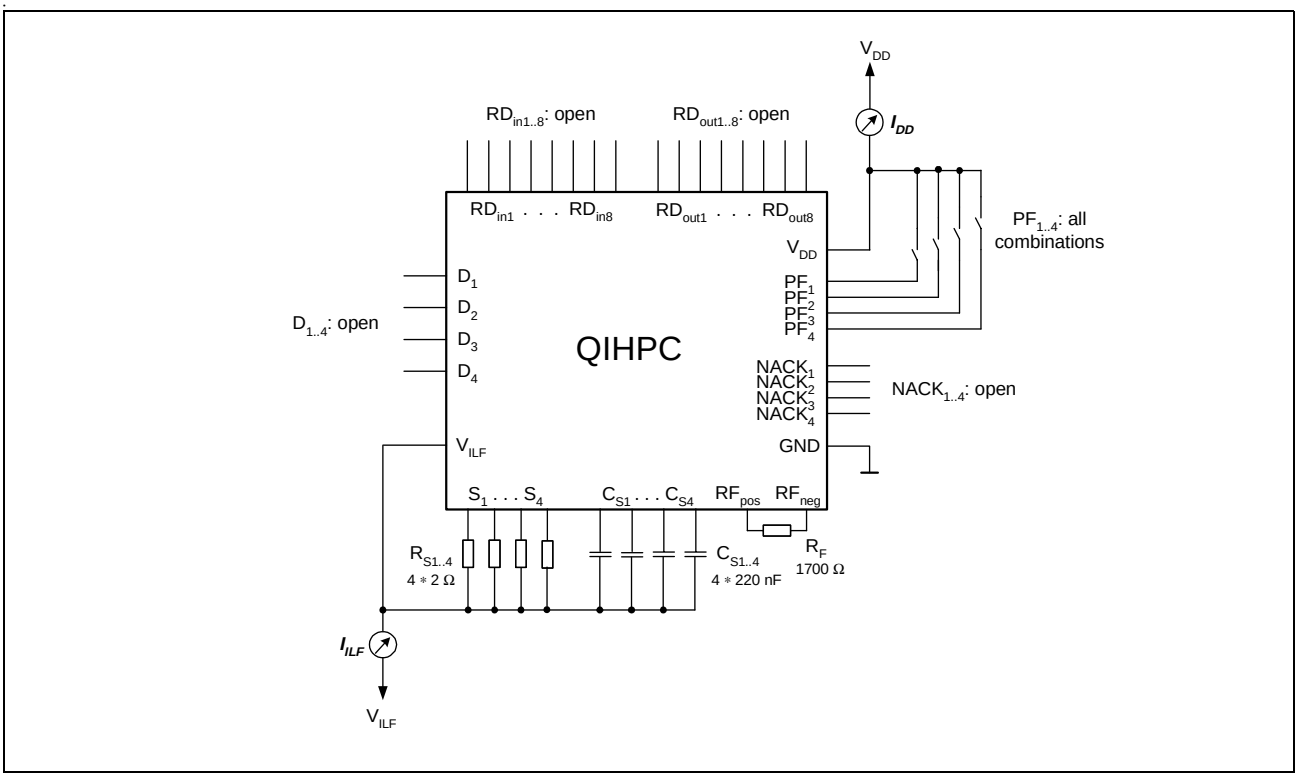


Figure 10 Supply Currents

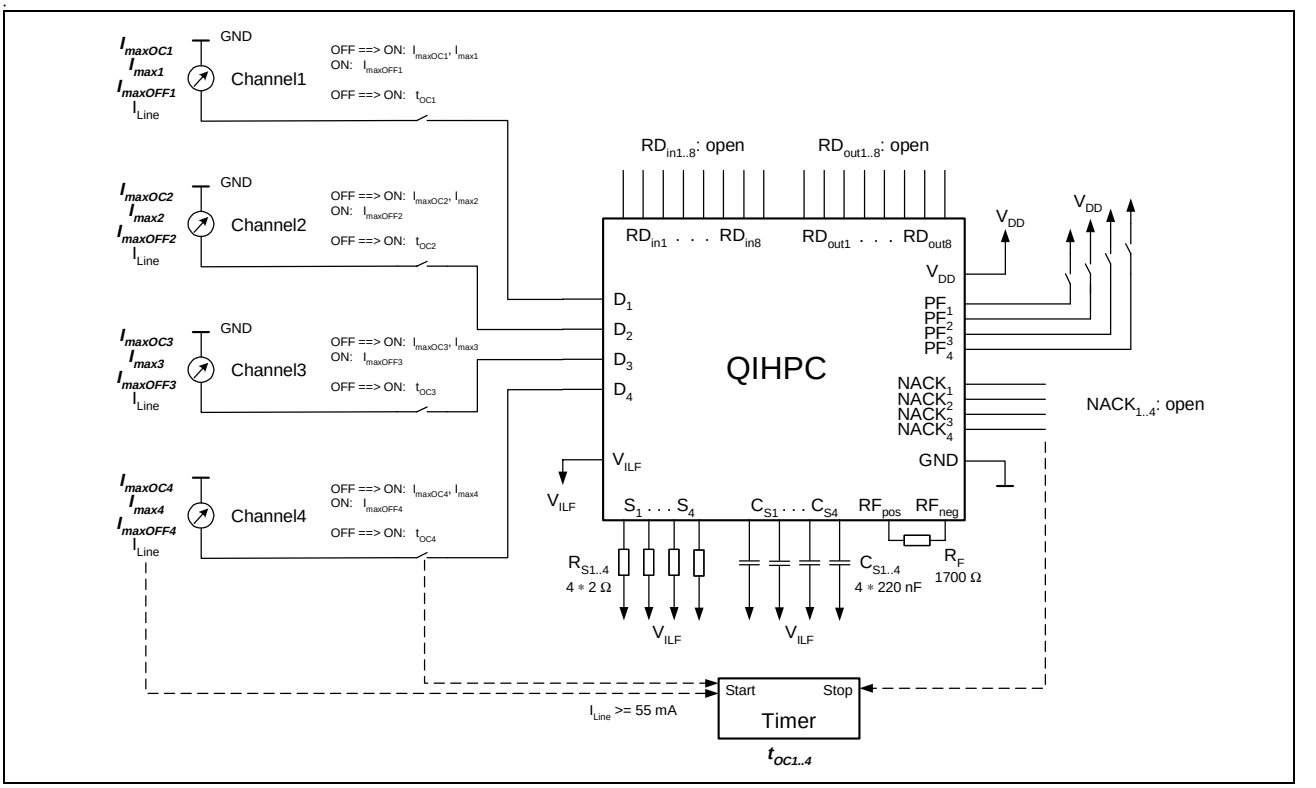


Figure 11 Line Currents and Delay Time t_{OC}

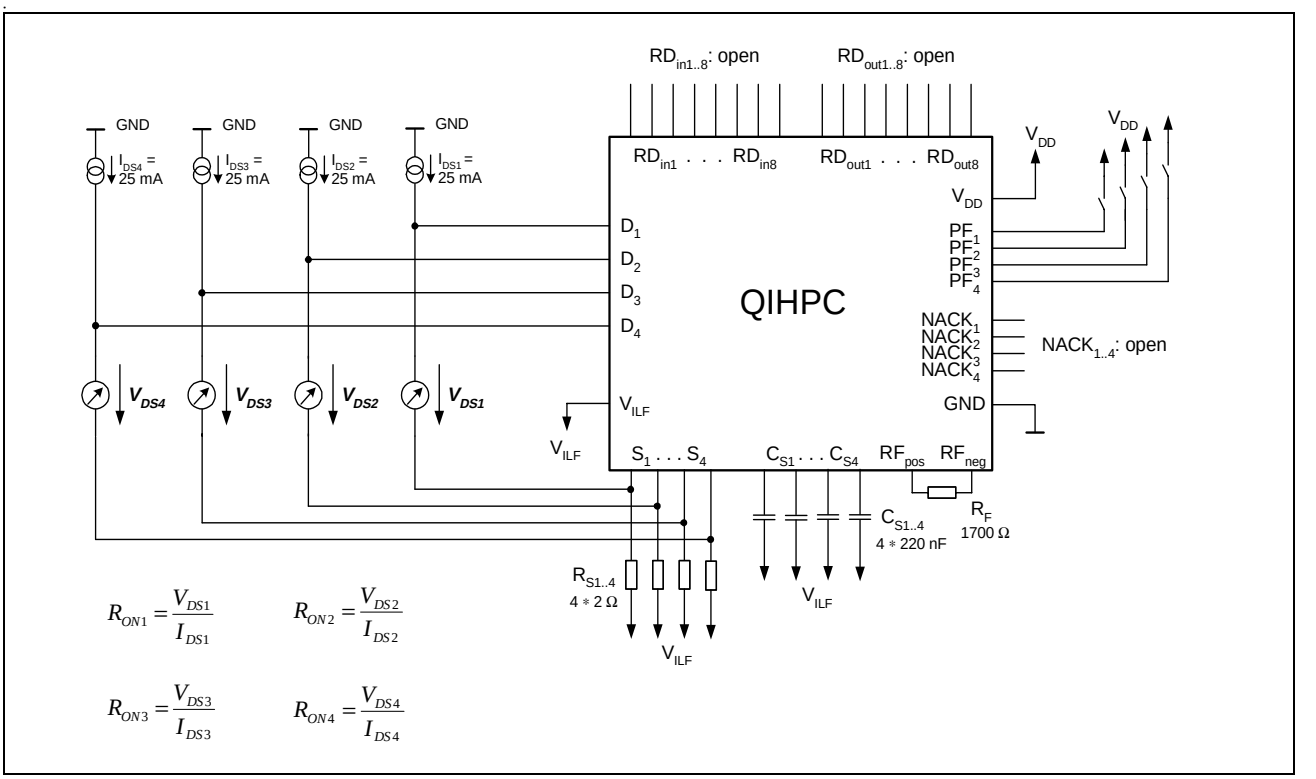


Figure 12 DMOS-R_{ON} resistance

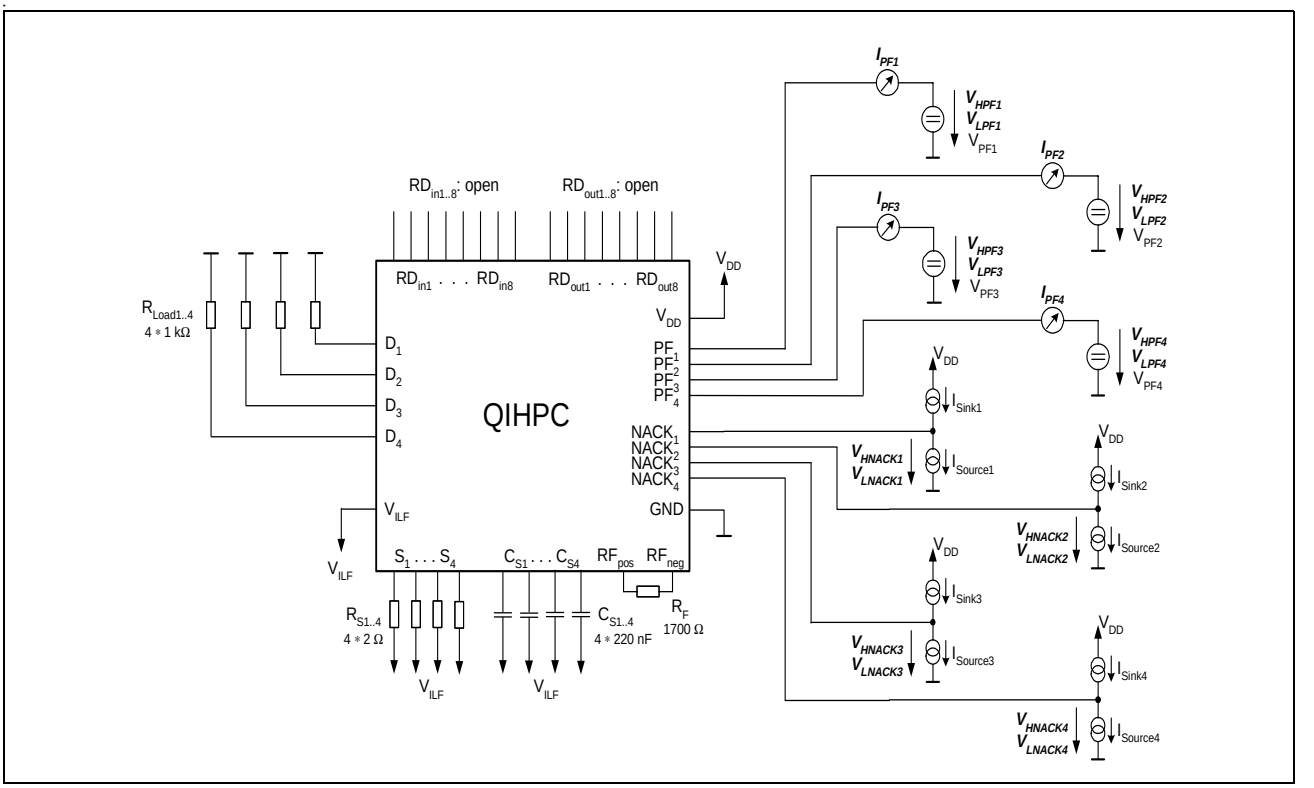


Figure 13 $PF_{1..4}$, Logic Input Levels and $NACK_{1..4}$, Logic Output Levels

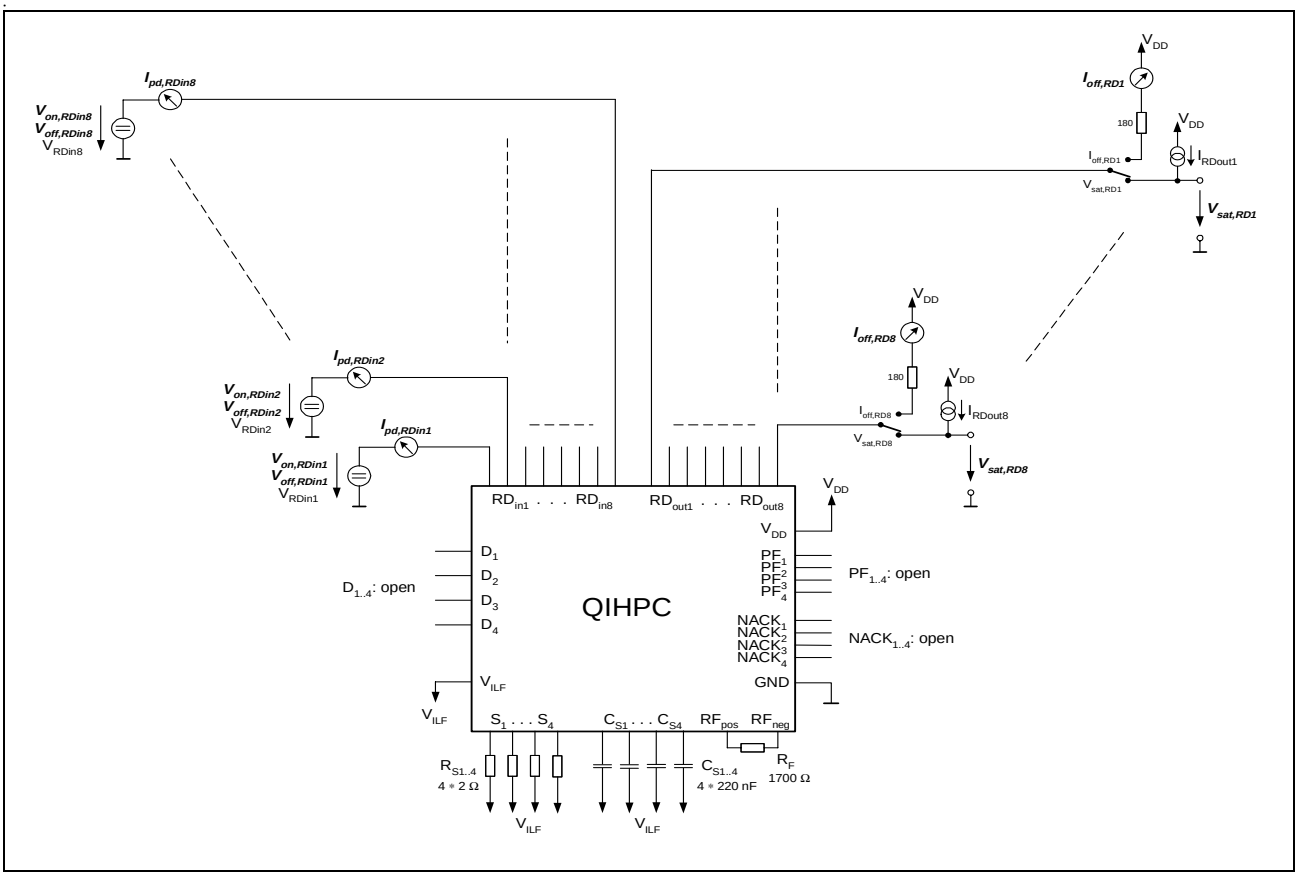


Figure 14 $RD_{in1..8}$, Relay Driver Inputs and $RD_{out1..8}$ Relay Driver Outputs

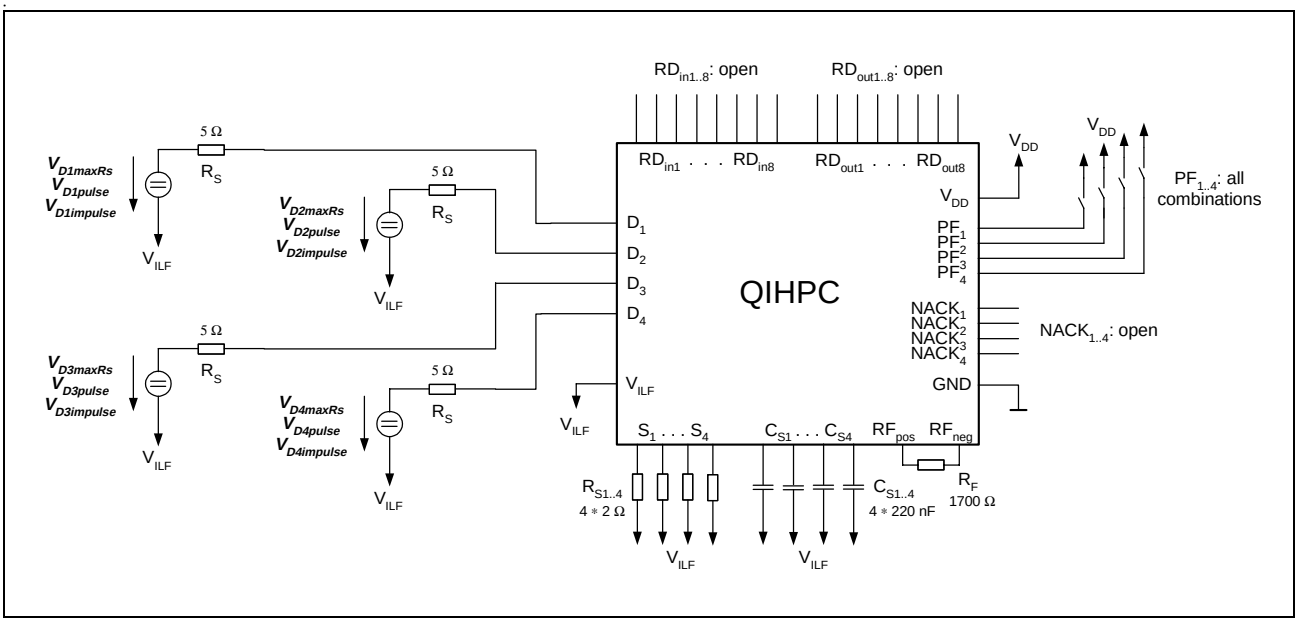
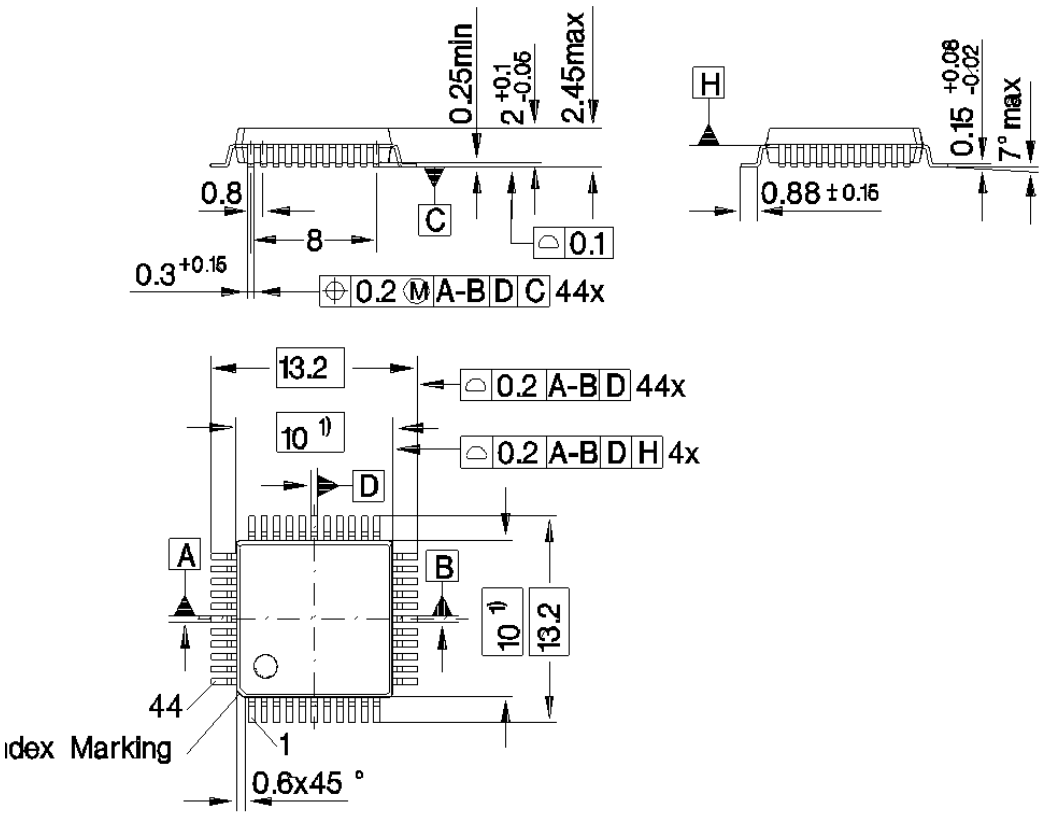


Figure 15 Test circuit for maximum DC-voltages, pulse voltages and impulse voltages on pins $D_{1..4}$

7 Package Outlines

P-MQFP-44
(Plastic Metric Quad Flat Package)



Does not include plastic or metal protrusion of 0.25 max. per side

Sorts of Packing

Package outlines for tubes, trays etc. are contained in our

SMD = Surface Mounted Device

Dimensions in mm