# Wideband, 38 dB Isolation at 1 GHz, CMOS 1.65 V to 2.75 V, SPST Switch

Enhanced Product

**ADG901-EP**

## FEATURES

- Wideband switch: −3 dB at 4.5 GHz
- Absorptive switch
- High off isolation: 38 dB at 1 GHz
- Low insertion loss: 0.8 dB at 1 GHz
- Single 1.65 V to 2.75 V power supply
- CMOS/LVTTL control logic
- Tiny 3 mm × 3 mm LFCSP package
- Low power consumption (<2.5 µA)

## ENHANCED PRODUCT FEATURES

- Supports defense and aerospace applications (AQEC standard)
- Military temperature range: −55°C to +125°C
- Controlled manufacturing baseline
- 1 assembly/test site
- 1 fabrication site
- Enhanced product change notification
- Qualification data available on request

## APPLICATIONS

- Wireless communications
- General-purpose radio frequency (RF) switching
- Dual-band applications
- High speed filter selection
- Digital transceiver front-end switch
- IF switching
- Tuner modules
- Antenna diversity switching list

## GENERAL DESCRIPTION

The ADG901-EP is a wideband switch that uses a CMOS process to provide high isolation and low insertion loss to 1 GHz. The ADG901-EP is an absorptive (matched) switch with 50 Ω terminated shunt legs. This switch is designed such that the isolation is high over the dc to 1 GHz frequency range. The ADG901-EP has on-board CMOS control logic, thus eliminating the need for external controlling circuitry. The control inputs are both CMOS and LVTTL compatible. The low power consumption of this CMOS device makes it ideally suited to wireless applications and general-purpose high frequency switching.

Additional application and technical information can be found in the ADG901 data sheet.

## FUNCTIONAL BLOCK DIAGRAM

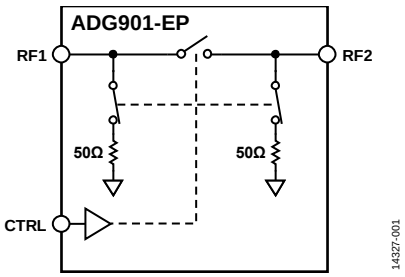


*Figure 1.*

## PRODUCT HIGHLIGHTS

1. −38 dB Off Isolation at 1 GHz
2. 0.8 dB Insertion Loss at 1 GHz
3. Tiny 8-Lead LFCSP Package

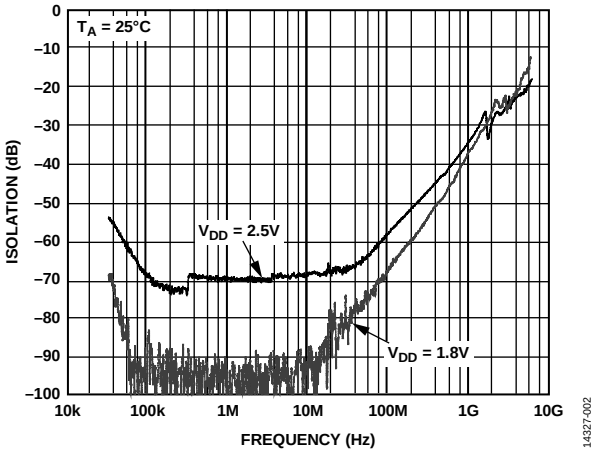


*Figure 2. Off Isolation vs. Frequency*

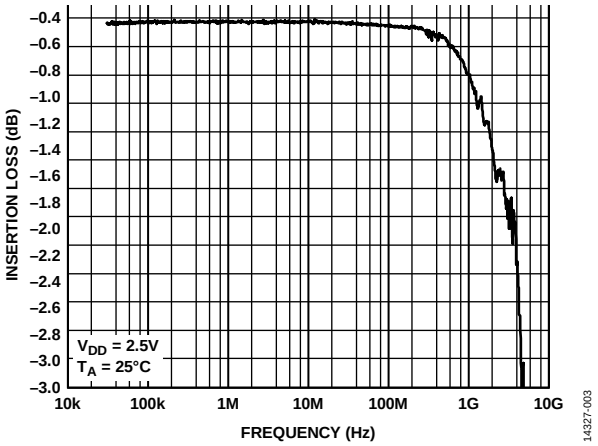


*Figure 3. Insertion Loss vs. Frequency*

Rev. A

Document Feedback



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## REVISION HISTORY

**12/2016—Rev. 0 to Rev. A**

Change to Product Title ..... 1

**9/2016—Revision 0: Initial Version**

# SPECIFICATIONS

$V_{DD}$ = 1.65 V to 2.75 V, GND = 0 V, input power = 0 dBm, temperature range = −55°C to +125°C, unless otherwise noted.

**Table 1.**

| Parameter | Symbol | Test Conditions/Comments | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|---|
| AC ELECTRICAL CHARACTERISTICS | | | | | | |
| −3 dB Frequency[2] | | | | 4.5 | | GHz |
| Insertion Loss | $S_{21}$, $S_{12}$ | DC to 100 MHz; $V_{DD}$ = 2.5 V ± 10%, see Figure 19 | | 0.4 | 0.7 | dB |
| | | 500 MHz; $V_{DD}$ = 2.5 V ± 10% | | 0.6 | 1 | dB |
| | | 1000 MHz; $V_{DD}$ = 2.5 V ± 10% | | 0.8 | 1.25 | dB |
| Isolation—RF1 to RF2 | $S_{21}$, $S_{12}$ | 100 MHz | 55 | 61 | | dB |
| | | 500 MHz | 40 | 45 | | dB |
| | | 1000 MHz | 31 | 38 | | dB |
| Return Loss (On Channel)[2] | $S_{11}$, $S_{22}$ | DC to 100 MHz | 18 | 28 | | dB |
| | | 500 MHz | | 25 | | dB |
| | | 1000 MHz | | 20 | | dB |
| Return Loss (Off Channel)[2] | $S_{11}$, $S_{22}$ | DC to 100 MHz | 15 | 23 | | dB |
| | | 500 MHz | | 21 | | dB |
| | | 1000 MHz | | 19 | | dB |
| On Switching Time[2] | $t_{ON}$ | 50% CTRL to 90% RF, see Figure 16 | | 4 | 6.5 | ns |
| Off Switching Time[2] | $t_{OFF}$ | 50% CTRL to 10% RF, see Figure 16 | | 6.5 | 10.5 | ns |
| Rise Time[2] | $t_{RISE}$ | 10% to 90% RF, see Figure 17 | | 3.1 | 5.5 | ns |
| Fall Time[2] | $t_{FALL}$ | 90% to 10% RF, see Figure 17 | | 6.0 | 9.5 | ns |
| Third-Order Intermodulation Intercept | IP3 | 900 MHz/901 MHz, 4 dBm, see Figure 21 | 28.5 | 36 | | dBm |
| Video Feedthrough[3] | | See Figure 20 | | 2.5 | | mV p-p |
| INPUT POWER | | | | | | |
| 1 dB Input Compression[4] | P1dB | 1000 MHz; see Figure 22 | | 17 | | dBm |
| DC ELECTRICAL CHARACTERISTICS | | | | | | |
| Input High Voltage | $V_{INH}$ | $V_{DD}$ = 2.25 V to 2.75 V | 1.7 | | | V |
| | $V_{INH}$ | $V_{DD}$ = 1.65 V to 1.95 V | 0.65 $V_{DD}$ | | | V |
| Input Low Voltage | $V_{INL}$ | $V_{DD}$ = 2.25 V to 2.75 V | | | 0.7 | V |
| | $V_{INL}$ | $V_{DD}$ = 1.65 V to 1.95 V | | | 0.35 $V_{DD}$ | V |
| Input Leakage Current | $I_I$ | 0 ≤ $V_{IN}$ ≤ 2.75 V | | ±0.1 | ±1 | µA |
| CAPACITANCE[2] | | | | | | |
| RF1/RF2, RF Port On Capacitance | $C_{RF}$ on | f = 1 MHz | | 1.2 | | pF |
| CTRL Input Capacitance | $C_{CTRL}$ | f = 1 MHz | | 2.1 | | pF |
| POWER REQUIREMENTS | | | | | | |
| $V_{DD}$ | | | 1.65 | | 2.75 | V |
| Quiescent Power Supply Current | $I_{DD}$ | Digital inputs = 0 V or $V_{DD}$ | | 0.1 | 2.5 | µA |

[1] Typical values are at $V_{DD}$ = 2.5 V and 25°C, unless otherwise specified.
[2] Guaranteed by design, not subject to production test.
[3] Video feedthrough is the dc transience at the output of any port of the switch when the control voltage is switched from high to low or low to high in a 50 Ω test setup, measured with 1 ns rise time pulses and 500 MHz bandwidth.
[4] For less than 100 MHz, refer to the AN-952 Application Note for more information about power handling.

## CONTINOUS CURRENT PER CHANNEL

**Table 2.**

| Parameter | 25°C | 85°C | 105°C | 125°C | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|---|
| CONTINUOUS CURRENT PER CHANNEL[1] | | | | | | 8-lead LFCSP, $\theta_{JA}$ = 48°C/W, dc bias = 0.5 V |
| $V_{DD}$ = 2.75 V, $V_{SS}$ = 0 V | 70 | 7 | 3.85 | 2.8 | mA maximum | |
| $V_{DD}$ = 1.65 V, $V_{SS}$ = 0 V | 56 | 7 | 3.85 | 2.8 | mA maximum | |

[1] Guaranteed by design, not subject to production test.

# ABSOLUTE MAXIMUM RATINGS

$T_A$ = 25°C, unless otherwise specified.

**Table 3.**

| Parameter | Rating |
|---|---|
| $V_{DD}$ to GND[1] | −0.5 V to +4 V |
| Inputs to GND[1, 2] | −0.5 V to $V_{DD}$ + 0.3 V |
| Continuous Current | Data[3] + 15% |
| Input Power[4] | 18 dBm |
| Operating Temperature Range (Industrial) | −55°C to +125°C |
| Storage Temperature Range | −65°C to +150°C |
| Junction Temperature | 150°C |
| Lead Temperature, Soldering (10 sec) | 300°C |
| IR Reflow, Peak Temperature (<20 sec) | 235°C |
| ESD | 1 kV |

[1] Tested at 125°C.
[2] When RF1 and RF2 are in the open position, the input to ground rating is −0.5 V to $V_{DD}$ − 0.5 V.
[3] See Table 2.
[4] The switch is tested in both the open and closed positions. In the closed condition, power is applied to RF1, and RF2 is terminated to a 50 Ω resistor to GND. In the open condition, power is applied to RF1 and RF2.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

**Table 4. Thermal Resistance**

| Package Type | $\theta_{JA}$ | $\theta_{JC}$ | Unit |
|---|---|---|---|
| CP-8-13[1] | 48 | 1 | °C/W |

[1] Test condition: thermal impedance simulated values are based on JEDEC 2S2P thermal test board with four thermal vias. See JEDEC JESD51.

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

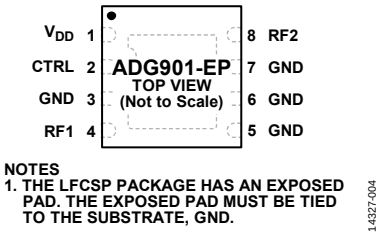


*Figure 4. 8-Lead LFCSP Pin Configuration*

**Table 5. Pin Function Descriptions**

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1 | $V_{DD}$ | Power Supply Input. These devices can be operated from 1.65 V to 2.75 V; decouple $V_{DD}$ to GND. |
| 2 | CTRL | CMOS or LVTTL Logic Level. CTRL input must not exceed $V_{DD}$. |
| | | Logic 0: RF1 isolated from RF2. |
| | | Logic 1: RF1 to RF2. |
| 3, 5, 6, 7 | GND | Ground Reference Point for All Circuitry on the Device. |
| 4 | RF1 | RF1 Port. |
| 8 | RF2 | RF2 Port. |
| | EPAD | Exposed Pad. The LFCSP package has an exposed pad. The exposed pad must be tied to the substrate, GND. |

**Table 6. Truth Table**

| CTRL | Signal Path |
|---|---|
| 0 | RF1 isolated from RF2 |
| 1 | RF1 to RF2 |

# TYPICAL PERFORMANCE CHARACTERISTICS

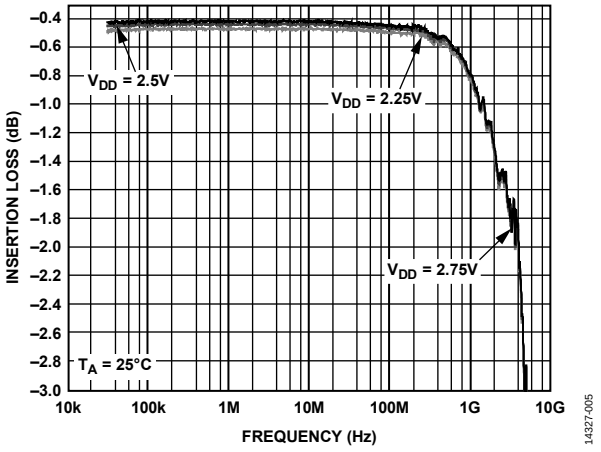


*Figure 5. Insertion Loss vs. Frequency over Supplies ($S_{12}$ and $S_{21}$)*

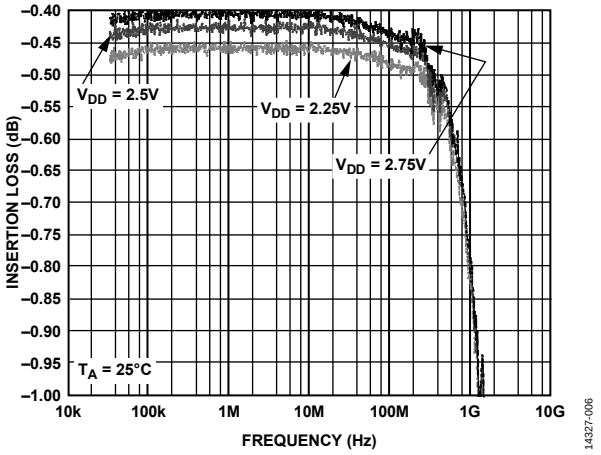


*Figure 6. Insertion Loss vs. Frequency over Supplies ($S_{12}$ and $S_{21}$) (Zoomed Figure 5 Plot)*

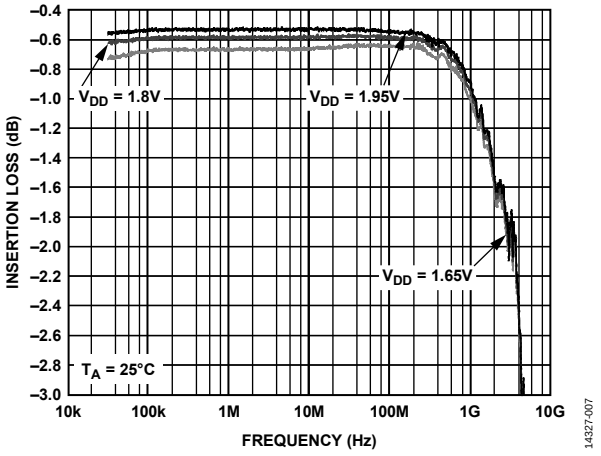


*Figure 7. Insertion Loss vs. Frequency over Supplies ($S_{12}$ and $S_{21}$)*

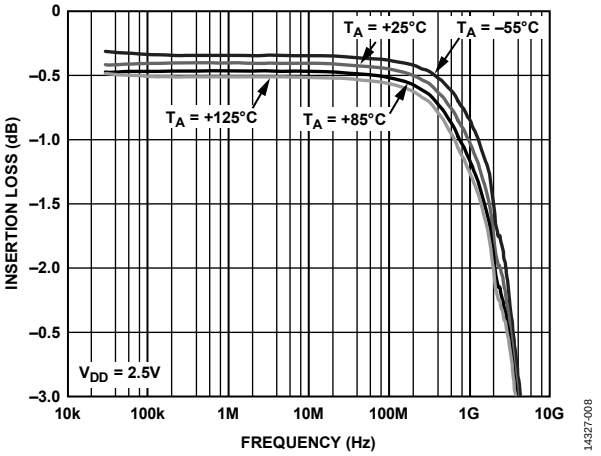


*Figure 8. Insertion Loss vs. Frequency over Temperature ($S_{12}$ and $S_{21}$)*

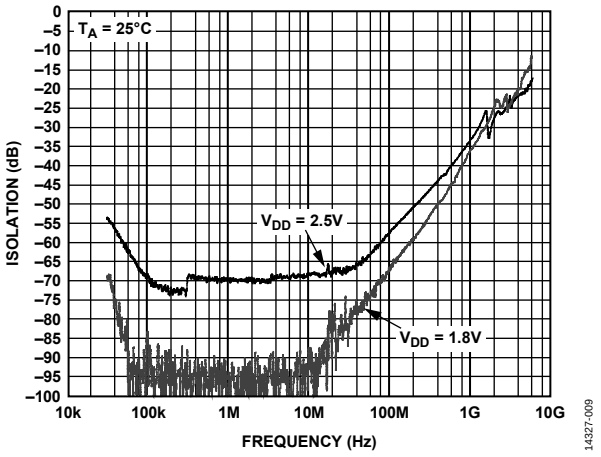


*Figure 9. Off Isolation vs. Frequency over Supplies ($S_{12}$ and $S_{21}$)*

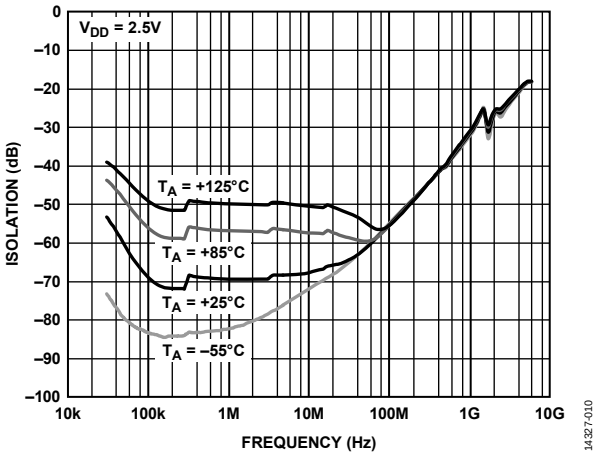


*Figure 10. Off Isolation vs. Frequency over Temperature ($S_{12}$ and $S_{21}$)*

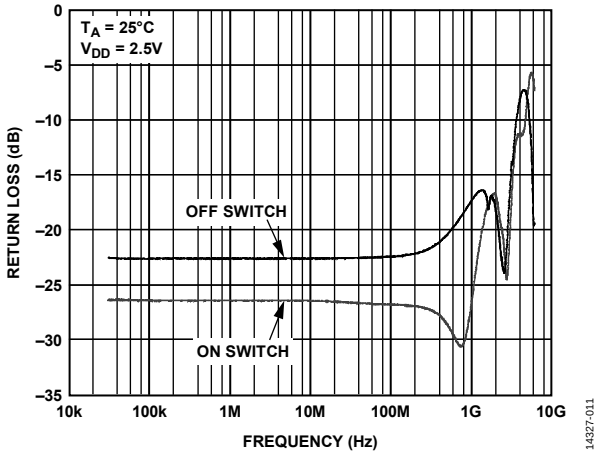


*Figure 11. Return Loss vs. Frequency ($S_{11}$)*

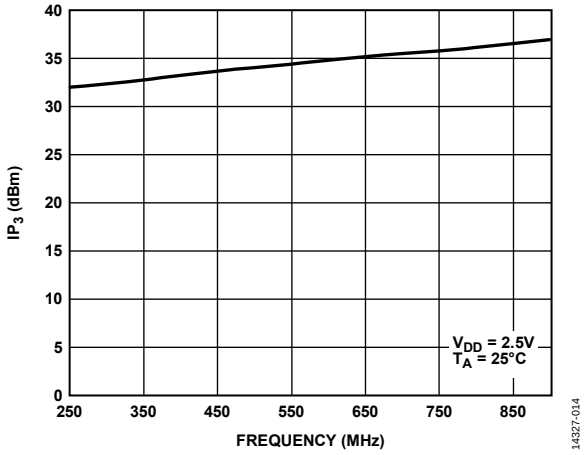


*Figure 14. $IP_3$ vs. Frequency*

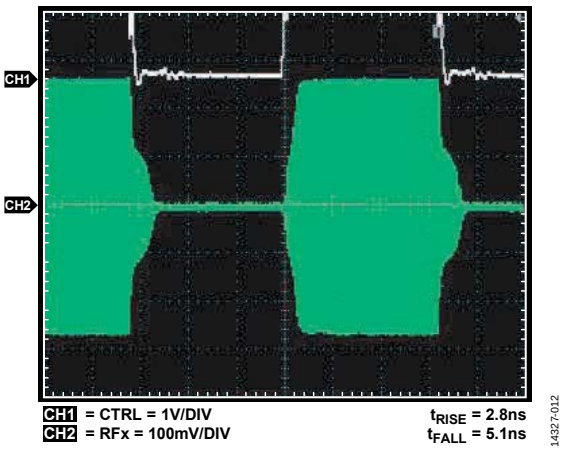


*Figure 12. Switch Timing*

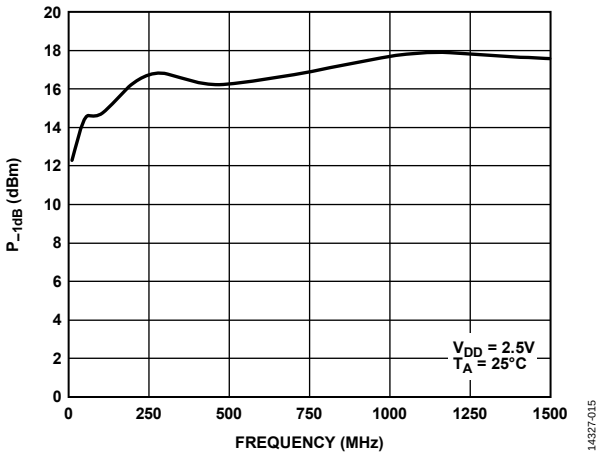


*Figure 15. P1dB vs. Frequency (DC Bias Not Used)*

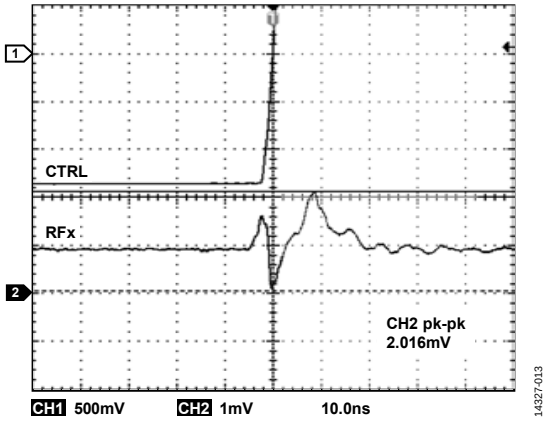


*Figure 13. Video Feedthrough*

# TERMINOLOGY

**$V_{DD}$**
Most positive power supply potential.

**$I_{DD}$**
Positive supply current.

**GND**
Ground (0 V) reference.

**CTRL**
Logic control input.

**$V_{INL}$**
Maximum input voltage for Logic 0.

**$V_{INH}$**
Minimum input voltage for Logic 1.

**$I_{IN}L$ ($I_{INH}$)**
Input current of the digital input.

**$C_{IN}$**
Digital input capacitance.

**$t_{ON}$**
Delay between applying the digital control input and the output switching on.

**$t_{OFF}$**
Delay between applying the digital control input and the output switching off.

**$t_{RISE}$**
Rise time. Time for the RF signal to rise from 10% to 90% of the on level.

**$t_{FALL}$**
Fall time. Time for the RF signal to fall from 90% to 10% of the on level.

**Off Isolation**
The attenuation between input and output ports of the switch when the switch control voltage is in the off condition.

**Insertion Loss**
The attenuation between input and output ports of the switch when the switch control voltage is in the on condition.

**P1dB**
1 dB compression point. The RF input power level at which the switch insertion loss increases by 1 dB over its low level value. It is a measure of how much power the on switch can handle before the insertion loss increases by 1 dB.

**$IP_3$**
Third-order intermodulation intercept. This is a measure of the power in false tones that occur when closely spaced tones are passed through a switch, whereby the nonlinearity of the switch causes these false tones to be generated.

**Return Loss**
The amount of reflected power relative to the incident power at a port. Large return loss indicates good matching. By measuring return loss the VSWR can be calculated from conversion charts. voltage standing wave ratio (VSWR) indicates the degree of matching present at a switch RF port.

**Video Feedthrough**
The spurious signals present at the RF ports of the switch when the control voltage is switched from high to low or low to high without an RF signal present.

# TEST CIRCUITS

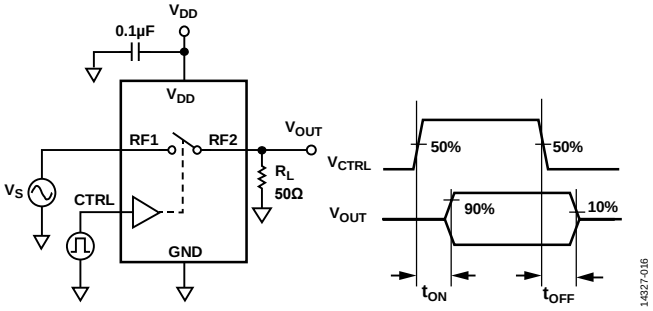


*Figure 16. Switching Timing: $t_{ON}$, $t_{OFF}$*

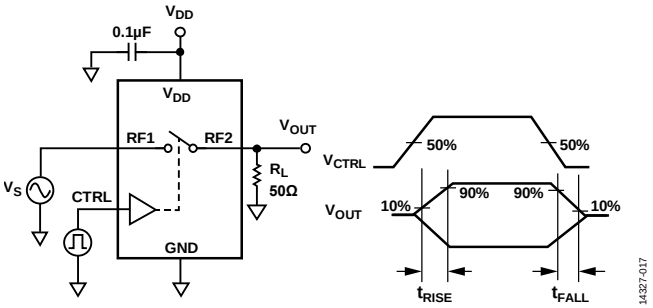


*Figure 17. Switch Timing: $t_{RISE}$, $t_{FALL}$*

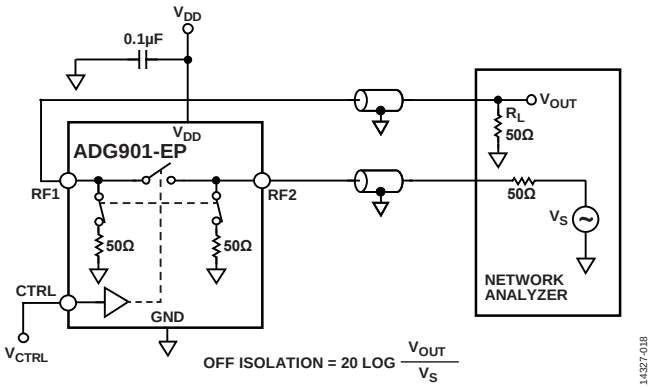


*Figure 18. Off Isolation*

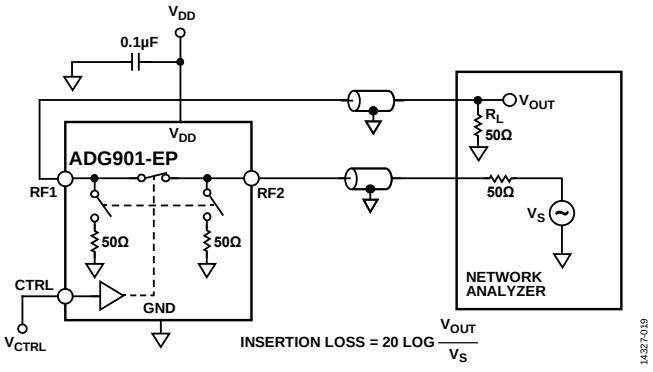


*Figure 19. Insertion Loss*

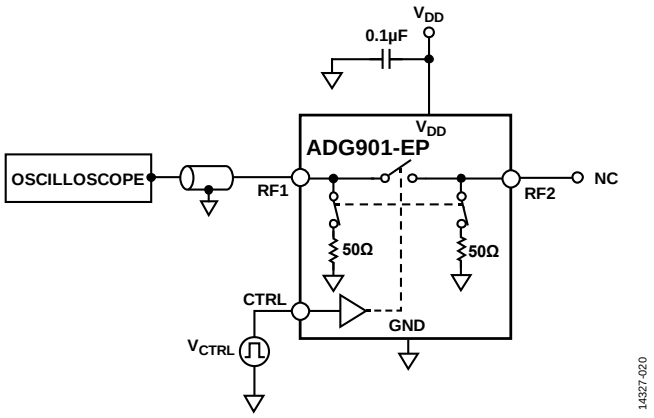


*Figure 20. Video Feedthrough*

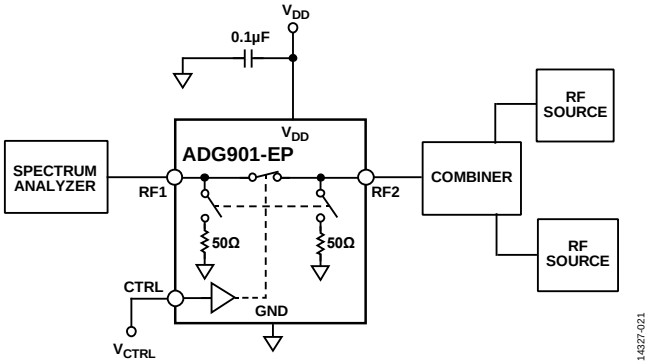


*Figure 21. IP3*

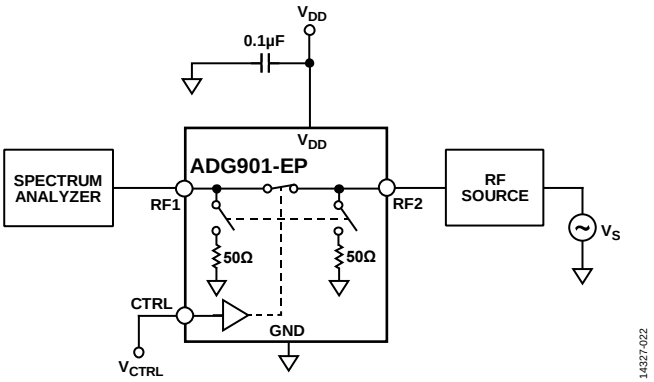


*Figure 22. P1dB*

# OUTLINE DIMENSIONS

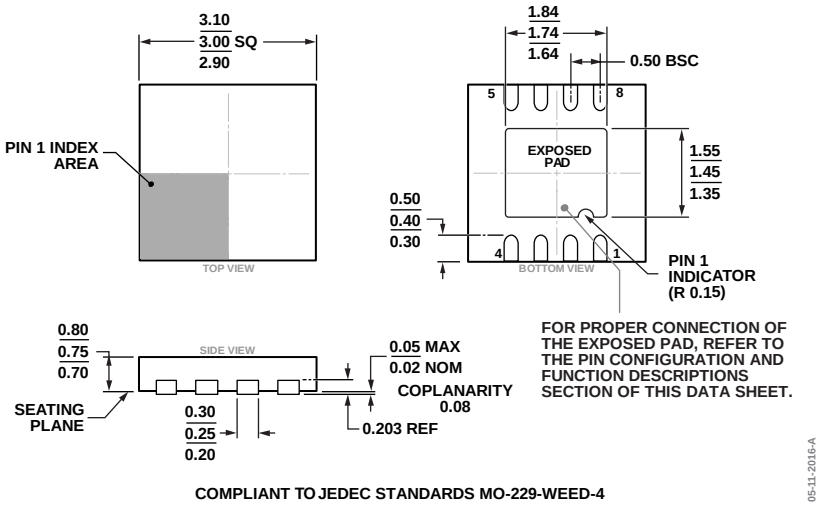


*Figure 23. 8-Lead Lead Frame Chip Scale Package [LFCSP]*
*3 mm × 3 mm Body and 0.75 mm Package Height*
*(CP-8-13)*
*Dimensions shown in millimeters*

## ORDERING GUIDE

| Model[1] | Temperature Range | Package Description | Package Option | Branding |
|---|---|---|---|---|
| ADG901SCPZ-EP | −55°C to +125°C | 8-Lead Lead Frame Chip Scale Package [LFCSP] | CP-8-13 | S4K |
| ADG901SCPZ-EP-RL7 | −55°C to +125°C | 8-Lead Lead Frame Chip Scale Package [LFCSP] | CP-8-13 | S4K |

[1] Z = RoHS Compliant Part.


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