TS4995

1.2 W fully differential audio power amplifier with selectable standby and 6 dB fixed gain

Features

- Differential inputs
- 90 dB PSRR @ 217 Hz with grounded inputs
- Operates from V_{CC} = 2.5 V to 5.5 V
- 1.2 W rail-to-rail output power @ V_{CC}=5 V, THD+N=1%, F=1 kHz, with an 8 Ω load
- 6 dB integrated fixed gain
- Ultra-low consumption in standby mode (10 nA)
- Selectable standby mode (active low or active high)
- Ultra-fast startup time: 10 ms typ. at V_{CC}=3.3 V
- Available in 9-bump flip chip (300 mm bump diameter)
- Ultra-low pop and click

Applications

- Mobile phones (cellular / cordless)
- PDAs
- Laptop / notebook computers
- Portable audio devices

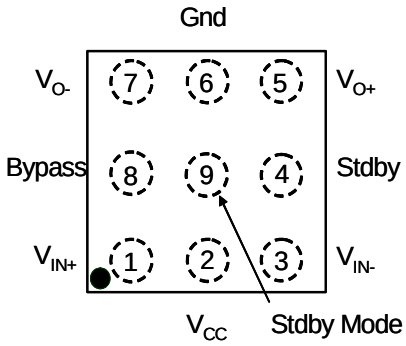
Description

The TS4995 is an audio power amplifier capable of delivering 1.2 W of continuous RMS output power into an 8 Ω load at 5 V. Thanks to its differential inputs, it exhibits outstanding noise immunity.

An external standby mode control reduces the supply current to less than 10 nA. A STBY MODE pin allows the standby pin to be active **high** or **low**. An internal thermal shutdown protection is also provided, making the device capable of sustaining short-circuits.

TS4995 - Flip chip 9

Pin connections (top view)



The TS4995 features an internal fixed gain at 6dB which reduces the number of external components on the application board.

The device is equipped with common mode feedback circuitry allowing outputs to be always biased at V_{CC}/2 regardless of the input common mode voltage.

The TS4995 is specifically designed for high quality audio applications such as mobile phones and requires few external components.

Contents

1 Absolute maximum ratings and operating conditions

Table 1. Absolute maximum ratings (AMR)

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage (1)	6	V
V_{in}	Input voltage (2)	GND to V_{CC}	V
T_{oper}	Operating free air temperature range	-40 to + 85	°C
T_{stg}	Storage temperature	-65 to +150	°C
T_j	Maximum junction temperature	150	°C
R_{thja}	Thermal resistance junction to ambient (3)	200	°C/W
P_{diss}	Power dissipation	Internally limited	W
ESD	MM: machine model (4)	200	V
	HBM: human body model (5)	1.5	kV
Latch-up	Latch-up immunity	200	mA
-	Lead temperature (soldering, 10sec)	260	°C

1. All voltage values are measured with respect to the ground pin.
2. The magnitude of input signal must never exceed V_{CC} + 0.3 V / GND - 0.3 V.
3. The device is protected in case of over temperature by a thermal shutdown activated at 150° C.
4. Machine model: a 200 pF cap is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5 Ω), done for all couples of pin combinations with other pins floating.
5. Human body model: 100 pF discharged through a 1.5 kΩ resistor between two pins of the device, done for all couples of pin combinations with other pins floating.

Table 2. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	2.5 to 5.5	V
V_{SM}	Standby mode voltage input: Standby Active LOW Standby Active HIGH	 V_{SM}=GND V_{SM}=V_{CC}	V
V_{STBY}	Standby voltage input: Device ON (V_{SM}=GND) or Device OFF (V_{SM}=V_{CC}) Device OFF (V_{SM}=GND) or Device ON (V_{SM}=V_{CC})	 $1.5 \leq V_{STBY} \leq V_{CC}$ $GND \leq V_{STBY} \leq 0.4$ (1)	V
T_{SD}	Thermal shutdown temperature	150	°C
R_L	Load resistor	≥ 4	Ω
R_{thja}	Thermal resistance junction to ambient	100	°C/W

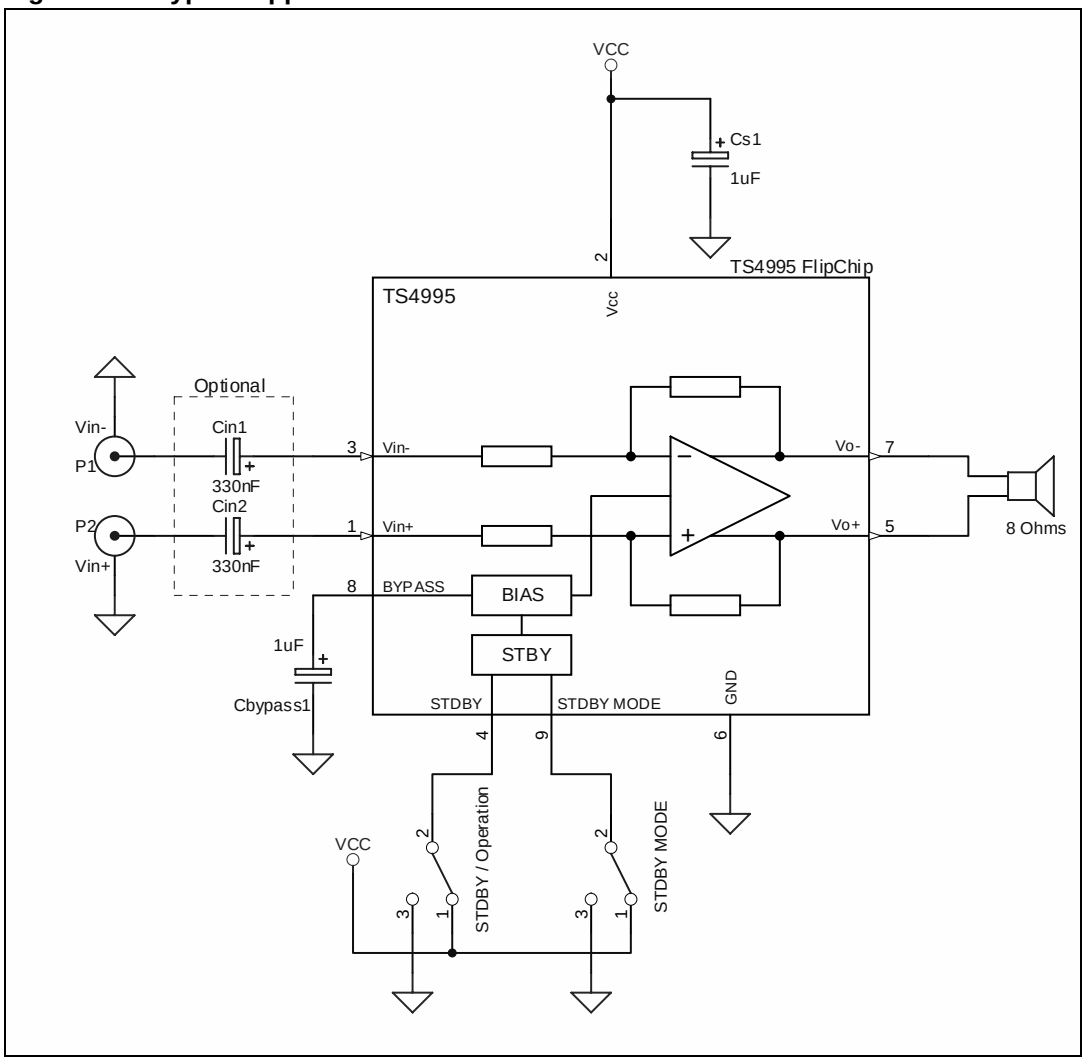
1. The minimum current consumption (I_{STBY}) is guaranteed when $V_{STB\ Y}$= GND or V_{CC} (the supply rails) for the whole temperature range.

2 Typical application schematics

Table 3. External component descriptions

Component	Functional description
C_s	Supply bypass capacitor that provides power supply filtering.
C_b	Bypass capacitor that provides half supply filtering.
C_{in}	Optional input capacitor that forms a high pass filter together with R_{in}. ($F_{cl} = 1 / (2 \times \pi \times R_{in} \times C_{in})$

Figure 1. Typical application



3 Electrical characteristics

Table 4. V_{CC} = +5V, GND = 0V, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{CC}	Supply current	No input signal, no load		4	7	mA
I_{STBY}	Standby current	No input signal, V_{STBY} = V_{SM} = GND, R_L = 8Ω No input signal, V_{STBY} = V_{SM} = V_{CC}, R_L = 8Ω		10	1000	nA
V_{oo}	Differential output offset voltage	No input signal, R_L = 8Ω		0.1	10	mV
V_{IC}	Input common mode voltage		0		4.5	V
P_o	Output power	THD = 1% Max, F= 1kHz, R_L = 8Ω	0.8	1.2		W
THD + N	Total harmonic distortion + noise	P_o = 850mW rms, 20Hz ≤ F ≤ 20kHz, R_L = 8Ω		0.5		%
$PSRR_{IG}$	Power supply rejection ratio with inputs grounded(1)	F = 217Hz, R = 8Ω, C_{in} = 4.7µF, C_b =1µF V_{ripple} = 200mV_{PP}	75(2)	90		dB
CMRR	Common mode rejection ratio	F = 217Hz, R_L = 8Ω, C_{in} = 4.7µF, C_b =1µF V_{ic} = 200mV_{PP}		60		dB
SNR	Signal-to-noise ratio	**A-weighted filter** R_L = 8Ω, THD +N < 0.7%, 20Hz ≤ F ≤ 20kHz		100		dB
GBP	Gain bandwidth product	R_L = 8Ω		2		MHz
V_N	Output voltage noise	**20Hz ≤ F ≤ 20kHz, R_L = 8Ω** Unweighted A-weighted Unweighted, standby A-weighted, standby		 11 7 3.5 1.5		μV_{RMS}
Z_{in}	Input impedance		15	20	25	kΩ
-	Gain mismatch		5.5	6	6.5	dB
t_{WU}	Wake-up time(3)	C_b =1µF		15		ms

1. Dynamic measurements - 20*log(rms(V_{out})/rms (V_{ripple})). V_{ripple} is the super-imposed sinus signal relative to V_{CC}.
2. Guaranteed by design and evaluation.
3. Transition time from standby mode to fully operational amplifier.

Table 5. V_{CC} = +3.3V (all electrical values are guaranteed with correlation measurements at 2.6V and 5V), GND = 0V, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{CC}	Supply current	No input signal, no load		3	7	mA
I_{STBY}	Standby current	No input signal, V_{STBY} = V_{SM} = GND, R_L = 8Ω No input signal, V_{STBY} = V_{SM} = V_{CC}, R_L = 8Ω		10	1000	nA
V_{oo}	Differential output offset voltage	No input signal, R_L = 8Ω		0.1	10	mV
V_{IC}	Input common mode voltage		0.4		2.3	V
P_o	Output power	THD = 1% max, F= 1kHz, R_L = 8Ω	300	500		mW
THD + N	Total harmonic distortion + noise	P_o = 300mW rms, 20Hz ≤ F ≤ 20kHz, R_L = 8Ω		0.5		%
$PSRR_{IG}$	Power supply rejection ratio with inputs grounded(1)	F = 217Hz, R = 8Ω, C_{in} = 4.7µF, C_b =1µF V_{ripple} = 200mV_{PP}	75(2)	90		dB
CMRR	Common mode rejection ratio	F = 217Hz, R_L = 8Ω, C_{in} = 4.7µF, C_b =1µF V_{ic} = 200mV_{PP}		60		dB
SNR	Signal-to-noise ratio	**A-weighted filter** R_L = 8Ω, THD +N < 0.7%, 20Hz ≤ F ≤ 20kHz		100		dB
GBP	Gain bandwidth product	R_L = 8Ω		2		MHz
V_N	Output voltage noise	**20Hz ≤ F ≤ 20kHz, R_L = 8Ω** Unweighted A weighted Unweighted, standby A weighted, standby		 11 7 3.5 1.5		μV_{RMS}
Z_{in}	Input impedance		15	20	25	kΩ
-	Gain mismatch		5.5	6	6.5	dB
t_{WU}	Wake-up time(3)	C_b =1µF		10		ms

1. Dynamic measurements - 20*log(rms(V_{out})/rms (V_{ripple})). V_{ripple} is the super-imposed sinus signal relative to V_{CC}.
2. Guaranteed by design and evaluation.
3. Transition time from standby mode to fully operational amplifier.

Table 6. V_{CC} = +2.6V, GND = 0V, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{CC}	Supply current	No input signal, no load		3	7	mA
I_{STBY}	Standby current	No input signal, V_{STBY} = V_{SM} = GND, R_L = 8Ω No input signal, V_{STBY} = V_{SM} = V_{CC}, R_L = 8Ω		10	1000	nA
V_{oo}	Differential output offset voltage	No input signal, R_L = 8Ω		0.1	10	mV
V_{IC}	Input common mode voltage		0.6		1.5	V
P_o	Output power	THD = 1% max, F= 1kHz, R_L = 8Ω	200	300		mW
THD + N	Total harmonic distortion + noise	Po = 225mW rms, 20Hz ≤ F ≤ 20kHz, R_L = 8Ω		0.5		%
$PSRR_{IG}$	Power supply rejection ratio with inputs grounded(1)	F = 217Hz, R = 8Ω, C_{in} = 4.7µF, C_b =1µF V_{ripple} = 200mV_{PP}	75(2)	90		dB
CMRR	Common mode rejection ratio	F = 217Hz, R_L = 8Ω, C_{in} = 4.7µF, C_b =1µF V_{ic} = 200mV_{PP}		60		dB
SNR	Signal-to-noise ratio	**A-weighted filter** R_L = 8Ω, THD +N < 0.7%, 20Hz ≤ F ≤ 20kHz		100		dB
GBP	Gain bandwidth product	R_L = 8Ω		2		MHz
V_N	Output voltage noise	**20Hz ≤F ≤20kHz, R_L = 8Ω** Unweighted A weighted Unweighted, standby A weighted, standby		 11 7 3.5 1.5		μV_{RMS}
Z_{in}	Input impedance		15	20	25	kΩ
-	Gain mismatch		5.5	6	6.5	dB
t_{WU}	Wake-up time(3)	C_b =1µF		10		ms

1. Dynamic measurements - 20*log(rms(V_{out})/rms (V_{ripple})). V_{ripple} is the super-imposed sinus signal relative to V_{CC}.
2. Guaranteed by design and evaluation.
3. Transition time from standby mode to fully operational amplifier.

Figure 2. THD+N vs. output power

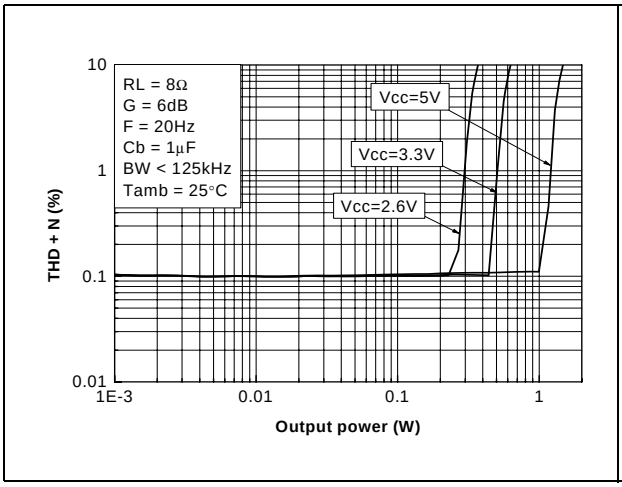


Figure 3. THD+N vs. output power

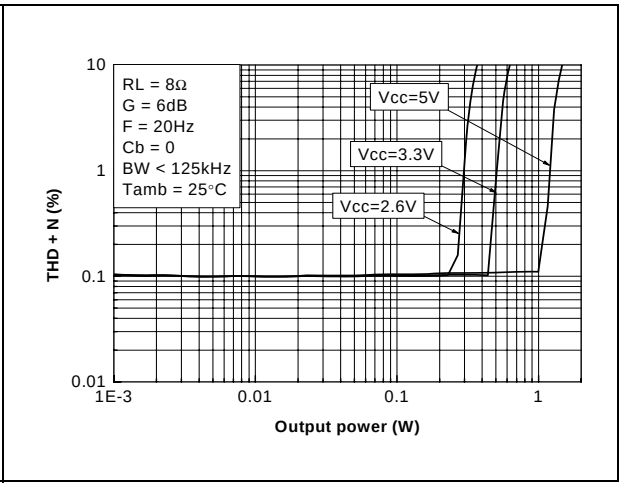


Figure 4. THD+N vs. output power

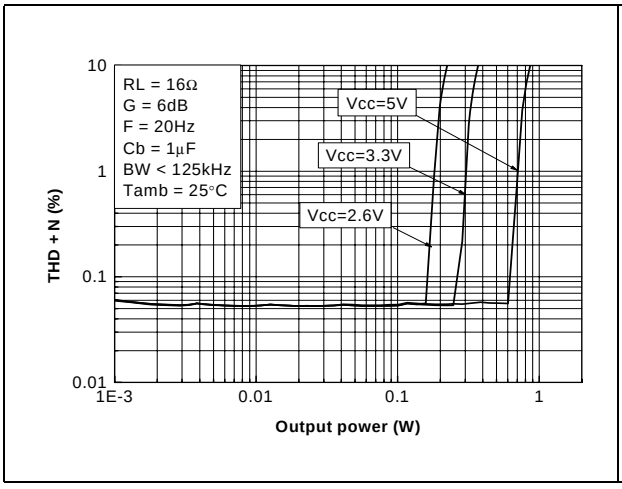


Figure 5. THD+N vs. output power

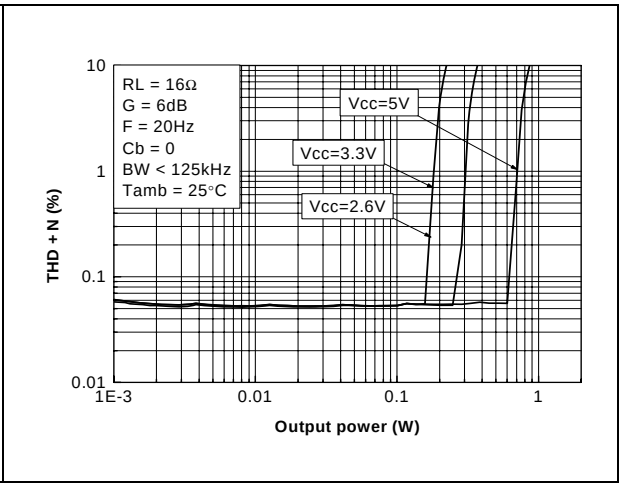


Figure 6. THD+N vs. output power

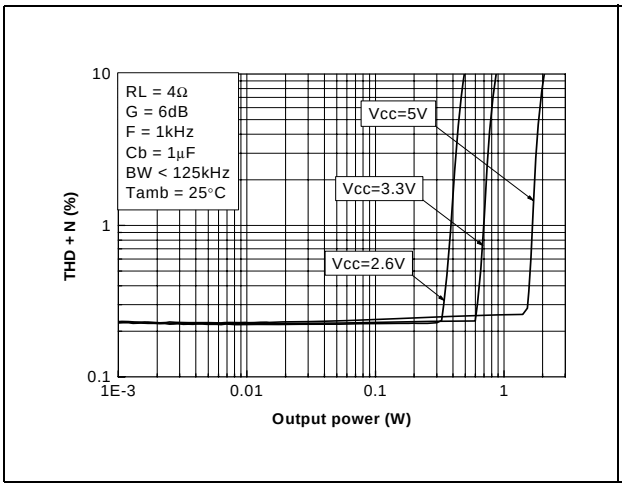


Figure 7. THD+N vs. output power

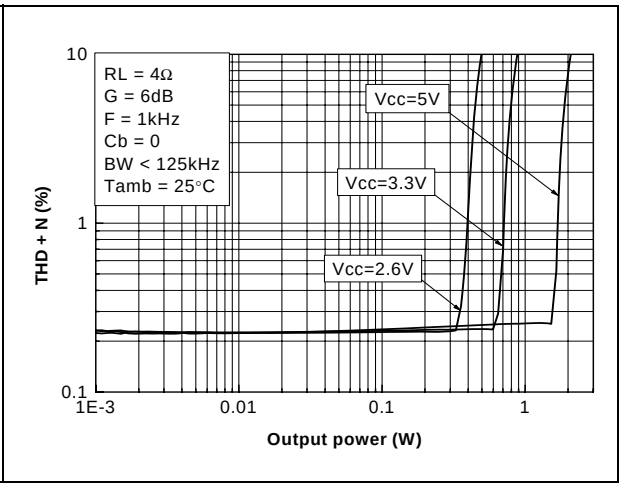


Figure 8. THD+N vs. output power

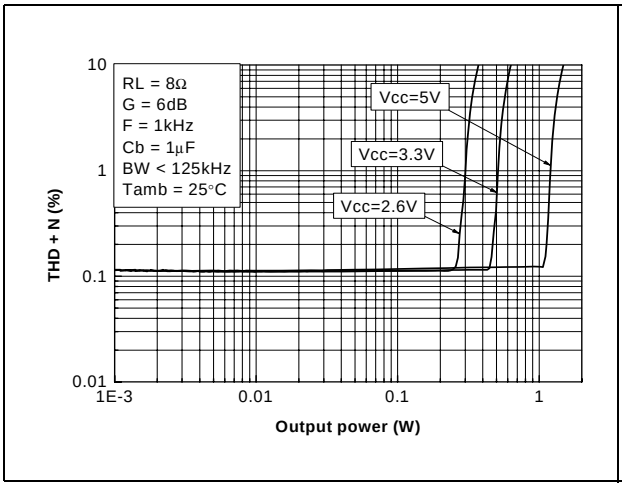


Figure 9. THD+N vs. output power

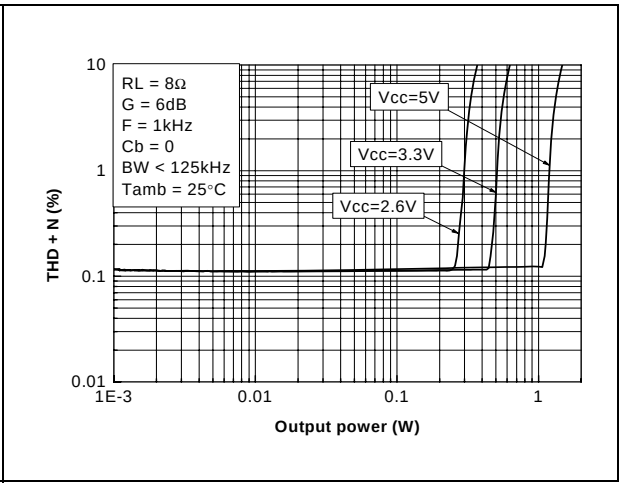


Figure 10. THD+N vs. output power

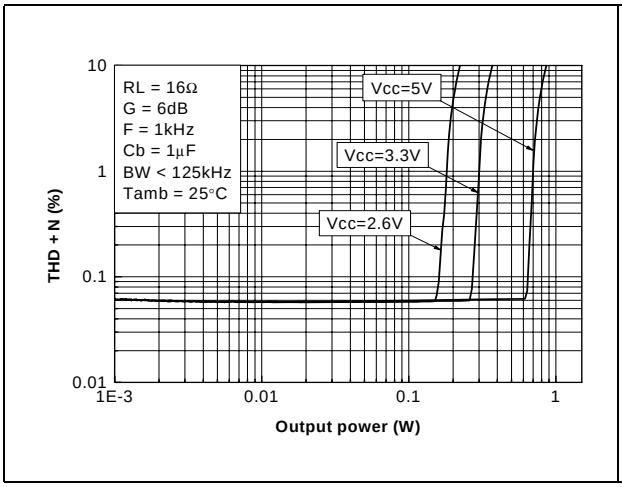


Figure 11. THD+N vs. output power

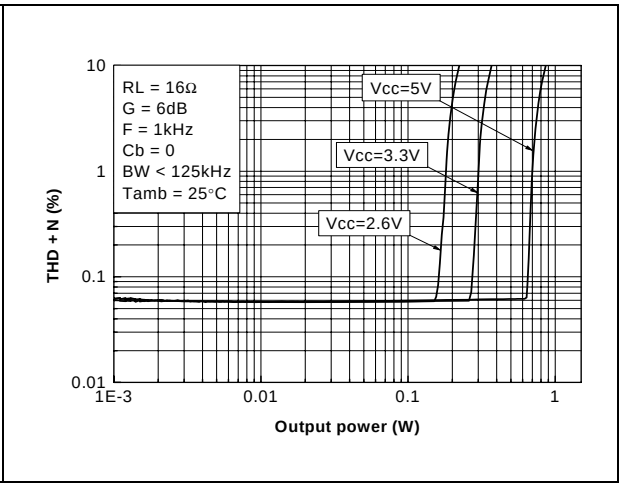


Figure 12. THD+N vs. output power

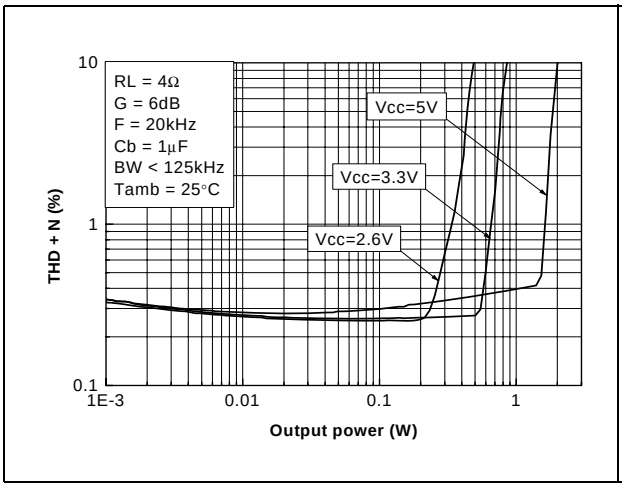


Figure 13. THD+N vs. output power

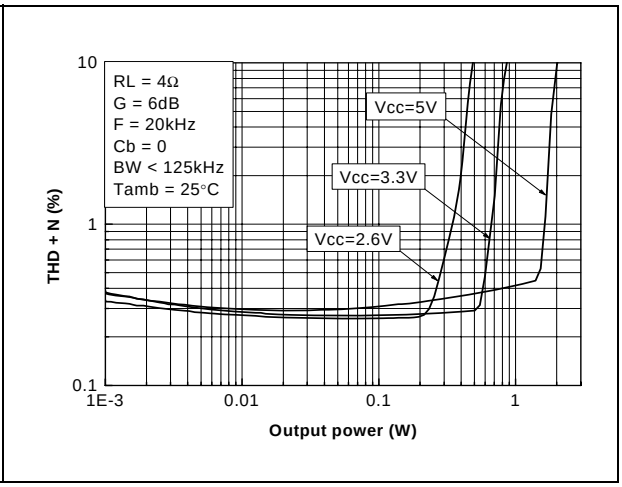


Figure 14. THD+N vs. output power

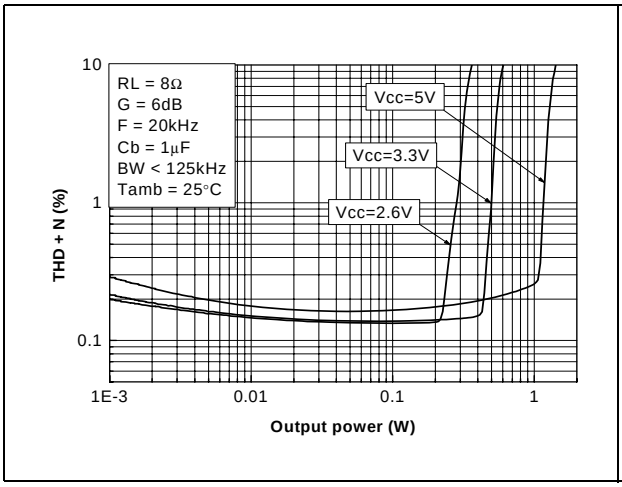


Figure 15. THD+N vs. output power

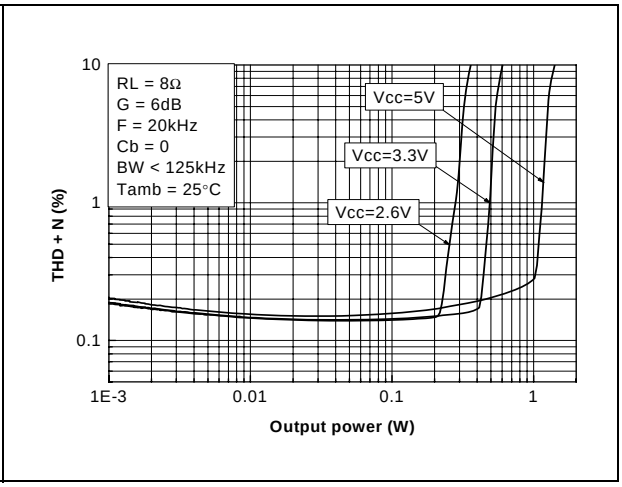


Figure 16. THD+N vs. output power

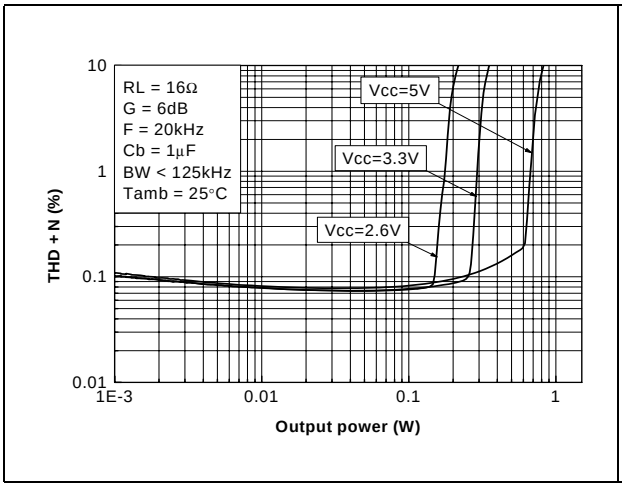


Figure 17. THD+N vs. output power

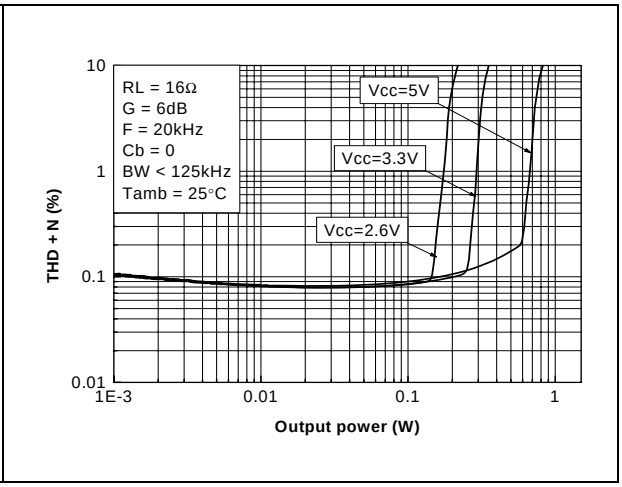


Figure 18. THD+N vs. frequency

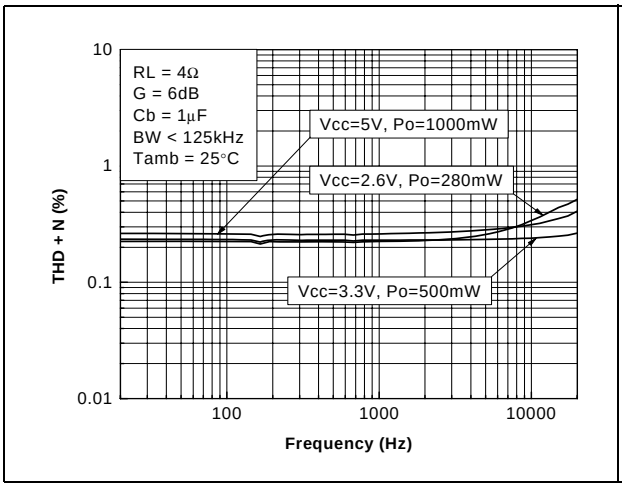


Figure 19. THD+N vs. frequency

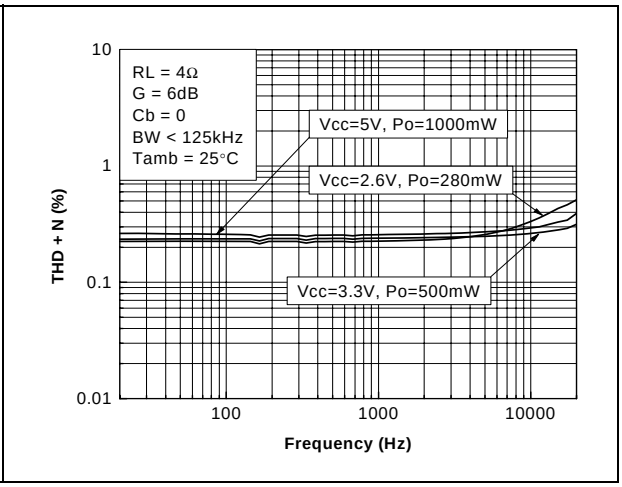


Figure 20. THD+N vs. frequency

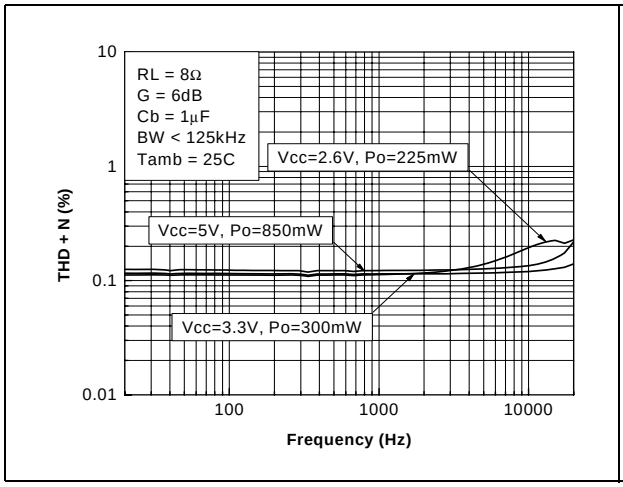


Figure 21. THD+N vs. frequency

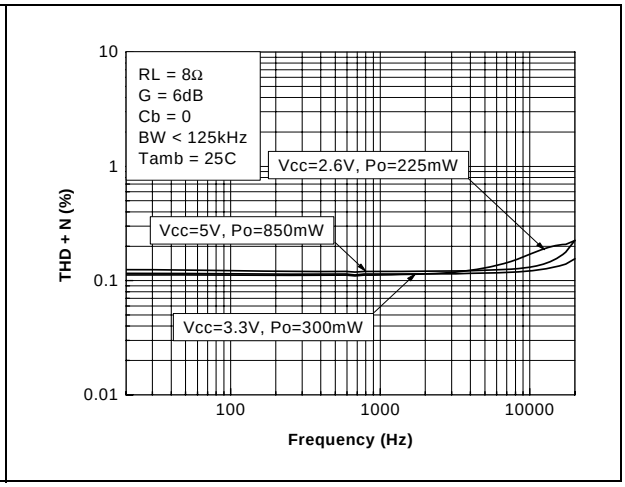


Figure 22. THD+N vs. frequency

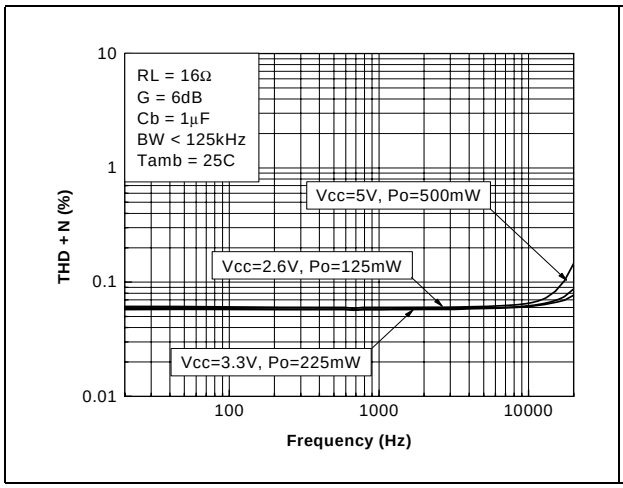


Figure 23. THD+N vs. frequency

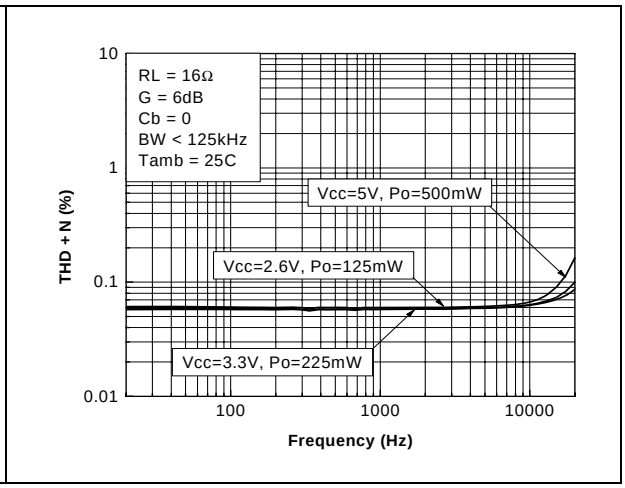


Figure 24. Output power vs. power supply voltage

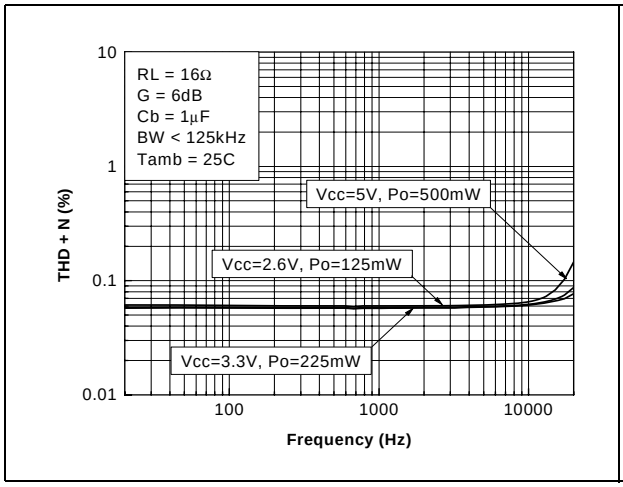


Figure 25. Output power vs. power supply voltage

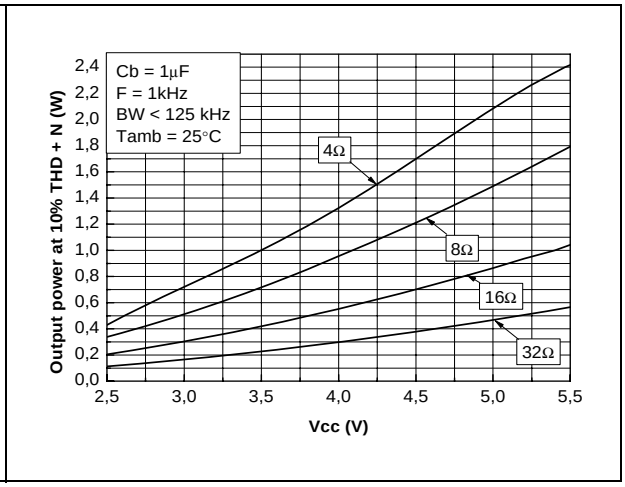


Figure 26. Output power vs. power supply voltage

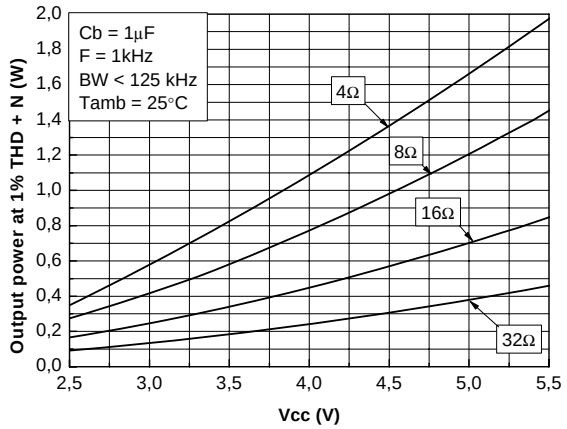


Figure 27. Power derating curves

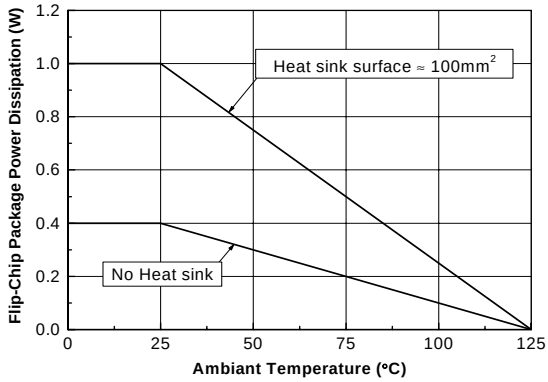


Figure 28. Output power vs. load resistance

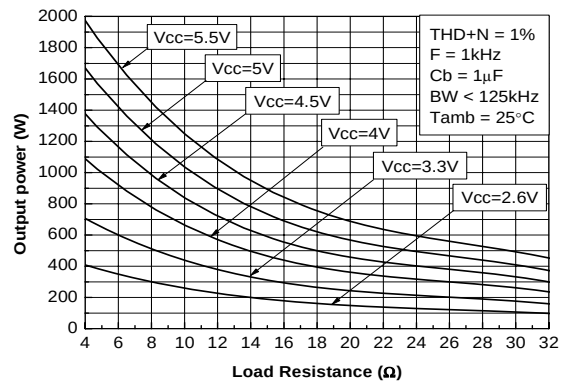


Figure 29. Power dissipation vs. output power

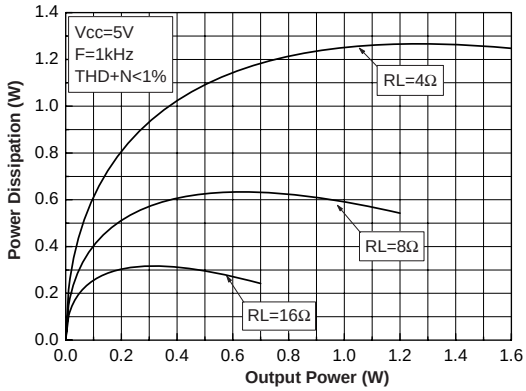


Figure 30. Power dissipation vs. output power

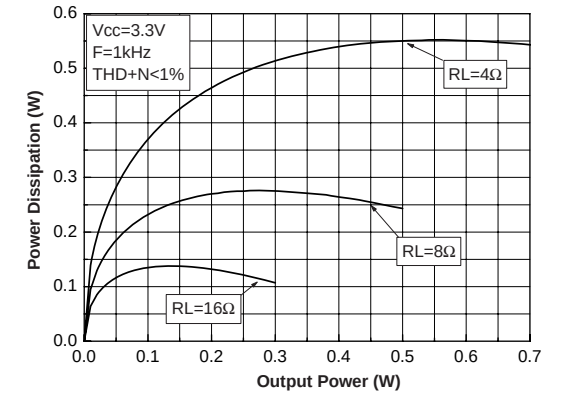


Figure 31. Power dissipation vs. output power

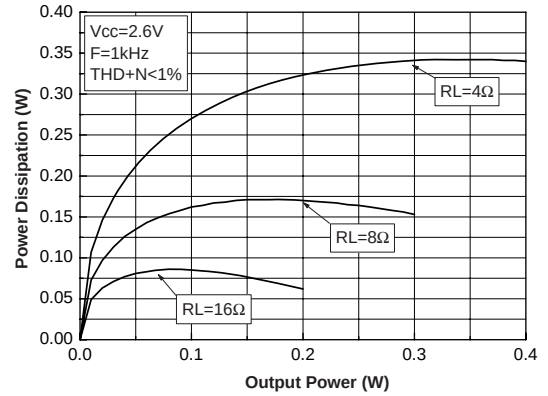


Figure 32. PSSR vs. frequency

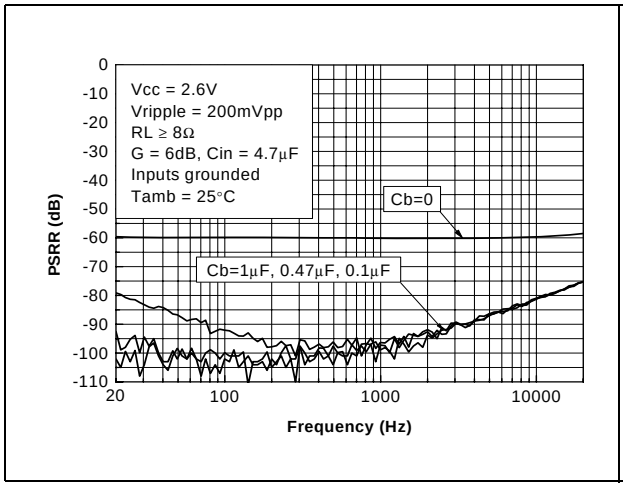


Figure 33. PSSR vs. frequency

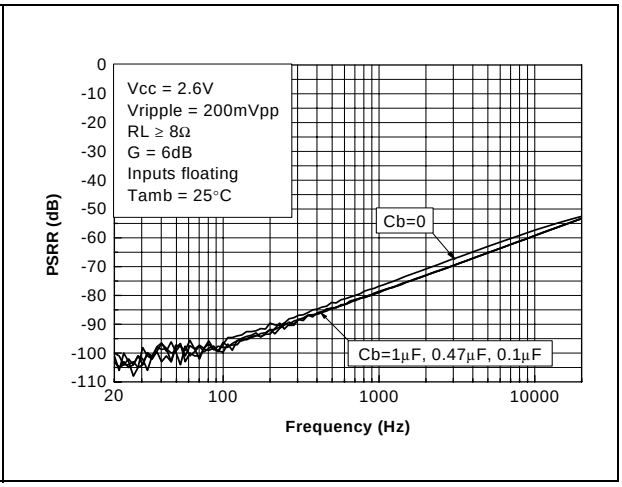


Figure 34. PSSR vs. frequency

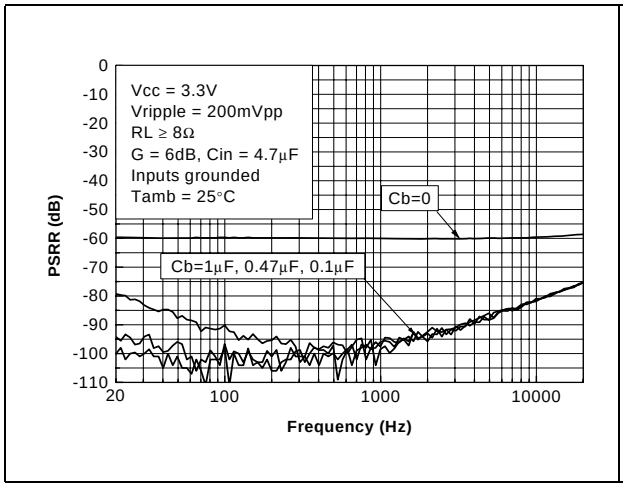


Figure 35. PSSR vs. frequency

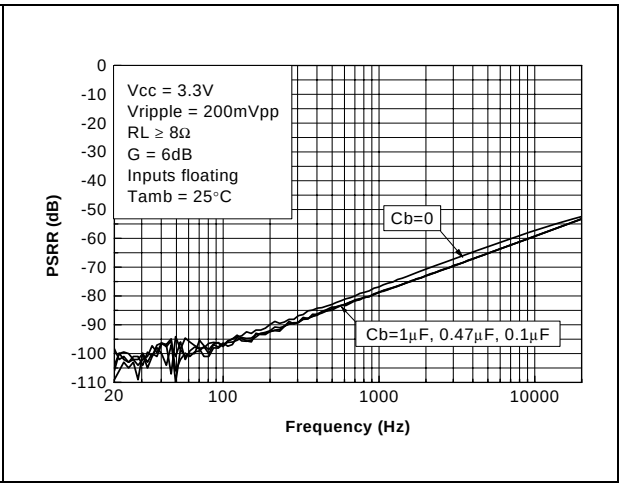


Figure 36. PSSR vs. frequency

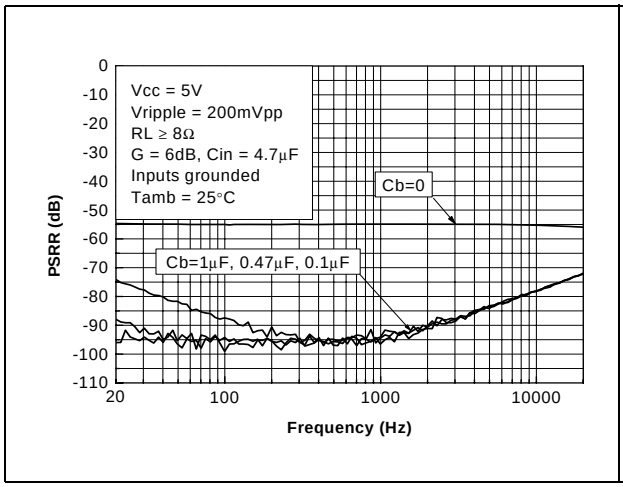


Figure 37. PSSR vs. frequency

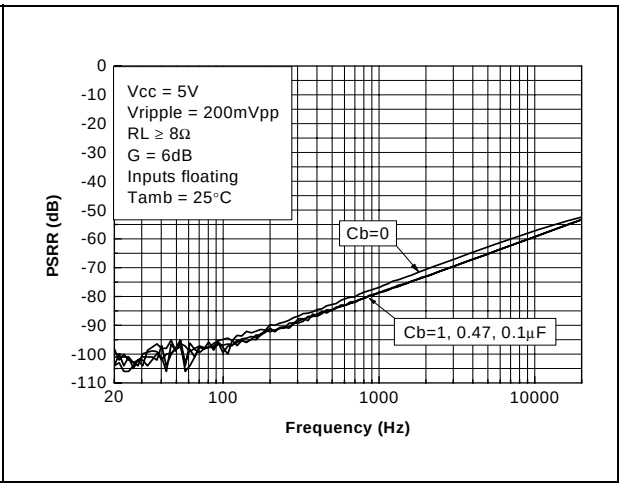


Figure 38. PSSR vs. common mode input voltage

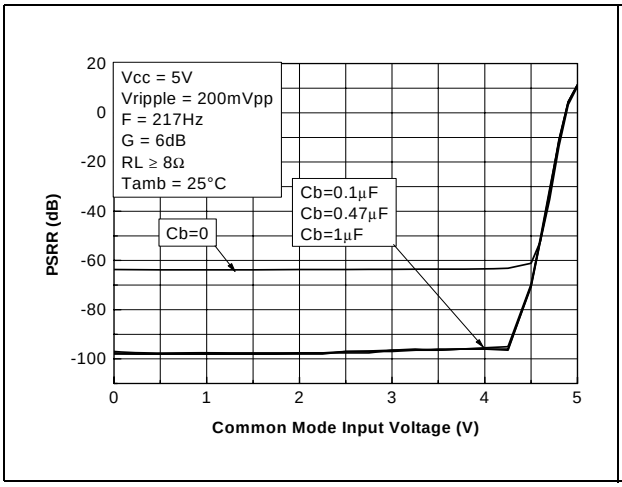


Figure 39. PSSR vs. common mode input voltage

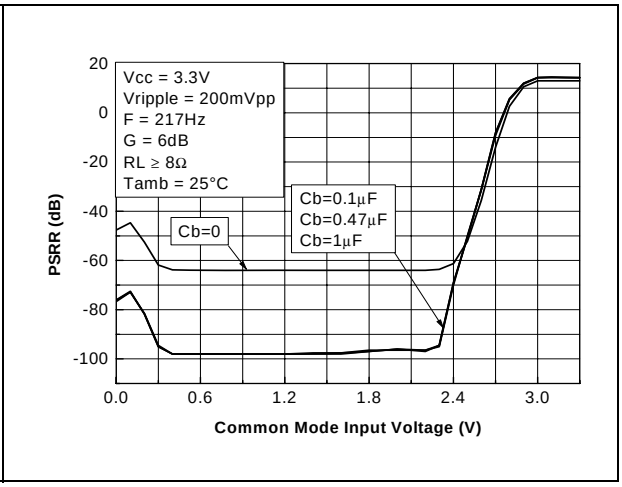


Figure 40. PSSR vs. common mode input voltage

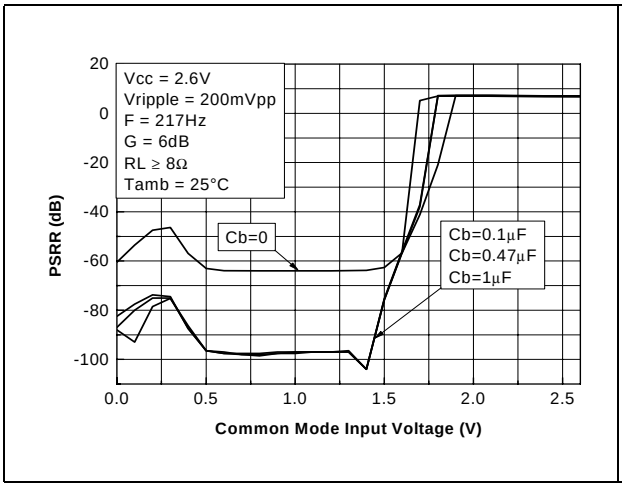


Figure 41. CMRR vs. frequency

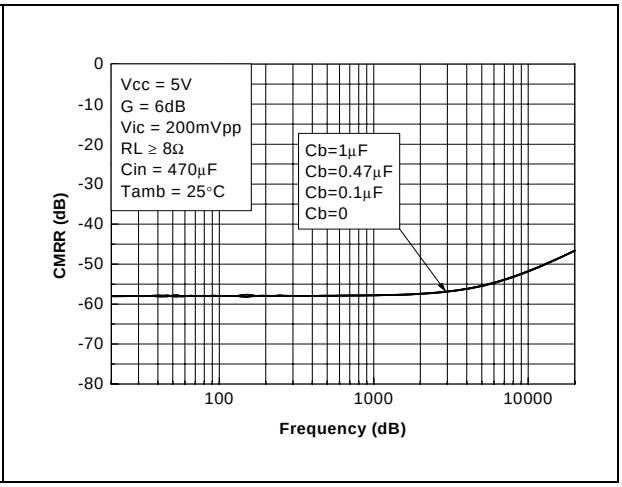


Figure 42. CMRR vs. frequency

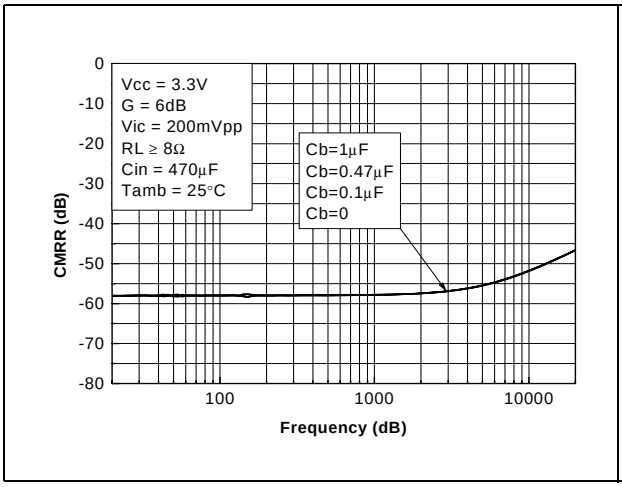


Figure 43. CMRR vs. frequency

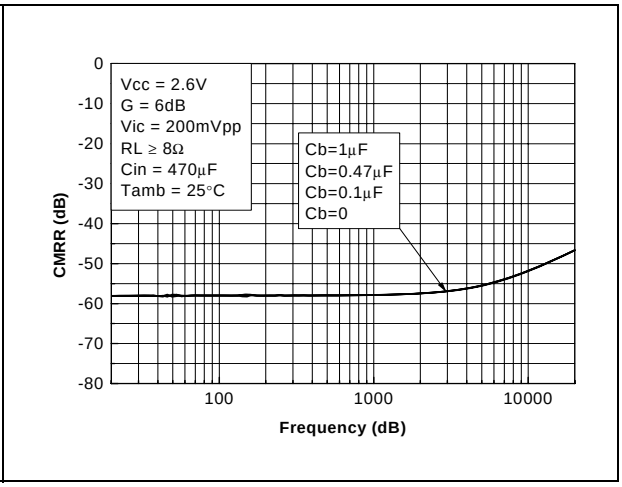


Figure 44. CMRR vs. common mode input voltage

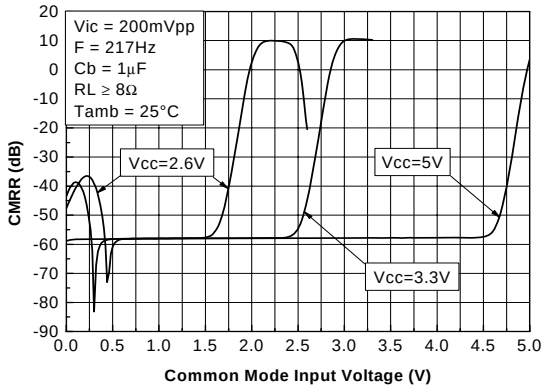


Figure 45. CMRR vs. common mode input voltage

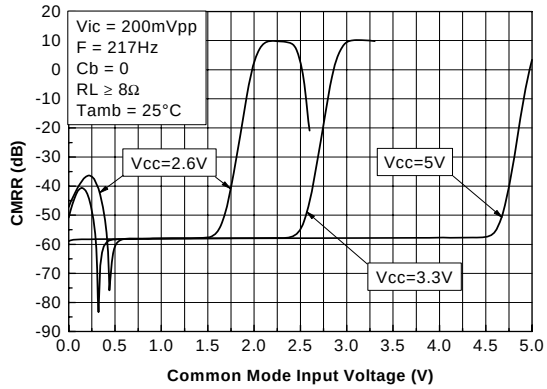


Figure 46. Current consumption vs. power supply voltage

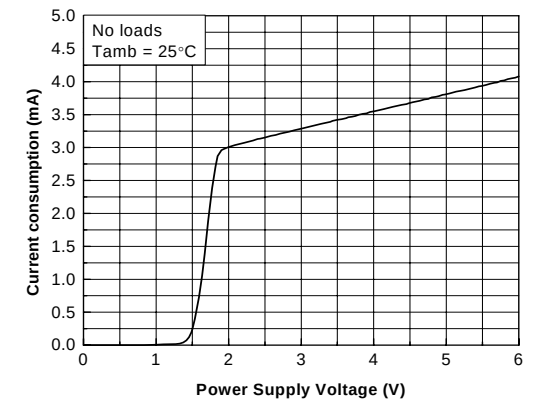


Figure 47. Differential DC output voltage vs. common mode input voltage

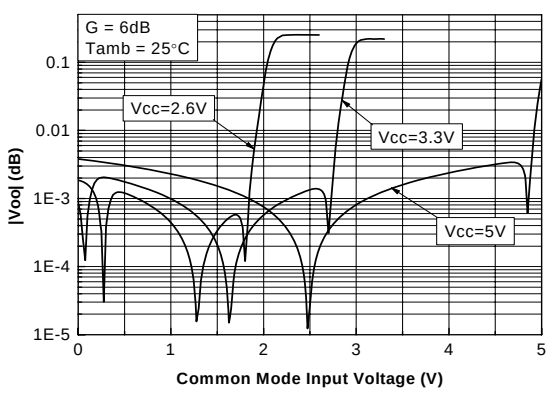


Figure 48. Current consumption vs. standby voltage

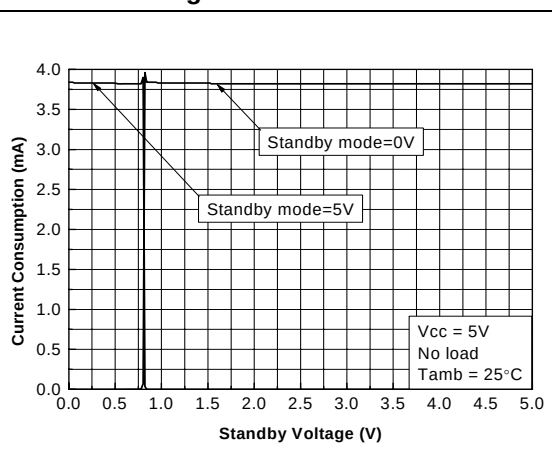


Figure 49. Current consumption vs. standby voltage

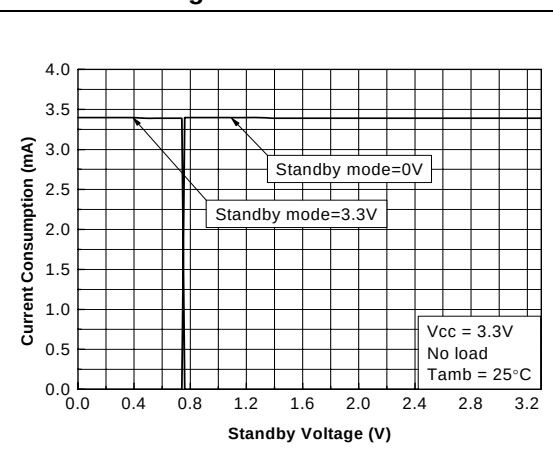


Figure 50. Current consumption vs. standby voltage

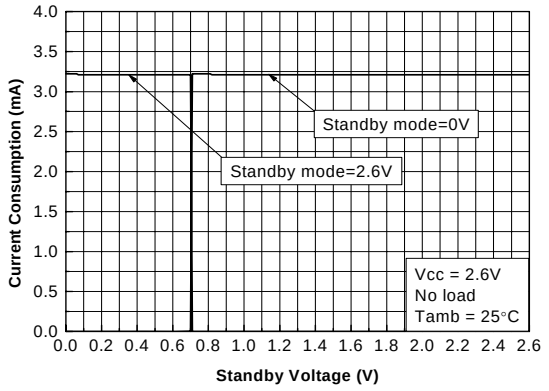


Figure 51. Frequency response

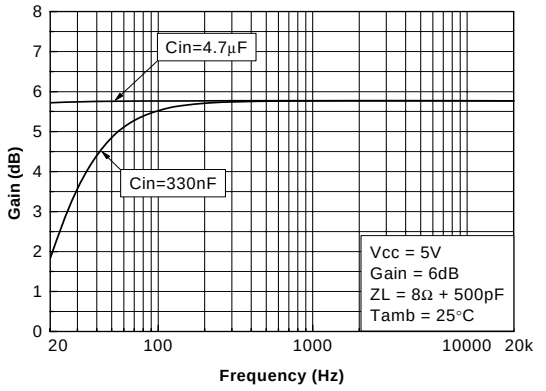


Figure 52. Frequency response

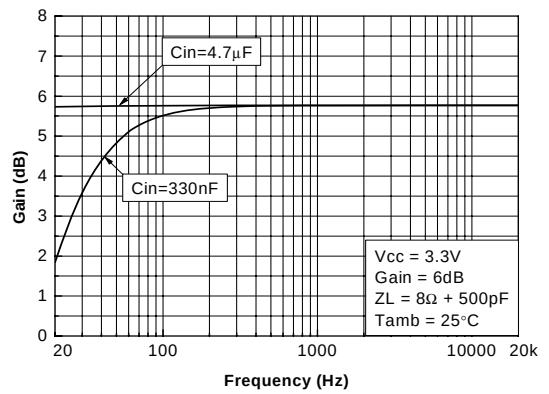


Figure 53. Frequency response

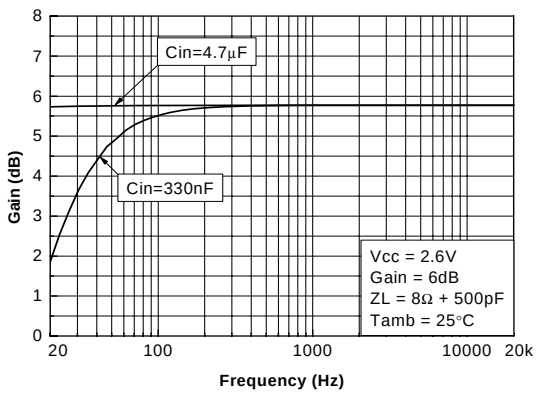


Figure 54. SNR vs. power supply voltage with unweighted filter

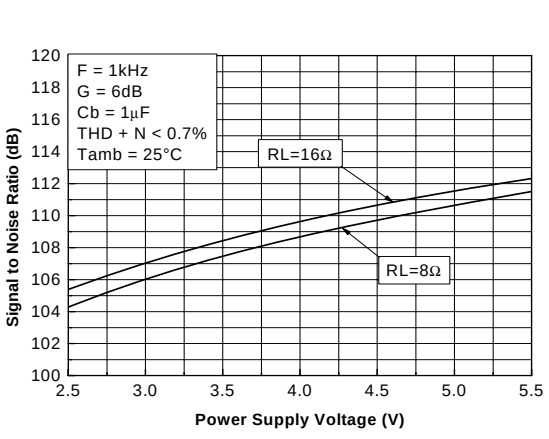
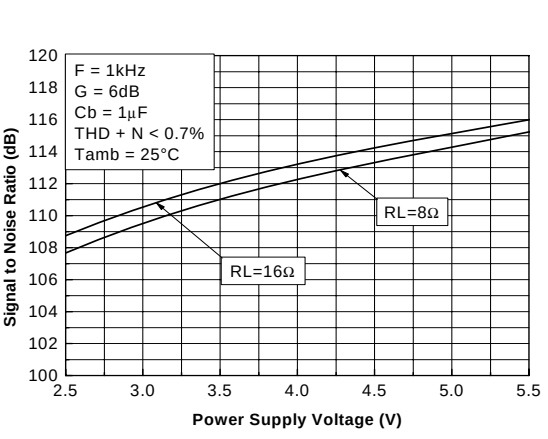


Figure 55. SNR vs. power supply voltage with A-weighted filter



4 Application information

4.1 Differential configuration principle

The TS4995 is a monolithic full-differential input/ output power amplifier with fixed +6 dB gain. The TS4995 also includes a common mode feedback loop that controls the output bias value to average it at $V_{CC}/2$ for any DC common mode input voltage. This allows maximum output voltage swing, and therefore, to maximize the output power. Moreover, as the load is connected differentially instead of single-ended, output power is four times higher for the same power supply voltage.

The **advantages** of a full-differential amplifier are:

- Very high PSRR (power supply rejection ratio)
- High common mode noise rejection
- Virtually no pop and click without additional circuitry, giving a faster start-up time compared to conventional single-ended input amplifiers
- Easier interfacing with differential output audio DAC
- No input coupling capacitors required due to common mode feedback loop

In theory, the filtering of the internal bias by an external bypass capacitor is not necessary. However, to reach maximum performance in all tolerance situations, it is recommended to keep this option.

4.2 Common mode feedback loop limitations

As explained previously, the common mode feedback loop allows the output DC bias voltage to be averaged at $V_{CC}/2$ for any DC common mode bias input voltage.

Due to the V_{IC} limitation of the input stage (see *Table 4 on page 5*), the common mode feedback loop can fulfil its role only within the defined range.

4.3 Low frequency response

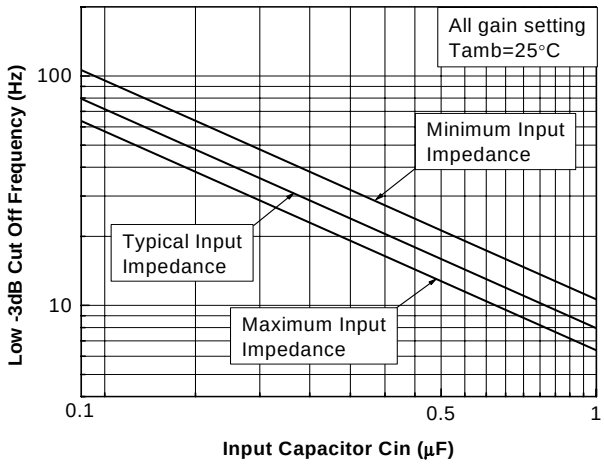
The input coupling capacitors block the DC part of the input signal at the amplifier inputs. C_{in} and R_{in} form a first-order high pass filter with -3 dB cut-off frequency.

$$F_{CL} = \frac{1}{2 \times \pi \times R_{in} \times C_{in}} \quad \text{(Hz)}$$

Note: The input impedance for the TS4995 is typically 20kΩ and there is tolerance around this value.

From *Figure 56*, you can easily establish the C_{in} value required for a -3 dB cut-off frequency.

Figure 56. -3 dB lower cut-off frequency vs. input capacitance



4.4 Power dissipation and efficiency

Assumptions:

- Load voltage and current are sinusoidal (V_{out} and I_{out})
- Supply voltage is a pure DC source (V_{CC})

The output voltage is:

$$V_{out} = V_{peak} \sin\omega t \text{ (V)}$$

and

$$I_{out} = \frac{V_{out}}{R_L} \text{ (A)}$$

and

$$P_{out} = \frac{V_{peak}^2}{2R_L} \text{ (W)}$$

Therefore, the average current delivered by the supply voltage is:

Equation 1

$$Icc_{AVG} = 2\frac{V_{peak}}{\pi R_L} \text{ (A)}$$

The power delivered by the supply voltage is:

Equation 2

$$P_{supply} = V_{CC} I_{ccAVG} \text{ (W)}$$

Therefore, the **power dissipated by each amplifier** is:

$P_{diss} = P_{supply} - P_{out}$ (W)

$$P_{diss} = \frac{2\sqrt{2}V_{CC}}{\pi\sqrt{R_L}}\sqrt{P_{out}} - P_{out}$$

and the maximum value is obtained when:

$$\frac{\partial Pdiss}{\partial P_{out}} = 0$$

and its value is:

Equation 3

$$Pdissmax = \frac{2Vcc^2}{\pi^2 R_L} \text{ (W)}$$

Note: This maximum value is only dependent on the power supply voltage and load values.

The **efficiency** is the ratio between the output power and the power supply:

Equation 4

$$\eta = \frac{P_{out}}{P_{supply}} = \frac{\pi V_{peak}}{4V_{CC}}$$

The maximum theoretical value is reached when $V_{peak} = V_{CC}$, so:

$$\eta = \frac{\pi}{4} = 78.5\%$$

The maximum die temperature allowable for the TS4995 is 125° C. However, in case of overheating, a thermal shutdown set to 150° C, puts the TS4995 in standby until the temperature of the die is reduced by about 5° C.

To calculate the maximum ambient temperature T_{amb} allowable, you need to know:

- The power supply voltage, V_{CC}
- The load resistor value, R_L
- The package type, R_{thja}

Example: V_{CC}=5 V, R_L=8 Ω, $R_{thja\text{-}flipchip}$= 100° C/W (100 mm^2 copper heatsink).

Using the power dissipation formula given above in *Equation 3*, this gives a result of:

$P_{dissmax}$ = 633mW

T_{amb} is calculated as follows:

Equation 5

$$T_{amb} = 125° C - R_{thja} \times P_{dissmax}$$

Therefore, the maximum allowable value for T_{amb} is:

T_{amb} = 125-100x0.633=61.7° C

4.5 Decoupling of the circuit

Two capacitors are needed to correctly bypass the TS4995: a power supply bypass capacitor C_S and a bias voltage bypass capacitor C_b.

The C_S capacitor has particular influence on the THD+N at high frequencies (above 7 kHz) and an indirect influence on power supply disturbances. With a value for C_S of 1 µF, one can expect THD+N performance similar to that shown in the datasheet.

In the high frequency region, if C_S is lower than 1 µF, then THD+N increases and disturbances on the power supply rail are less filtered.

On the other hand, if C_S is greater than 1 µF, then those disturbances on the power supply rail are more filtered.

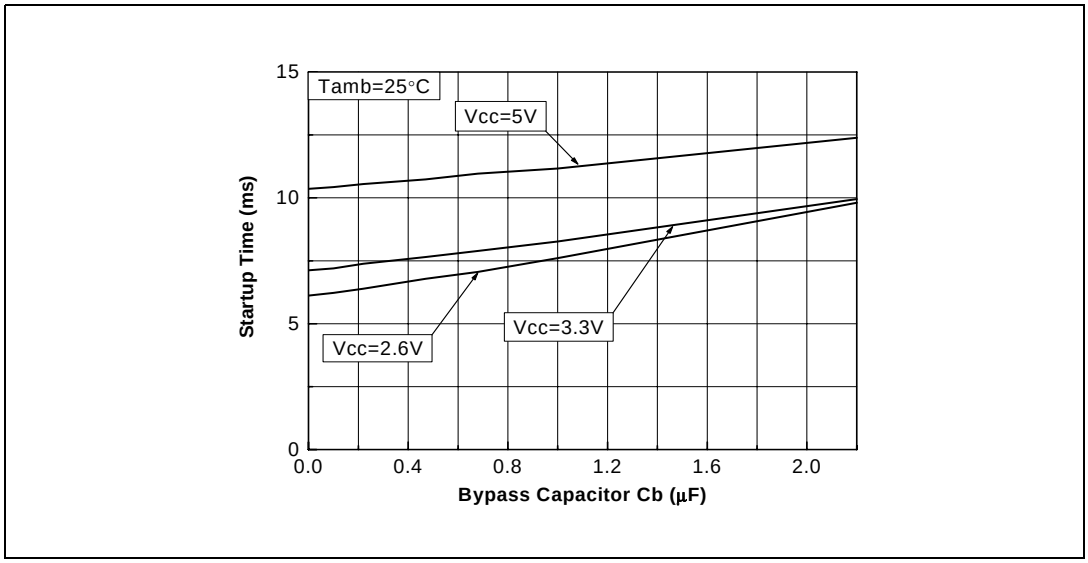
The C_b capacitor has an influence on the THD+N at lower frequencies, but also impacts PSRR performance (with grounded input and in the lower frequency region).

4.6 Wake-up time t_{WU}

When the standby is released to put the device ON, the bypass capacitor C_b is not charged immediately. Because C_b is directly linked to the bias of the amplifier, the bias will not work properly until the C_b voltage is correct. The time to reach this voltage is called the wake-up time or t_{WU} and is specified in *Table 4 on page 5*, with C_b=1 µF. During the wake-up phase, the TS4995 gain is close to zero. After the wake-up time, the gain is released and set to its nominal value.

If C_b has a value different from 1 µF, then refer to the graph in *Figure 57* to establish the corresponding wake-up time.

Figure 57. Startup time vs. bypass capacitor



4.7 Shutdown time

When the standby command is set, the time required to put the two output stages in high impedance and the internal circuitry in shutdown mode is a few microseconds.

Note: In shutdown mode, the Bypass pin and V_{in}+, V_{in}- pins are shorted to ground by internal switches. This allows a quick discharge of C_b and C_{in}.

4.8 Pop performance

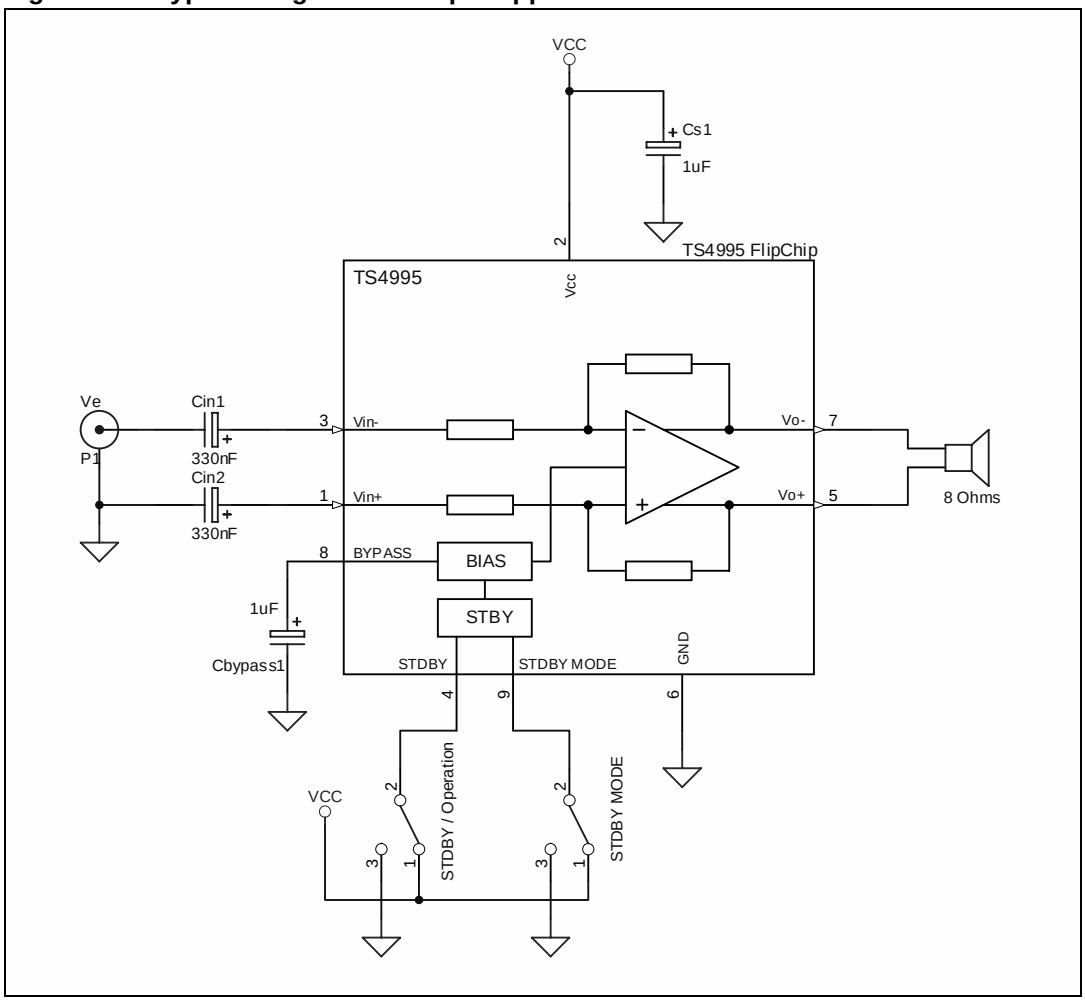
Due to its fully differential structure, the pop performance of the TS4995 is close to perfect. However, due to mismatching between internal resistors R_{in}, R_{feed}, and external input capacitors C_{in}, some noise might remain at startup. To eliminate the effect of mismatched components, the TS4995 includes pop reduction circuitry. With this circuitry, the TS4995 is close to zero pop for all possible common applications.

In addition, when the TS4995 is in standby mode, due to the high impedance output stage in this configuration, no pop is heard.

4.9 Single-ended input configuration

It is possible to use the TS4995 in a single-ended input configuration. However, input coupling capacitors are needed in this configuration. The schematic diagram in *Figure 58* shows an example of this configuration.

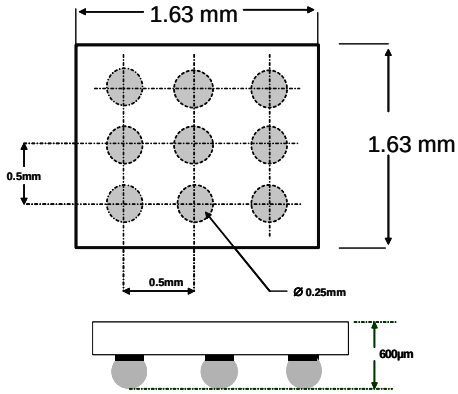
Figure 58. Typical single-ended input application



5 Package information

To meet environmental requirements, STMicroelectronics offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an STMicroelectronics trademark. ECOPACK specifications are available at: www.st.com.

Figure 59. 9-bump flip-chip package mechanical drawing



- Die size: 1.63mm x 1.63mm ± 30µm
- Die height (including bumps): 600µm
- Bumps diameter: 315µm ±50µm
- Bump diameter before reflow: 300µm ±10µm
- Bumps height: 250µm ±40µm
- Die height: 350µm ±20µm
- Pitch: 500µm ±50µm
- Coplanarity: 60µm max

Figure 60. Tape and reel schematics

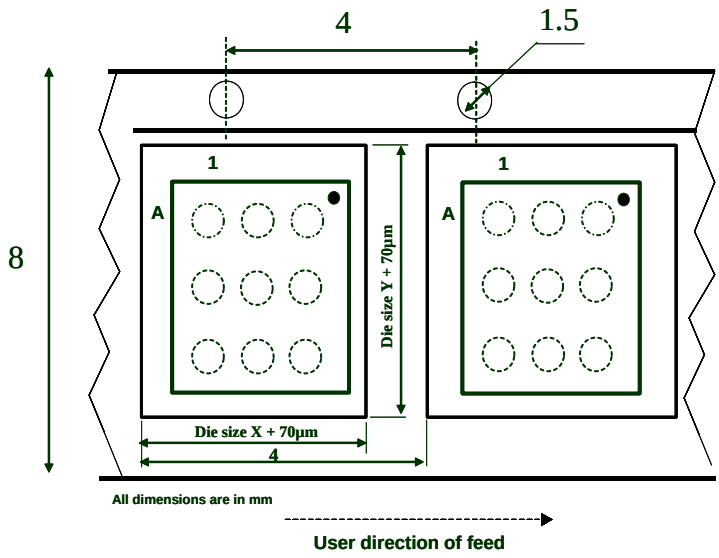
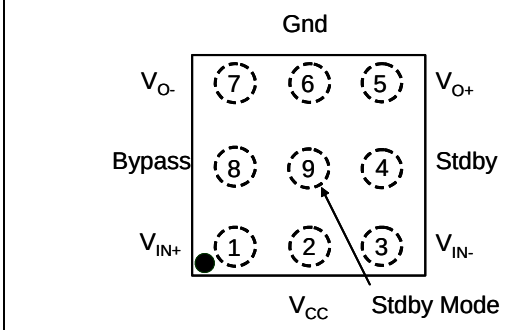
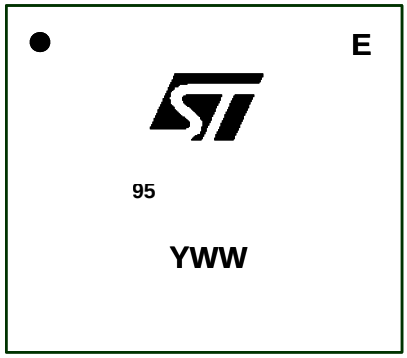


Figure 61. Pin out (top view)



– Balls are underneath

Figure 62. Marking (top view)



6 Ordering information

Table 7. Order code

Order code	Temperature range	Package	Packing	Marking
TS4995EIJT	-40° C to +85° C	Lead free flip chip 9	Tape & reel	95

7 Revision history

Table 8. Document revision history

Date	Revision	Changes
1-Jun-2006	1	Final datasheet.
25-Oct-2006	2	Additional information for 4Ω load.
25-Mar-2008	3	Modified *Figure 60: Tape and reel schematics* to correct die orientation.

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST’s terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST’S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

UNLESS EXPRESSLY APPROVED IN WRITING BY AN AUTHORIZED ST REPRESENTATIVE, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS "AUTOMOTIVE GRADE" MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER’S OWN RISK.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com